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Wafer-scalable, aligned carbon nanotube transistors operating at frequencies of over 100 GHz

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Wireless device technology operating in the millimetre-wave regime (30 to 300 GHz) increasingly needs to offer both high performance and a high level of integration with complementary metal–oxide–semiconductor (CMOS) technology. Aligned carbon nanotubes are proposed as an alternative to III–V technologies in such applications because of their highly linear signal amplification and compatibility with CMOS. Here we report the wafer-scalable fabrication of aligned carbon nanotube field-effect transistors operating at gigahertz frequencies. The devices have gate lengths of 110 nm and are capable, in distinct devices, of an extrinsic cutoff frequency and maximum frequency of oscillation of over 100 GHz, which surpasses the 90 GHz cutoff frequency of radio-frequency CMOS devices with gate lengths of 100 nm and is close to the performance of GaAs technology. Our devices also offer good linearity, with distinct devices capable of a peak output third-order intercept point of 26.5 dB when normalized to the 1 dB compression power, and 10.4 dB when normalized to d.c. power.

As wireless devices migrate to higher-frequency operating bands, such as 5G millimetre wave, the monolithic integration of previously separate technologies—including GaAs power amplifiers, complementary metal–oxide–semiconductor (CMOS) control circuits and silicon-on-insulator switches—into a common platform becomes increasingly important. Such integration is required to lower the parasitic effects originating from the wirebonds and traces that are common in system-in-package solutions[1]. The integration is also driven by the desire for advanced functionality, as more CMOS control circuits are needed to manage complex radio-frequency (RF) front ends, which can include multiple circuit pathways for multiband operations, as well as features such as multiple input and multiple output (MIMO), beamforming, carrier aggregation and envelope tracking.

III–V technologies, such as GaAs pseudomorphic high-electron-mobility transistors (pHEMTs), have been the standard for high-linearity, low-noise applications in the microwave and millimetre bands for decades[2]. However, their use of GaAs substrates makes them incompatible with Si CMOS integration. This is a major limitation that has led to the loss of market share to RF-CMOS, despite the fact that GaAs offers superior performance[1,3].

Aligned carbon nanotube field-effect transistor (aCNT-FET) technology relies on a simple, room-temperature surface-coating method to apply nanotubes to a substrate. This decouples the semiconductor material from a specific type of bulk substrate and allows high-level integration with CMOS for system-on-chip-level complexity, which has been demonstrated recently for a mixed CNT–CMOS digital circuit application[4]. Unlike the incumbent technologies, such as pHEMTs, which create charge confinement within a bulk material via a heterostructure-derived two-dimensional electron gas layer, the charges in CNTs are naturally confined in one dimension, which leads to desirable transport characteristics. For example, quasiballistic transport has been observed for tube lengths of 300 nm, which is a direct consequence of its reduced scattering degrees of freedom[5]. Empirically observed current density and transconductance values of up to 25 μA (ref. [5]) and 20–40 μS (refs. [6–9]), respectively, have been reported for single-tube measurements, which on scaling into dense arrays would exceed those of the incumbent technologies.

Theoretical[10,11] and empirical[12] work also suggests that this one-dimensional (1D) charge transport allows CNT-FETs to achieve highly linear signal amplification. Modern wireless technology increasingly relies on highly linear devices to achieve spectral-efficient modulation (that is, more data per unit bandwidth) and high spurious-free dynamic range to extract weak signals from increasingly crowded airwaves. Achieving high linearity at low d.c. power levels would be an additional advantage for power-constrained applications.

Although these CNT characteristics have been known on an individual tube basis, to make a useful amplifier it is necessary to produce an array of thousands of aligned semiconducting CNTs operating in parallel. The two primary engineering challenges for radio-frequency CNT-FETs—enriching as-produced CNTs to a high semiconducting fraction (>99.9%; ref. [13]) and assembling them into densely aligned arrays (up to 70 tubes μm^{-1}; refs. [14–16])—have been overcome. The challenge now turns to device-level process improvements that will harness the fundamental material advantages of CNTs.

In this Article, we report a wafer-scalable process for creating aCNT-FET devices. We use the approach to fabricate hundreds of devices and show that they offer improved RF performance characteristics compared with previous CNT-FETs; Fig. 1a shows the

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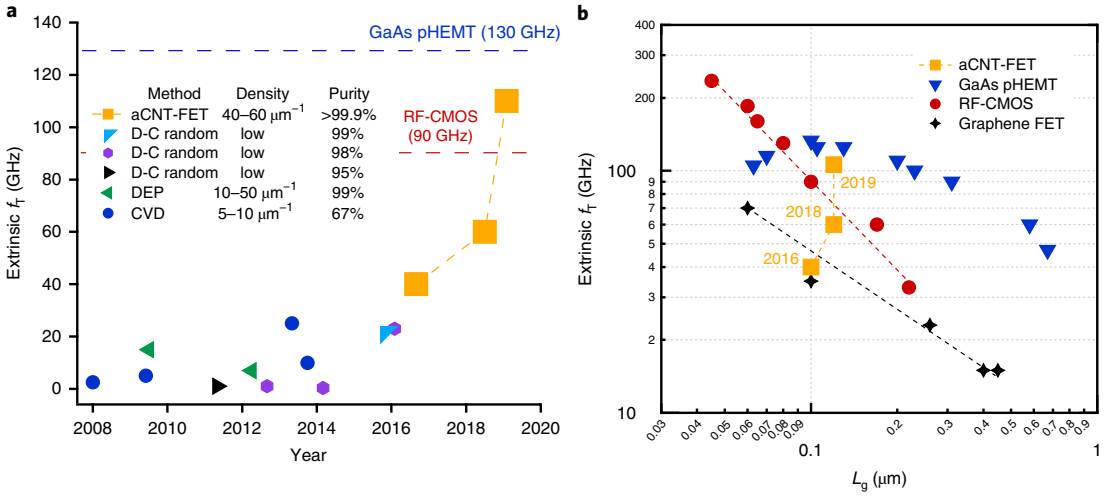

Fig. 1 | The technology evolution of RF CNT-FET devices. a, The extrinsic f_T versus year shows the rapid rate of advancement once the engineering challenges of achieving (1) high-purity semiconducting CNTs (>99.9%[13]) in (2) dense, aligned arrays (40–60 CNTs μm^{-1})[15] were overcome. Combining these improvements with our T-gate device process has allowed the CNTs' underlying properties to more materially manifest at gigahertz frequencies. Previous methods such as chemical vapour deposition (CVD)[31,37–39], dielectrophoresis (DEP)[40,41] and drop-cast (D-C) random CNTs at semiconductor enrichments of 95% (ref. [32]), 98% (refs. [33,34]) and 99% (ref. [30]) were held back by the following factors: low densities, random network morphology, low semiconducting purity and/or a high bundle fraction of CNTs. For comparison, the dashed horizontal lines indicate f_T for the incumbent technologies of GaAs pHEMT, 130 GHz at 100 nm gate length[18], and 130 nm node RF-CMOS, 90 GHz at 100 nm gate length[24]. **b**, The f_T versus L_g for our work from 2016 (ref. [15]), 2018 (ref. [22]) and 2019 (this work), which exceeds RF-CMOS[24], is nearly on par with GaAs pHEMTs[18], and clearly superior to graphene devices[35,42–44]. The dashed lines are employed to indicate trends.

improvement in extrinsic cutoff frequency (f_T) of reported CNT-FET devices over the last decade. We also demonstrate that the performance metrics of the devices, including their f_T, exceed or challenge those of RF-CMOS and GaAs pHEMT technologies (Fig. 1b).

Aligned CNT deposition

Dense, aligned arrays of high-semiconducting-purity (>99.9% as determined optically), polymer-sorted single-walled CNTs with linear densities of 40–60 CNTs μm^{-1} (inclusive of individual CNTs and bundles of ≥2 CNTs) were deposited over a 20 × 30 mm^2 area of the wafers using our ZEBRA technology, a modified version (Methods) of the floating evaporative self-assembly process first codeveloped by the Arnold and Gopalan Groups at the University of Wisconsin, Madison[16].

During the deposition process, CNT ink is dosed dropwise, leading to bands of aligned CNTs that have a mean width of 28 μm as shown in Fig. 2b,d. Between these aligned bands are interface regions having a mean width of ~5 μm and composed of generally aligned CNTs as shown in the SEM images of Fig. 2b,c. This overcomes an initial limitation of floating evaporative self-assembly[16,17], where the size and spacing of aligned CNT bands yielded <50% linear coverage for a wide-channel device due to bare substrate regions existing between the aligned bands and randomly-oriented-CNT regions at the band edges. We have observed that by reducing surface waves on the water subphase during deposition the CNT-ink–water–substrate contact line becomes more stable in the axis normal to the subphase surface and results in contiguous bands of aligned CNTs. The CNT morphology as patterned and introduced into an aCNT-FET device is depicted in the SEM images of Fig. 2e,g, while Fig. 2h shows an AFM height image of monolayer CNTs on a typical ZEBRA wafer.

To determine the wafer coverage of densely aligned CNTs, a high density of identical devices, with gate length (L_g) = 400 nm, were patterned on a silicon wafer (with 50 nm thermally oxidized SiO_2) and their d.c. characteristics were measured using a Cascade automated probe station. By averaging the maximum achieved drain current, $I_{d,max}$, data from the 12 devices in each 1.5 mm × 1.5 mm die (over 4,700 devices in total), a wafer map was created that effectively depicts the CNTs' relative density and alignment across the wafer, as shown in Fig. 2f. The densest and best aligned CNTs are located near the centre horizontal axis of the wafer because of its proximity to the CNT-ink dispenser during the deposition process[16]. The degree of alignment lessens and the linear density decreases away from this region, leading to the observed reduction in $I_{d,max}$. No fundamental limitations exist to scaling up the process to an arbitrarily sized deposition area, but such an effort has not been the focus of this proof-of-concept work.

Fabrication of aCNT-FET devices

Fabrication of the RF aCNT-FET devices was performed using standard, scalable, semiconductor tools on 100-mm-diameter, single-crystal quartz wafers. After the aligned CNT deposition, as described in the previous section, a combination of electron-beam lithography (EBL) and stepper-based photolithography was used for all patterning. Source and drain contact electrodes were patterned first by EBL to (1) deposit the Pd contact metal onto the cleanest possible interface by avoiding accumulated contaminants from subsequent processing, (2) decouple the source–drain length dimension from that of the gate size, which is a constraint when self-aligned contacts are used[15], and (3) reduce the accumulation of CNT bundling during processing. This was followed by photolithographic patterning of the CNT channel area and metal pads in a coplanar waveguide arrangement. We utilize a T-shaped gate geometry, commonly used in III–V HEMT devices[18], since it is effective at minimizing the gate length (for short carrier transit times) while simultaneously minimizing the gate resistance (by increasing the overall gate cross-section). The T-gates were patterned by EBL using a trilayer polymethyl methacrylate (PMMA) stack and metallized with 240 nm of Al/Ni/Au, as shown in Fig. 3. The dielectric was formed by oxidizing the Al gate metal to form a thin, self-terminating layer of Al_2O_3. We estimate the oxide thickness to be ~4.5 nm

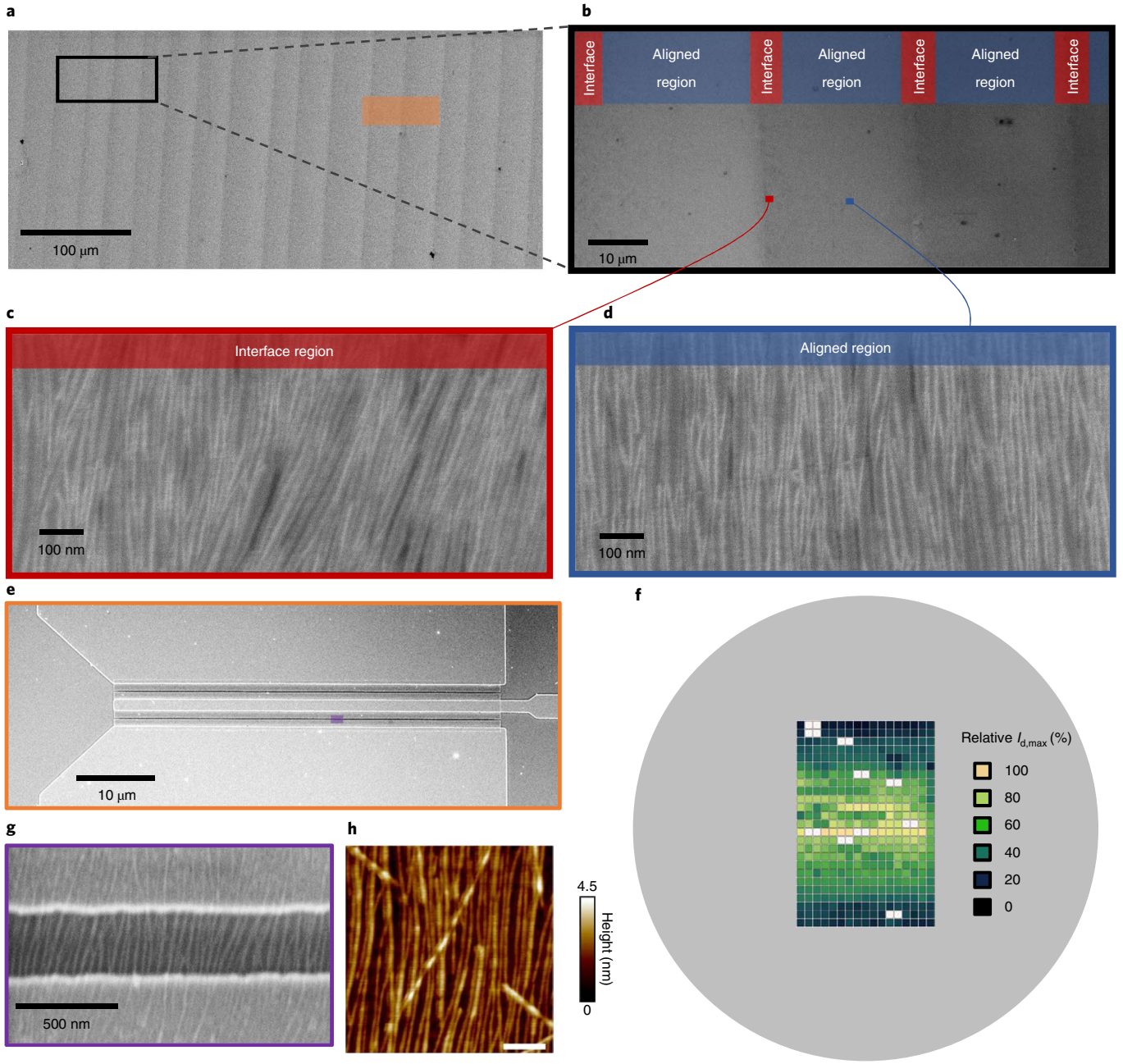

Fig. 2 | Aligned CNT arrays for RF-FET. Device fabrication began with the deposition of dense, aligned arrays of high-semiconducting-purity CNTs. **a–d**, CNT ink is dosed onto the surface in a dropwise fashion, leading to bands of aligned CNTs (**a**–**c**) separated by smaller interface regions (**d**) that consist of generally aligned CNTs. **e**, SEM image depicting a 2×50 µm wide FET channel (2×50 µm wide d.c. test device shown; RF devices in this article are all 2×25 µm physical gate width). **f**, A wafer map of a typical ZEBRA wafer created using the relative $I_{d,max}$ as a proxy for CNT density and alignment: the best alignment and density occur in a 15-mm-wide band in the centre of the wafer. Dies with white squares were voided due to device defects. **g**, SEM image depicting aligned CNTs in the FET channel contacted by the source and drain electrodes. The orange rectangle in **a** depicts the field of view of **e**, to scale, showing the size of the aCNT-FET devices with respect to the bands of aligned CNTs. The purple rectangle in **e** depicts the field of view of **g**, to scale, showing aligned CNTs that form a fraction of the array in each aCNT-FET device. **h**, The AFM height map. Scale bar, 100 nm.

by ellipsometry on Al films deposited and oxidized using the same process. The T-gates had L_g of 110 nm and source–drain lengths (L_{sd}) of 160 nm for one device set (wafers 1 and 2), and L_g = 135 nm, L_{sd} = 190 nm for the other set (wafers 3 and 4), with both sets having channel widths of 2×25 µm. At this width, each aCNT-FET contained an array of 2,000 to 3,000 CNTs in parallel. These device widths were increased from the previous work (2×10 µm; refs. [15,16]), an advancement made scalable by our development of contiguously deposited aligned CNT films, as detailed above. Larger widths are integral to producing CNT-FET devices useful for monolithic microwave integrated circuit RF amplifier applications.

D.c. and RF characterization of T-gate devices

Initial d.c. device characterization was performed on four wafers to screen for champion devices, with a maximum drain–source voltage (V_{ds}) magnitude of −1.0 V. Transfer curves (width-scaled drain current density I_d as a function of gate–source bias V_{gs}) were acquired and devices with a high-bias $I_{on}/I_{off} > 30$ and $I_{d,max} > 200$ mA mm^{-1}

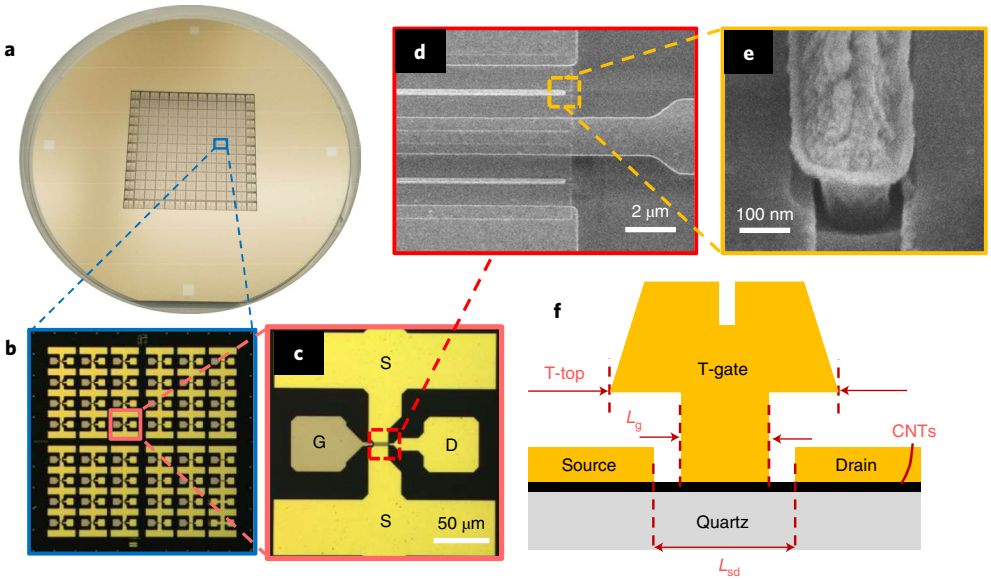

Fig. 3 | aCNT-FET devices fabricated with a wafer-scalable process. a,**b**, aCNT-FET T-gate devices were fabricated on 100 mm quartz wafers (**a**, photograph) and patterned with a 7 × 7 array of dies each containing 46 available devices plus 2 calibration shorts (**b**, optical micrograph) and test dies around the perimeter of the patterned dies. **c**, Optical micrograph of the coplanar waveguide structure of a single aCNT-FET. S, source; G, gate; D, drain. **d**, SEM image of one edge of aCNT-FET device, showing source electrodes (top and bottom), drain electrode (centre) and gate electrodes (centre of channel). **e**, SEM image of a T-gate centred in the channel, taken at a tilt angle of 65°. **f**, Depiction of aCNT-FET device cross-section. T-gate layout dimensions varied between devices on the die. Here we feature devices with L_g ~ 110 nm, L_{sd} ~ 160 nm and T-top ~ 200–250 nm.

were chosen as promising candidates for high-speed RF performance, for a total of 107 devices with L_g ~ 110 nm and 229 devices with L_g ~ 140 nm. Of these, d.c. data from 15 of the top 110 nm gate length devices (from wafer 2) in terms of RF self-gain, RF g_m/ RF g_o, are presented in Fig. 4a,b. Here, RF g_m is the RF transconductance while RF g_o is the RF output conductance and both are calculated using *S*-parameters as described below. The transfer curves $I_d(V_{gs})$ in Fig. 4a were uniform in threshold voltage and current, with $I_{d,max}$ averaging −230 mA mm^{-1} at V_{ds} = −1.0 V with a standard deviation of about 8%. This uniformity was reproduced across the four wafers, as summarized in Supplementary Table 2.1. For the higher biases, the output family of curves $I_d(V_{ds})$ recorded a maximum current density magnitude of −392 mA mm^{-1} among the full set of devices at V_{ds} = −1.5 V, shown in Supplementary Fig. 2.1a. I_{on}/I_{off} was found to be dependent on channel width and source–drain length, as discussed in Supplementary Section 4, as well as bias, as is typical for scaled CNT-FETs[19–21]. Under operating bias (V_{ds} = −1.5 V), I_{on}/I_{off} averaged 50 for the devices discussed here with source–drain lengths of 160 nm, increasing to ~90 for the high RF self-gain devices with source–drain lengths of 190 nm. At low bias (V_{ds} = −10 mV), the mean I_{on}/I_{off} ratio was ~600 for the selected devices, demonstrating the high enrichment of the CNT source material.

For the initial RF characterization, *S*-parameter data were obtained at 1.5 GHz, and transconductance (RF g_m) values were obtained by transforming to *Y*-parameters and solving for the g_m. The data shown in Fig. 4c were scaled by the channel width, and were acquired at multiple static V_{gs} bias points after allowing the current to settle. (Corresponding static-bias output and transfer curves are presented in Supplementary Fig. 2.2.) The highest-performance device of the full set had an RF g_m of 395 mS mm^{-1} while the average over the 15 select devices was 330 mS mm^{-1} at V_{ds} = −1.5 V. The maximum swept bias transconductance derived from the d.c. transfer curves averaged 220 mS mm^{-1} for the back sweep at V_{ds} = −1.0 V, in good agreement with the RF values when scaled by V_{ds}.

The extrinsic (as-measured) f_T and maximum oscillation frequency, f_{max}, were measured at multiple gate-bias points as shown parametrically in Fig. 4e,f. (In this article we present only extrinsic or as-measured data, to emphasize the practical results.) These values were extracted from the *x*-axis intercepts of linefits with −20 dB per decade slopes of the current gain (H_{21}) and the maximum unilateral power gain (U_{MAX}) as a function of frequency (Fig. 4d). The maximum achieved f_T and f_{max} values of the full set of 107 devices was 106 GHz for both metrics on distinct devices, and averaged 77 GHz and 99 GHz, respectively, for those 15 devices selected for Fig. 4. f_T scaled nearly proportionally with the transconductance, as seen in Fig. 4e, curving down slightly for high gate overdrive voltages, V_{gs} < −1.5 V, reflecting an increase in the contributions of parasitics, also exhibited in Supplementary Fig. 2.1b. f_{max} similarly followed a nearly linear relationship with f_T for small gate overdrives, as shown in Fig. 4f, but fell well short of linear for V_{gs} < −1.5 V, possibly reflecting an increasing RF g_o with more negative gate bias even when the RF g_m was stable, as shown in Fig. 4c and Supplementary Fig. 2.1c. Decreasing the gate resistance further will reduce these parasitic effects on f_{max}.

In this set selected for high self-gain, the RF *S*-parameters were uniform with f_T and f_{max} having 6% and 3%, respectively, reflecting the uniformity seen in the d.c. transport characteristics. To explore how well this uniformity in figures of merit might translate to integrated devices, an amplifier model with standard components was designed using Advanced Design System (ADS) software, with a target frequency of maximum amplification of 10 GHz, and the gain S_{21} was calculated versus frequency for 15 devices selected from wafer 2, as shown in Supplementary Fig. 3.2. At the 10 GHz design point, the gain averaged 13.6 dB with a standard deviation of only 1.3%, showing that the variance in the champion transistors will probably not limit amplifier performance. The next step is to package such a device into a single-stage amplifier module, which for a previous (2018) device has been demonstrated and achieved a gain of 11.6 dB at 1.15 GHz (ref. [22]).

aCNT-FET linearity characterization

In modern communication systems, where the airwaves are becoming more and more congested and data density per unit bandwidth is increasing, having high, broadband linear amplification is highly

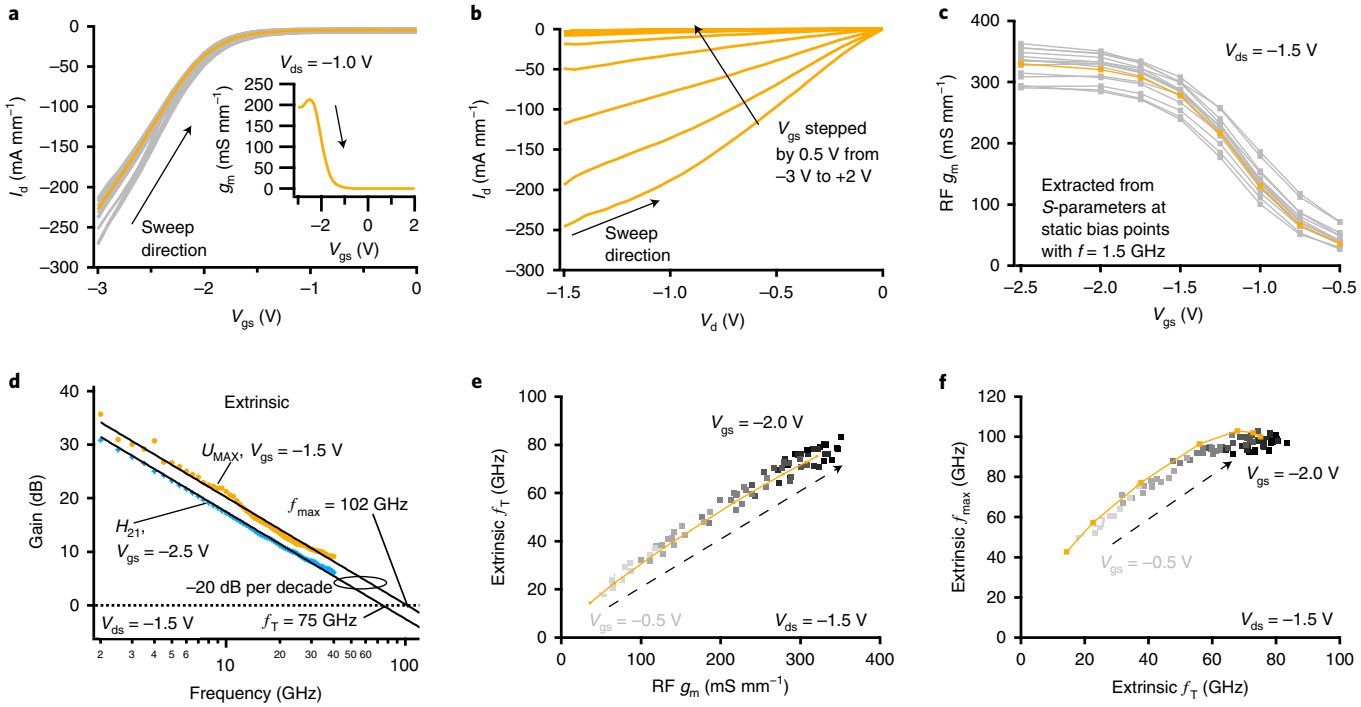

Fig. 4 | D.c. and RF electrical performance of the 15 aCNT-FETs with highest self-gain from wafer 2. Symbols indicate measured data and the solid lines are guides for the eye. The data for the device with the highest f_{max} from the set is highlighted in yellow. **a**, Measured reverse-swept transfer curve $I_d(V_{gs})$. Inset: the calculated reverse-swept-bias $g_m(V_{gs})$ for the highlighted device. **b**, Measured reverse-swept-bias family of (output) curves $I_d(V_{ds})$. **c**, Calculated static-bias RF g_m versus V_{gs}. **d**, Calculated H_{21} and U_{MAX} plotted versus frequency and −20 dB per decade fits (solid lines) for the highlighted device. **e**, Calculated f_T plotted parametrically versus calculated static-bias RF g_m as functions of V_{gs}, as indicated by the dashed arrow and colour gradient. **f**, Calculated f_{max} plotted parametrically versus calculated f_T as functions of V_{gs}, as indicated by the dashed arrow and colour gradient.

desirable. As input levels rise, creating an amplified, linear reproduction of an input signal without distortion is a challenge because nonlinearities in the device transfer function generate third-order intermodulation distortion products (IMD3) by mixing strong input signals. In signal-rich environments, IMD3 power (P_{IMD3}) can exceed the signal-free noise floor, which limits the receiver's sensitivity beyond its system noise figure. The output third-order intercept point (OIP3) is the common figure of merit measured in devices and systems to predict the internally generated IMD3 products resulting from the presence of strong RF signals. A high OIP3 is desirable since a 1 dB increase in OIP3 decreases the IMD3/fundamental signal ratio by 2 dB. Other common figures of merit are arrived at by normalizing OIP3 to the d.c. power consumed (OIP3/P_{dc}) or to the RF output power level associated with compression where device gain decreases by 1 dB from its small-signal value, OIP3/P_{1dB}. Previous work has theoretically suggested[10,11] and later demonstrated[12] that CNT-FETs offer intrinsically superior transfer linearity and therefore higher OIP3/P_{dc} and OIP3/P_{1dB} compared with incumbent semiconductors. Here we show that, within the set of our aCNT-FETs, the respective champion devices had a peak OIP3/P_{dc} of 10.4 dB and an OIP3/P_{1dB} of 26.5 dB. Generally, values exceeding the 10 dB rule of thumb[23] for these figures of merit are considered very good. This is in addition to our previous results that showed OIP3/P_{dc} of 15.7 dB (ref. [22]).

Figure 5a diagrams the linearity measurement system. A two-tone linearity technique was used to measure OIP3 values over a V_{gs} range of −3 V to 0 V, swept as a triangle wave at 1 kHz, which was found to remove most hysteresis, as described in Methods and shown in Fig. 5a. (The slight looping effects of the plotted values in Fig. 5c–g are from the residual hysteresis.) The input signal was composed of two RF fundamentals, 1,498 MHz and 1,502 MHz, at a −14 dBm power level combined with the 1 kHz triangle wave V_{gs}, and the drain bias voltage was held at V_{ds} = −1.5 V. A spectrum analyser, set to its zero-span frequency mode, captured the fundamental and IMD3 distortion product levels as a function of time, while an oscilloscope combined with a differential scope probe captured $V_{gs}(t)$ and $I_d(t)$ as functions of time. This allowed for the parametric determination of OIP3(V_{gs}) and OIP3/P_{dc}(V_{gs}) simultaneously with the transfer curve linearity. The latter was characterized by calculating the effective transconductance, $g_{me}(V_{gs})$, which is equal to $\frac{i_d}{v_{gs}}$ when $z_L \gg \frac{1}{y_o}$; i_d, v_{gs}, z_L and y_o are respectively RF quantities of drain current, gate voltage, output load impedance and drain admittance. When the drain is shorted (that is, $z_L \ll 1/g_o$), $g_{me}(V_{gs})$ approximates the true transconductance, $g_m(V_{gs})$ (Supplementary Section 6). Commercially manufactured GaN FET devices were used to test the measurement system, which showed good agreement for the transconductance values obtained using the various methods.

Figure 5c shows the upper (1,506 MHz) and lower (1,494 MHz) OIP3(V_{gs}) for the OIP3 champion device. The peak OIP3 measured was 17.6 dBm, with an associated gain of −1.6 dB. The low gain is due to driving the gate without a matching network, but the actual maximum stable gain at 1.5 GHz is 25 dB. The upper OIP3 and lower OIP3 originate from the upper- and lower-frequency IMD3 products, respectively, shown in generalized form in Fig. 5h. Their minima correspond to the inflection points of $g_{me}(V_{gs})$ as plotted in Fig. 5d, confirming the validity of the swept measurement method. The peaks of OIP3(V_{gs}), Fig. 5c, correspond roughly to the troughs of P_{IMD3}, Fig. 5e, but not exactly since OIP3 is both proportional to device gain and inversely proportional to P_{IMD3}.

OIP3/P_{dc}(V_{gs}) was calculated, as described in Methods, as the minimum (worst case) of the upper and lower OIP3 at each point of V_{gs}. OIP3/P_{dc} is plotted in Fig. 5f,g for the OIP3 and OIP3/P_{dc} champion aCNT-FET devices and was 4 dB and 10.4 dB, respectively, demonstrating the potential for high linearity in low-noise

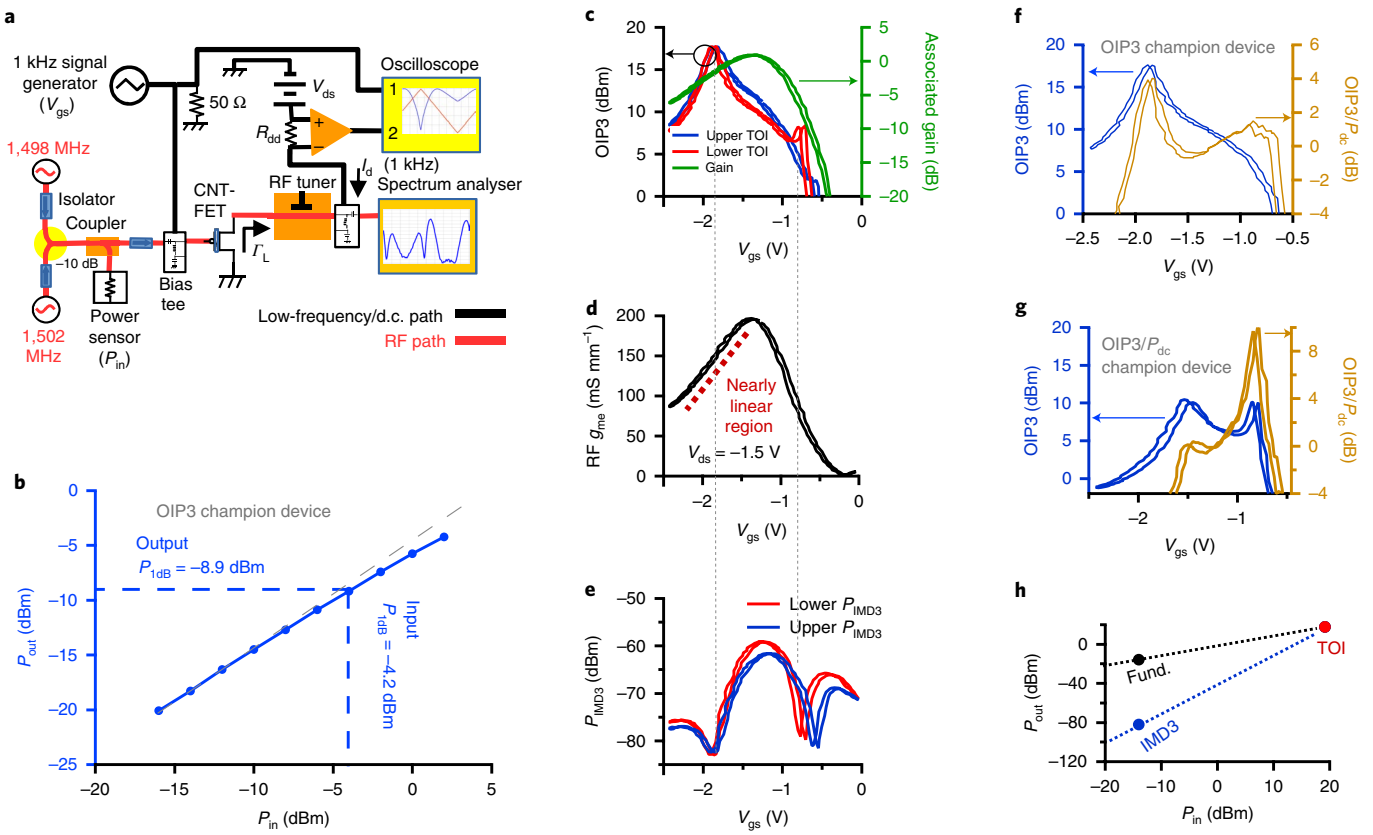

Fig. 5 | Linearity measurements of arrayed CNT-FETs. a, The test setup applies a triangle waveform to the gate of the device under test to measure the transconductance derived from the spectrum analyser RF power, $g_{me}(V_{gs})$ (Methods and Supplementary Section 6), IMD3(V_{gs}) and upper/lower OIP3(V_{gs}). V_{gs} is swept at a 1 kHz rate to minimize hysteresis effects and the tuner is adjusted to maximize the peak OIP3. **b**, One-tone power gain plot depicting 1 dB compression. **c**, OIP3 and gain. TOI, third-order-intercept. **d**, RF g_{me}. **e**, P_{IMD3} versus gate voltage. In **c**–**e** the vertical dotted lines are provided as guides to the eye to indicate features at common gate voltages. **f**,**g**, Composite OIP3(V_{gs}) (minimum OIP3 of upper and lower) and OIP3/P_{dc} for the OIP3 champion (**f**) and the OIP3/P_{dc} champion (**g**). The data shown in **b**–**f** were measured on a single aCNT-FET, specifically the device that exhibited the largest OIP3. **h**, The third-order-intercept point is derived by extrapolating the dBm P_{IMD3} point, which scales at 3:1 as defined in equation (5), to where it intersects the dBm P_{fund} line.

amplifiers utilizing CNT-FETs. The output 1 dB gain compression power level was −8.9 dBm for the OIP3 champion (Fig. 5b), giving a figure of merit OIP3/P_{1dB} = 26.5 dB, showing that aCNT-FETs compare well with the incumbent semiconductor technologies[22].

Aggregated results and outlook for aCNT-FETs

The figures of merit f_T, f_{max}, g_m, $I_{d,max}$ and f_T/g_m were extracted from aggregate data of the 107 devices with $L_g \sim 110$ nm and the 229 devices with $L_g \sim 140$ nm and plotted as histograms in Fig. 6. Despite the relative immaturity of the technology, the device results from these aCNT-FETs challenge the figures of merit of the incumbent technologies of GaAs pHEMT and RF-CMOS at similar gate lengths. For example, the top aCNT-FET devices fabricated here have already exceeded the benchmark f_T of 90 GHz for 100-nm-gate-length RF-CMOS devices (130 nm node)[24]. In the short term, we expect that the other figures of merit for the aCNT-FET technology will also exceed those of the incumbents on the basis of the resolution of known challenges such as utilizing longer CNTs, the passivation of charge-traps, a reduction in the source and drain resistances, and gate-dielectric optimization.

As an example, increasing the fraction of longer CNTs is expected to result in faster devices. For our CNT length distribution (mean = 603 nm, Supplementary Section 1) and the drain–source lengths explored in this work (ranging from 140 to 200 nm), only 30–40% of the CNTs in the channel are expected to completely span it with good contacts (meaning >50 nm of Pd–CNT contact-length overlap at each of the source and drain contacts[25,26], Supplementary Section 1). The CNTs that do not directly span the channel will either terminate within the channel as an open circuit or span via a percolation pathway, thereby introducing a large CNT–CNT contact resistance. These percolating or open-circuit CNTs will contribute little to g_m but will retain the same contribution to the gate capacitance, C_{gg}, thus negatively impacting f_T via the relationship $f_T \approx g_m/2\pi C_{gg}$. Having a larger proportion of longer CNTs will increase the fraction directly spanning and resulting in a decreased parasitic effect.

Further gains in device speed, notably f_{max}, will result from improving the devices' current saturation, as power gain depends on a decreased output conductance g_o. Under static d.c. bias as occurs during RF measurement and amplifier operation, saturation in these devices may be obscured by bias drift caused primarily by mobile surface and interfacial charge traps[27]. The charge-trap effects manifest in these devices as (1) hysteretic sweeps in V_{gs} and V_{ds} and (2) increased OFF-currents at both high biases and short channel lengths, as further explored in Supplementary Section 5. The Supplementary Information further discusses how saturation behaviour might be improved by using CNT films with longer length distributions, decreasing the access-region resistance, and by improving the array order of the CNTs in the film to reduce screening.

A comparative advantage of our aCNT-FETs over the incumbent technology, as evident in Fig. 6e, is their high f_T to g_m ratio, which

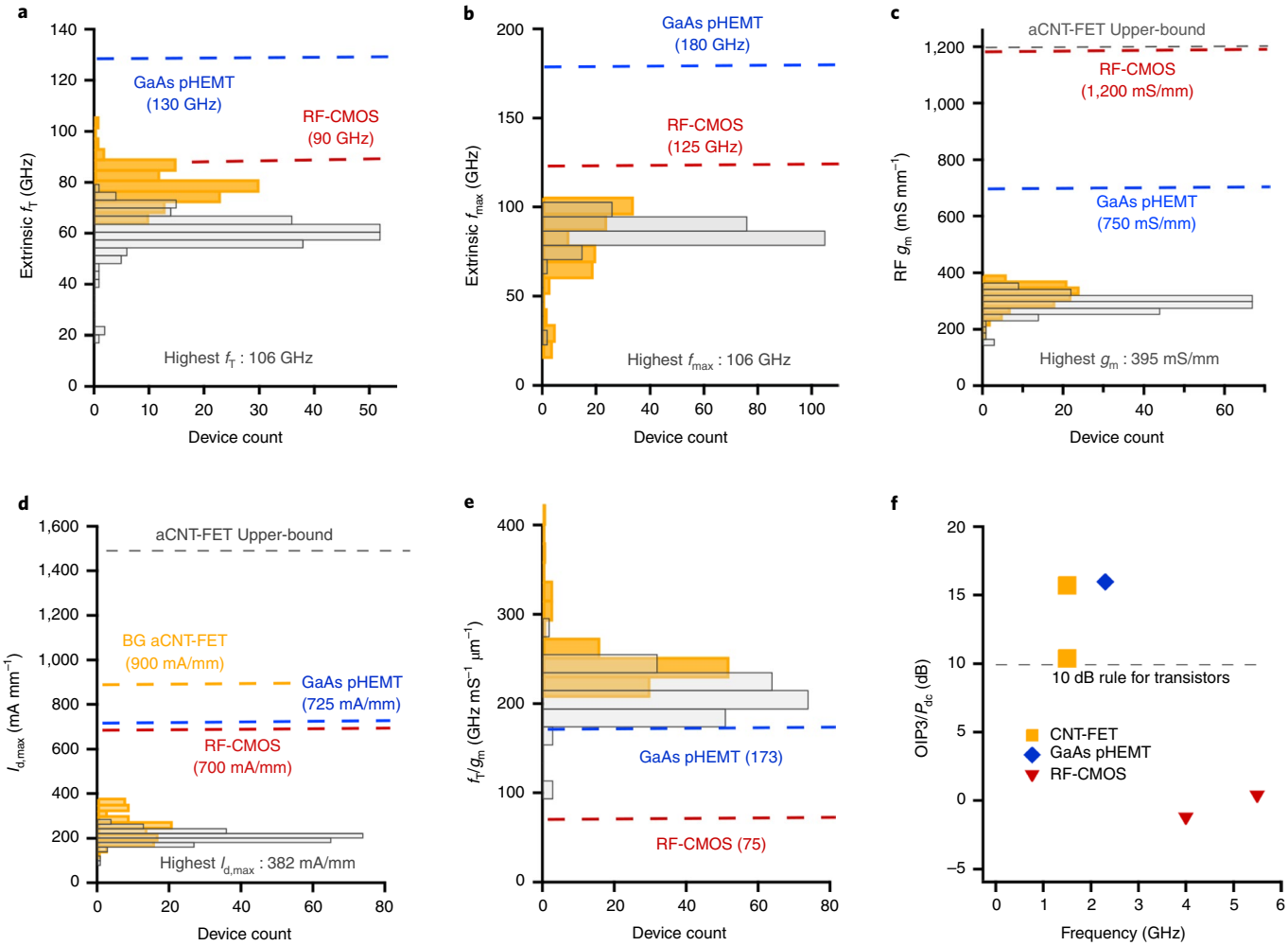

Fig. 6 | Benchmarking to incumbent RF technologies. Bars represent binned statistical data, and dashed lines indicate metrics or bounds from the literature. **a**–**e**, Aggregate data of 107 T-gate aCNT-FET devices with L_g ~ 110 nm (orange bars) and 229 devices with L_g ~ 140 nm (grey bars) displayed in histograms for different FET metrics: f_T (**a**), f_{max} (**b**), g_m (**c**), $I_{d,max}$ (**d**) and f_T/g_m (**e**). Holistically, the metrics demonstrate that aCNT-FET is challenging the incumbent technologies, RF-CMOS and GaAs pHEMT. Devices with comparable channel lengths were used for the incumbent technology benchmark comparison, specifically data from TSMC's 130 nm node RF-CMOS process (L_g = 100 nm)[24] and data from WIN Semiconductor's L_g = 100 nm GaAs pHEMT process[18]. Using single-CNT-device results, 25 μA (ref. [5]) and 20 μS (refs. [6–9]) per CNT, and scaling to 60 CNTs μm^{-1}, we place an approximate upper bound on possible aCNT-FET performance. **d** includes data from a back-gate (BG) aCNT-FET[21] with a similar CNT density, to highlight what is possible without access-region resistance. The high f_T per unit g_m multiple in **e** relative to the incumbent technology probably originates in part from the lower parasitic capacitance unique to aCNT-FETs. **f**, The low-frequency linearity ratio, OIP3/P_{dc}, shows aCNT-FET data surpassing the 10 dB rule of thumb (10.4 dB from this work and 15.7 dB from our previous work[22]), which is superior to that of RF-CMOS (without circuit-based linearization)[45,46], and on par with a commercial GaAs pHEMT (Qorvo QPL6202Q).

indicates a 1.5–3 times higher f_T value per unit of g_m over that of pHEMTs and RF-CMOS devices with comparable gate lengths. Since this ratio is proportional to the inverse of the total gate capacitance, $1/(C_{gg}+C_{gp})$, where C_{gp} is the gate parasitic capacitance, we attribute this intrinsic advantage to the lower parasitic capacitance of aCNT-FETs. The parasitic capacitances consist primarily of the fringing-field capacitances from the T-gate to the CNTs in the access region and to the source and drain electrodes. This fringing-field capacitance to the CNTs is smaller in aCNT-FET devices, because for geometric reasons fringing capacitance is smaller for the 1D cylinders such as CNTs than for 2D and 3D materials[28]. RF-CMOS devices are particularly disadvantaged by parasitic capacitance because their gates overlap with a portion of the highly doped source and drain silicon. The lower dielectric constant of 3.8 for SiO_2 versus 11.9 for $Al_xGa_{1-x}As$ and 11 for Si will also reduce parasitic capacitance for the fringe fields that traverse the substrate.

To give some perspective on what the technology may ultimately achieve, in Fig. 6c,d we include an estimated upper bound for aCNT-FET performance based on scaling up single-CNT-device results of 20 μS (refs. [6–9]) and 25 μA (ref. [5]) per CNT to that of a 60 CNTs μm^{-1} device. This results in a transconductance of 1,200 mS mm^{-1} and a current density of 1,500 mA mm^{-1}, which projects to an upper-bound f_T greater than 300 GHz for a 110-nm-gate-length device, assuming the same f_T/g_m ratio. These upper bounds, while optimistic, greatly exceed those of the incumbent technology and present a large target for technological growth, achievable by fundamental device improvements, beyond our results.

Conclusions

We have demonstrated a wafer-scalable approach for producing aligned CNT-FETs with the leading edge of the device's extrinsic f_T and f_{max} performance distribution exceeding 100 GHz and, within

the set of tested devices, linearity metrics OIP3 normalized to d.c. power and P_{1dB} both exceeding 10 dB. These capabilities, which challenge those of incumbent RF amplifier technology, are the result of the benefits of 1D materials—namely, reduced scattering, small parasitic capacitance and high linearity—and were achieved through refinements in CNT deposition and device processing. The next steps will be to further improve the linearity, as well as investigating noise characterization and optimization. Our results suggest that CNT-FET technology could ultimately offer both the high performance of GaAs pHEMTs and integration compatibility with CMOS.

Methods

Deposition of densely aligned high-semiconducting-purity CNTs. Single-walled, arc-discharge CNTs were sorted using the conjugated polymer poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-co-(6,6′-(2,2′-bipyridine))] (PFO–BPy) to form a high-semiconducting-purity single-walled CNT solution in toluene[13]. The CNTs were transferred into chloroform for the aligned deposition. Densely aligned, high-semiconducting-purity (>99.9% on the basis of optical purity), PFO–BPy polymer-sorted single-walled CNTs with linear densities of 40–60 CNTs μm^{-1} (inclusive of individual CNTs and bundles of ≥2 CNTs) were deposited, forming a monolayer over a 20 × 30 mm^2 area of the single-crystal quartz substrate. By introducing modifications to the floating evaporative self-assembly baseline process, as codeveloped by the Arnold and Gopalan Groups at the University of Wisconsin, Madison[16,29], a more continuous, uniformly aligned CNT film can be deposited: specifically, by reducing surface waves on the Langmuir–Blodgett trough's water subphase. These surface waves were substantially reduced, as evident from observing surface reflections of light sources, by (1) isolating the air-flow around the apparatus using a custom-built enclosure, (2) placing the trough on a vibration isolation air-table and (3) operating in a class 100/1,000 cleanroom and low-vibration (sub-basement) environment.

Fabrication of aCNT-FETs. CNT-based FETs were fabricated with the T-gate structure commonly used in III–V HEMT devices[18]. An ASML5500-200 *i*-line stepper was used to pattern the CNT area, coplanar waveguide and probe pads. Unwanted CNTs outside the device channel were etched with low-power O_2 plasma. Metallization of the coplanar waveguide layer was performed by e-beam evaporation of Ti/Au (50 nm/200 nm) for the drain and source wiring/pads and Ti/Au/Ni (50 nm/200 nm/10 nm) for the gate wiring/pad. Both the contact layer and T-gate were patterned by EBL, with the patterns written using a 100 keV Vistec EBPG 5000+ES with the contact pad formed from a bilayer polymethyl methacrylate process while the T-gate was patterned via a trilayer resist process. Metallized contact electrodes consisted of 35 nm of electron-beam-evaporated Pd while the T-gate metal stack was Al/Ni/Au (60 nm/30 nm/150 nm). The head of the T-gate had a dimension of ~250 nm. The Al_2O_3 dielectric was formed using the method[15,30–36] of oxidizing the Al gate by baking the wafer on a hot plate at 120 °C for 2.5 h. This temperature and duration ensure oxidation of the T-gate's underside. Ellipsometry measurements on a test sample determined that this process resulted in ~4.5 nm native Al_2O_3 thickness, which is within the expected range for Al surface oxides, which are known to self-terminate at 3–5 nm (ref. [36]).

Back-gated test wafers were fabricated on 50 nm thermal oxide Si wafers using a similar process except that the source/drain contacts were patterned by photolithography and had an L_{sd} = 400 nm.

Test and measurement. On-wafer measurements were performed on the aCNT-FETs using a semi-automated probe station (Cascade Summit 12000B-S), which can efficiently and automatically test thousands of devices. D.c. electrical characterization was performed using a semiconductor analyser (Keithley 4200). *S*-parameter data was taken using a 10 MHz–40 GHz Agilent PNA-series network analyser (E8363B) and calibrated to the probe tips using a standard short–open–load–thru calibration with an off-wafer precision standard.

Method of linearity, transconductance and compression measurements. Figure 5a illustrates the equipment setup used to measure OIP3 and employed to measure g_m, and 1 dB output compression (P_{1dB}). This test sweeps V_{gs} at 1 kHz in a triangle wave to obtain characteristics free from charge-trapping effects. I_d was measured via a differential amplifier and oscilloscope measuring the voltage drop across R_{dd} = 1.8 Ω. The I_d measurement was calibrated using a known d.c. current through R_{dd} while measuring the d.c. voltage produced by the differential amplifier. Oscilloscope readings were calibrated to accurately measure $V_{gs}(t)$ and $I_d(t)$, while the spectrum analyser data were calibrated to measure the RF output power levels as functions of time. A triangle-wave signal generator was used to both trigger the oscilloscope and spectrum analyser as well as driving the aCNT-FET gate.

The spectrum analyser is first tuned to selected RF signals (fundamentals) and third-order distortion products (IMD3) then subsequently set to the zero-span mode to capture both output fundamental power levels, $P_{out,fund}(t)$, and the upper and lower third-order distortion product RF power levels ($P_{IMD3,lower}(t)$ and $P_{IMD3,upper}(t)$). The swept gate voltage $V_{gs}(t)$ is then used with the spectrum analyser measurements to produce $P_{out,fund}(V_{gs})$ parametrically, along with the respective upper- and lower-frequency output IMD3 products $P_{IMD3,lower}(V_{gs})$ and $P_{IMD3,upper}(V_{gs})$. The IMD3 products are the third-order distortion products generated from the two-tone fundamentals via nonlinearities in the aCNT-FET under test.

RF transconductance and output conductance from *S*-parameters. *S*-parameters were also measured for V_{ds} = −1.5 V at stepped points of V_{gs} to yield RF $g_m(V_{gs})$, which is the primary version of the transconductance quoted in the text, as well as RF $g_o(V_{gs})$ for purposes of calculating the self-gain. Simultaneously, the drain current was monitored during the *S*-parameter measurements to yield the transfer curve, static $I_d(V_{gs})$. V_{gs} was set and I_d was allowed to stabilize over 10 s measurement intervals until I_d drift was below 1% between measurement intervals. Next, *S*-parameters were measured from 1 GHz to 1.6 GHz and the *S*-parameter measurement was repeated until stable, that is until the change of $|S_{21}|$ was less than 0.2 dB between measurements at any frequency. After this *S*-parameter stabilization step the *S*-parameters and corresponding static I_d were recorded for each V_{gs} setting. V_{gs} was then set at the next point and the static I_d and *S*-parameter measurements repeated as above for all V_{gs} points selected. The stabilization steps served to reduce effects of drift from the charge-trapping effects. The RF $g_m(V_{gs})$ data were then derived from the measured *S*-parameters and are compared in Supplementary Information with $g_{me}(V_{gs})$ from the RF output power measurements discussed below.

***V*$_{gs}$ swept RF transconductance and transfer curve measurement method.** The test setup of Fig. 5a was also used to obtain $g_{me}(V_{gs})$ from the spectrum analyser RF power measurements and the parametric transfer curve $I_d(V_{gs}(t))$ from the oscilloscope measurements. This test is similar to that used for the OIP3 except that one of the RF sources is turned off and the other is tuned to 1,500 MHz. Incident RF power applied to the gate, P_{in}, is set to a constant −14 dBm, which is low enough not to reduce the device gains. Again, the aCNT-FET gate is driven by both the RF signal and the 1 kHz triangle wave, $V_{gs}(t)$. $P_{out}(t)$ was measured via the spectrum analyser and calibrated to remove losses of the RF tuner and cables. The RF $i_d(t)$ was derived from $P_{out}(t)$ and z_L via

$$i_d(t) = \sqrt{\frac{P_{out}(t)}{\mathrm{real}(z_L)}} \tag{1}$$

Assuming that the aCNT-FETs present an open circuit at their gates,

$$v_{gs} = 2\sqrt{Z_0 P_{in}} \tag{2}$$

where Z_0 = 50 Ω is the system characteristic impedance. Therefore,

$$g_{me}(t) = \frac{1}{2}\sqrt{\frac{P_{out}(t)}{\mathrm{real}(z_L) Z_0 P_{in}}} \tag{3}$$

and since $V_{gs}(t)$ was measured

$$g_{me}(V_{gs}) = \frac{1}{2}\sqrt{\frac{P_{out}(V_{gs})}{\mathrm{real}(z_L) Z_0 P_{in}}} \tag{4}$$

The transfer curve was extracted parametrically via the oscilloscope as before as $I_d(V_{gs}(t))$ from the $I_d(t)$ and $V_{gs}(t)$ measurements.

OIP3 measurement method. In general, semiconductor device metrics such as OIP3 and P_{1dB} depend on z_L and the corresponding reflection coefficient, Γ_L. The RF tuner (Fig. 5a) is tuned to find the Γ_L that maximizes the peak value of OIP3(V_{gs}). The 1 kHz sweep of V_{gs} eliminates the need for a slow, simultaneous, two-dimensional search in V_{gs} and Γ_L. The value of Γ_L that maximizes the peak OIP3(V_{gs}) is Γ_{Lopt3}, which was determined for a few aCNT-FETs and then assumed to be near optimum, for the rest of the measurements of aCNT-FETs having similar gate widths, to measure OIP3(V_{gs}).

The gate is driven with a two-tone RF signal—that is, the two fundamentals, set to both have equal P_{in} at 1,498 MHz and 1,502 MHz for lower and upper tones respectively. P_{in} is set using the power sensor. The upper- and lower-frequency third-order RF distortion products appear at 1,494 MHz and 1,506 MHz and their powers are measured as P_{IMD3L} and P_{IMD3U} respectively at the output of the device under test. Ideally $P_{IMD3L} = P_{IMD3U}$, but in real devices these can differ by several decibels due to the simultaneous presence of AM to AM and AM to PM distortion effects[28]. Therefore, $OIP3_U$ (upper OIP3) and $OIP3_L$ (lower OIP3) are derived from P_{IMD3L} and P_{IMD3U} respectively, and the quoted OIP3 is the lower of $OIP3_U$ and $OIP3_L$. Distortion measurements here have been made at a single P_{in} = −14 dBm and the OIP3 is calculated via

$$OIP3_x = \frac{3P_{fund} - P_{IMD3x}}{2} \tag{5}$$

where P_{fund} is the output RF power of the device under test at each fundamental frequency, the above are in dBm and x is L or U. Moreover, P_{fund}, P_{IMD3x} and I_d are measured as functions of time during the swept V_{gs} OIP3 measurements, therefore allowing us to parametrically relate P_{fund}, P_{IMD3x}, I_d and OIP3 to V_{gs}. Note that equation (5) assumes that, on a dB scale, P_{IMD3x} versus P_{in} has a 3:1 slope while the P_{fund} versus P_{in} slope is 1:1. From these, $P_{dc}(V_{gs})$, OIP3(V_{gs}), $I_d(V_{gs})$ and the ratio (OIP3/P_{dc})(V_{gs}) are all calculated where $P_{dc}(V_{gs}) = V_{ds}I_d(V_{gs})$ and V_{ds} is constant at −1.5 V during the measurements.

One decibel gain compression point method. $P_{1dB}(V_{gs})$ was measured, using the setup in Fig. 5a, in a manner similar to that for OIP3(V_{gs}) except that just one RF source at 1,500 MHz drove the CNT-FET gate and P_{in} was measured via the RF power meter. P_{in} was stepped and $P_{out}(t)$ was measured via the spectrum analyser, enabling calculation of the gain, $\text{gain}(t) = \frac{P_{out}(t)}{P_{in}}$. The measurement of $V_{gs}(t)$ allows parameterization of $P_{out}(P_{in}, V_{gs})$ and gain(P_{in}, V_{gs}), which are not confounded by trap-caused hysteresis effects. The 1 dB compression point itself, $P_{1dB}(V_{gs})$, for all swept points of V_{gs}, was then calculated from $P_{out}(P_{in}, V_{gs})$ and gain(P_{in}, V_{gs}) by locating the P_{in} that reduces gain(P_{in}, V_{gs}), by 1 dB. Here, the V_{gs} point of interest is that close to the V_{gs} point that maximizes the peak OIP3(V_{gs}) and is defined as V_{gs3opt}. During the P_{1dB} measurements, the tuner was set to provide an RF load reflection coefficient of Γ_{Lopt3}, that is, that which maximized the OIP3 of the CNT-FET under test. Therefore, $P_{out}(P_{in}, V_{gs3opt})$ is reported in Fig. 5b as a function of P_{in}.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author on reasonable request.

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Author contributions

C.R., A.A.K. and T.A.C. performed device fabrication. Analysis of the data was performed by A.A.K., P.F.M., C.R. and T.A.C. Electrical measurements were performed by P.F.M.

Device simulation was performed by P.F.M., A.A.K. and B.I.H. Writing of the manuscript was performed by C.R., A.A.K., P.F.M. and T.A.C.. Technology development management and strategic technical planning were performed by C.R., K.G., C.Z. and M.R.A.

Competing interests

The authors declare the following competing financial interest: C.R., A.A.K., P.F.M., T.A.C. and K.G. are employees of Carbonics Inc., a startup company focused on commercializing CNT transistors for microwave and millimetre-wave applications. C.Z. is a co-founder and shareholder of Carbonics Inc.

Additional information

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