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ARTICLE

Aligned Carbon Nanotube Synaptic Transistors for Large-Scale Neuromorphic Computing

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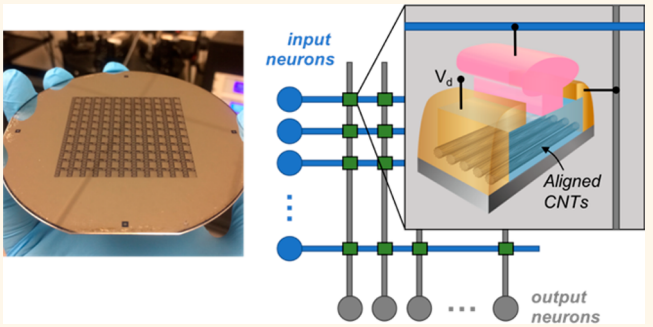
ABSTRACT: **This paper presents aligned carbon nanotube (CNT) synaptic transistors for large-scale neuromorphic computing systems. The synaptic behavior of these devices is achieved *via* charge-trapping effects, commonly observed in carbon-based nanoelectronics. In this work, charge trapping in the high-*k* dielectric layer of top-gated CNT field-effect transistors (FETs) enables the gradual analog programmability of the CNT channel conductance with a large dynamic range (*i.e.*, large on/off ratio). Aligned CNT synaptic devices present significant improvements over conventional memristor technologies (*e.g.*, RRAM), which suffer from abrupt transitions in the conductance modulation and/or a small dynamic range. Here, we demonstrate exceptional uniformity of aligned CNT FET synaptic behavior, as well as significant robustness and nonvolatility *via* pulsed experiments, establishing their suitability for neural network implementations. Additionally, this technology is based on a wafer-level technique for constructing highly aligned arrays of CNTs with high semiconducting purity and is fully CMOS compatible, ensuring the practicality of large-scale CNT+CMOS neuromorphic systems. We also demonstrate fine-tunability of the aligned CNT synaptic behavior and discuss its application to adaptive online learning schemes and to homeostatic regulation of artificial neuron firing rates. We simulate the implementation of unsupervised learning for pattern recognition using a spike-timing-dependent-plasticity scheme, indicate system-level performance (as indicated by the recognition accuracy), and demonstrate improvements in the learning rate resulting from tuning the synaptic characteristics of aligned CNT devices.**



KEYWORDS: *carbon nanotube, synapse, transistor, neuromorphic, machine learning*

The approaching fundamental limits for process scaling of complementary metal-oxide-semiconductor (CMOS) technology have led to significant material and device research aimed at developing a more efficient and better performing replacement for MOS field-effect-transistors (MOSFETs).[1−4] Low-dimensional (*e.g.*, 2-D and 1-D) materials such as graphene and carbon nanotubes (CNTs) are promising candidates with excellent scalability and desirable electronic transport properties under low-voltage operation.[5−9] Moreover, recent developments in the functionality of CNT devices,[10−13] as well as their compatibility with three-dimensional (3-D) integration,[14,15] may enable the implementation of non-von-Neumann architectures that eliminate the separation of memory and logic, thus reducing power consumption and heat generation resulting from expensive data transferring (*i.e.*, the von-Neumann "bottleneck").[16,17] The time- and power-efficient computing benefits of these architectures are especially beneficial for low-power mobile electronic systems. Moreover, the increasing deployment of mobile, data-gathering devices for the Internet of Things (IoT) presents a significant need for efficient and high-throughput data preprocessing at the edge of the network (*i.e.*, edge computing).[18,19]

Neuromorphic architectures, inspired by the human brain, emulate the structure and functionality of biological neural systems and can enable the realization of highly efficient computing systems.[20,21] By utilizing the synaptic properties of resistive switching (*i.e.*, memristive) devices, artificial neural networks can be fabricated in a crossbar configuration offering the desired density, parallelism, and 3-D integration compat-

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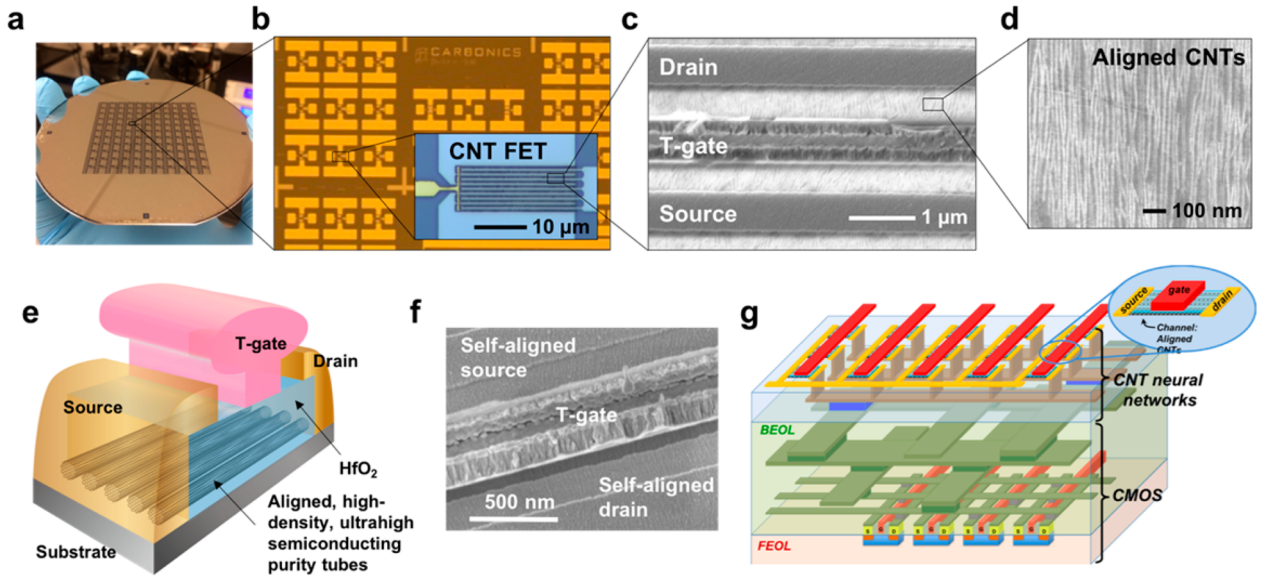

Figure 1. (a) Aligned CNT FET wafer fabricated by Carbonics. (b) Top-gated aligned CNT FET test structures (inset is the zoomed-in view of the channel region from a 10-finger device; each channel "finger" is 20 μm wide). (c) Scanning electron microscope (SEM) image of the aligned CNT FET active region. (d) SEM of the aligned CNT channel. (e) Cross-sectional schematic of the aligned CNT FET. (f) Top view of the aligned CNT FET including t-shaped top-gate and self-aligned source/drain regions. (g) Conceptual back-end-of-line (BEOL) integration of aligned CNT FETs for artificial neural network implementation in crossbar configuration.

ibility desired for the efficient hardware implementation of machine learning algorithms and neuro-inspired computing architectures.[22−24] This approach has been used to demonstrate tasks such as recognition, classification, learning, and decision making.[18,25−28]

The most widely studied memristive device for the hardware implementation of artificial neural networks in a crossbar configuration is the filamentary type (*e.g.*, RRAM).[29−33] This technology offers great features including a simple two-terminal structure, low-power operation, and good endurance and retention.[33] However, it suffers from significant device-to-device and cycle-to-cycle variability,[34] as well as from abruptness of resistance modulation,[35−38] due to the inherent filamentary operation.[39] This abruptness is undesirable for neuromorphic systems[40] and can be eliminated from the characterization of RRAM synaptic behavior through the application of a forming step (*i.e.*, initial generation of the conductive filament). Nonetheless, the dynamic range (*i.e.*, resistance modulation range) after the formation of the conductive filament is limited, as further changes in resistance result only from modulation of the filament cross-sectional area.[41] Moreover, the requirement of a forming step and the significant variation of the forming/set voltage[42,43] introduce additional system-level complexity (and associated cost), unwanted for the efficient hardware implementation of artificial neural networks. Because of these limitations, synaptic devices with alternative resistive switching mechanisms are desirable. Recently, charge-trapping synaptic transistors have been proposed as an alternative for the hardware implementation of artificial neural networks. Devices with Si[44] as well as random network CNT channels[11,12] have been demonstrated with promising preliminary results. It is well established that CNT-based devices have exceptional scaling properties that extend beyond the Si roadmap[8] and are considered a primary candidate for next-generation computing systems that vertically integrate logic and memory.[15,45] Importantly, achieving superior device uniformity and stability requires controlled placement of CNTs (*i.e.*, alignment) as well as controlled semiconducting purity.[46] In this work, we present a wafer-scale aligned CNT synaptic transistor technology for large-scale neuromorphic systems. An advantage of CNTs for the development of charge-trapping synaptic transistors is their large sensitivity to charged defect scattering. Because of their small physical dimensions, CNT conductivity can change significantly as a result of changes in the charge state of nearby defects.[47,48] As we will show, the sensitivity of individual CNTs translates into measurable changes of CNT FET conductance, especially for FETs with aligned CNTs where transport and scattering effects are isolated to 1-D,[49] resulting in a robust synaptic behavior with large dynamic range. We present a thorough analysis of the robust synaptic behavior in aligned CNT transistors based on DC and pulsed electrical characterization. We discuss the implementation of aligned CNT-based artificial neural networks and present system-level simulations of unsupervised learning for pattern recognition applications. Additionally, we demonstrate the synaptic tuning capability of an aligned CNT FET and discuss its application to adaptive learning schemes for artificial neural networks and/or to implement homeostatic regulation of neuron firing rates.

RESULTS AND DISCUSSION

Aligned CNT Synaptic Transistors. Single-walled carbon nanotubes (SWCNTs) and SWCNT FETs have exceptional 1-D electronic transport properties, making them an excellent candidate for various applications including high-speed logic devices,[50] radio frequency (RF) transistors,[51] and nonvolatile memory.[52] However, for most of these applications, the organized assembly (*i.e.*, alignment) of SWCNTs with controlled semiconducting purity is critical for optimizing device performance and for developing practical, reliable, and scalable technologies.[46,53−55] In this work, a recently improved evaporation-driven process, named floating evaporative self-assembly (FESA),[56,57] has been utilized by Carbonics Inc. to fabricate highly aligned SWCNT devices at the wafer level

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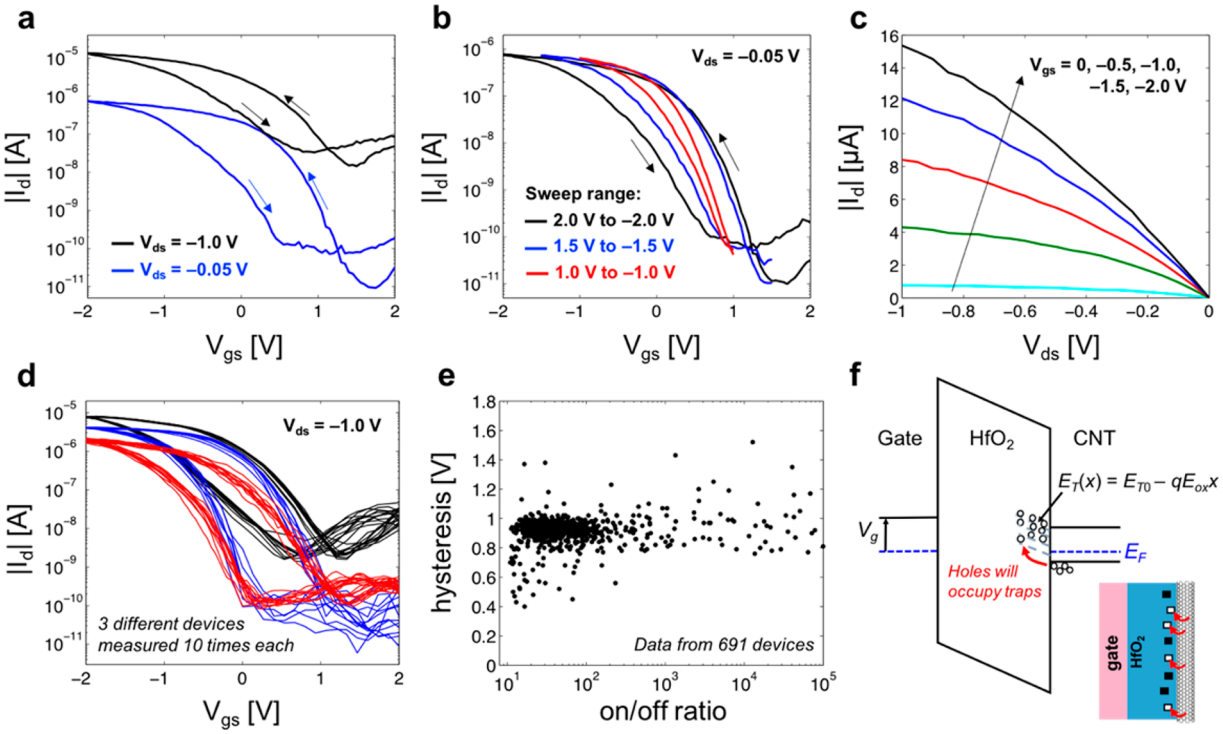

Figure 2. (a) Dual-sweep I_d–V_{gs} characteristics of aligned CNT FETs for V_{ds} = −1.0 and −0.05 V revealing large gate hysteresis. (b) Dependence of hysteresis window on the voltage sweep range of dual-sweep I_d–V_{gs} measurements. (c) I_d–V_{ds} characteristics for increasing V_{gs}. (d) Multiple cycles of dual-sweep I_d–V_{gs} indicating repeatability of hysteresis effects. (e) Distribution of hysteresis plotted as a function of the on/off ratio. (f) Energy band diagram illustrating charge-trapping effects in aligned CNT FETs.

(Figure 1a). Figure 1b is the optical image of a multifingered top-gated aligned CNT FET. The scanning electron microscope (SEM) images of a gate region and of the aligned SWCNTs are respectively shown in Figure 1c and d. A schematic of the self-aligned T-gate transistor structure is illustrated in Figure 1e, and the SEM image of the finalized device including self-aligned source/drain regions is shown in Figure 1f. The T-gate structure is characteristic of RF application that these devices were initially designed for. It enhances gate control, helps scaling down the channel length, and reduces parasitic capacitance.[58] Thus, it can enhance the dynamic behavior of gate-bias-dependent charge-trapping mechanisms and improve the performance of aligned CNT synaptic transistors, enabling faster operation.

This wafer-level process is fully compatible with CMOS, owing to the low-temperature fabrication of aligned CNT devices. Thus, it is feasible to achieve 3-D integration of aligned CNT devices and CMOS circuits to enable non-von-Neumann architectures, such as neuromorphic topologies, that conquer the communication bottleneck between memory and logic. Figure 1g illustrates the conceptual back-end-of-line (BEOL) 3-D integration of aligned CNT and CMOS for neuromorphic computing systems. In this architecture, aligned CNT FETs are connected in a crossbar configuration and operate as the synaptic elements of an artificial neural network, and neural circuits are implemented with CMOS. We first present the electrical characteristics of the aligned CNT FETs, followed by the demonstration and analysis of their synaptic properties. Later, we describe the aligned CNT-based neuromorphic crossbar configuration as well as the implementation and performance of artificial spiking neural networks for pattern recognition based on unsupervised learning.

Figure 2a plots the drain current (I_d) as a function of the gate-to-source voltage (V_{gs}) for a drain bias (V_d) of −1.0 V and −50 mV from a CNT FET with a channel width to length ratio of $W/L \approx 60\ \mu m/1\ \mu m$. These data are from a six-finger top-gated CNT FET with 20 μm channel width per finger (only measured three of the six channels divided between two drain electrodes for a total of 60 μm). P-type operation in the CNT FET is indicated by the exponentially increasing (negative) current with increasing $-V_{gs}$, resulting from hole conduction in the valence band of the CNTs. The dual sweeps in Figure 2a also indicate large counterclockwise gate hysteresis attributed to a dynamic screening of the electric field due to charge injection/emission (*i.e.*, trapping/detrapping) near and/or at the interface between the CNTs and the 4.6 nm thick HfO_2 gate dielectric. Figure 2b plots the dual-sweep transfer characteristics with V_d = −0.05 V, measured with increasing gate sweep range from ±0.5 to ±2.0 V. Increasing the gate sweep range allows accessing a wider range of energetically distributed traps and enhances the field-driven tunneling mechanisms that allow charge trapping/detrapping.[59] As discussed below, this voltage control of trap occupancy allows gradually modulating charge-induced electrostatic and scattering effects, resulting in a robust synaptic device operation. For completion, in Figure 2c we plot the family of I_d–V_{ds} curves obtained with increasing V_{gs} from 0 V to −1.0 V in steps of −0.5 V.

We plot multiple cycles of dual-sweep I_d–V_{gs} measurements from three different devices in Figure 2d, to demonstrate the repeatability of the charge-trapping effects and their impact on the hysteresis and electrical characteristics of the CNT FETs. Having a sufficiently large on/off ratio is important for achieving synaptic operation with a large dynamic range (*i.e.*, a large range of conductance modulation). We experimentally

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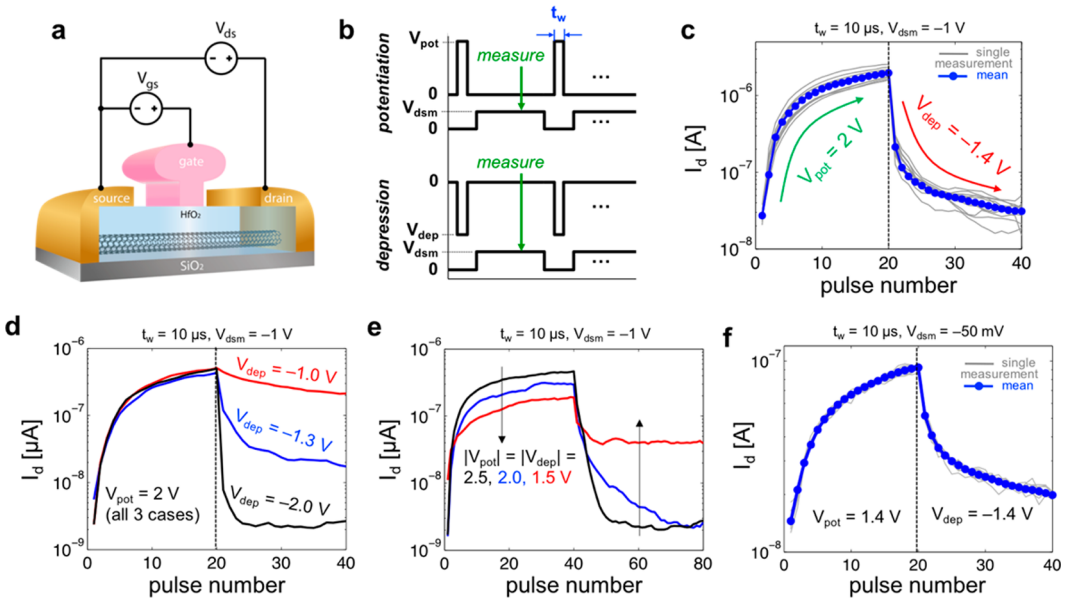

Figure 3. (a) Biasing configuration for pulsed measurements of synaptic properties of aligned CNT FETs. (b) Diagram of the pulsed measurements for long-term potentiation and long-term depression. (c) Measured synaptic characteristics of an aligned CNT FET. (d, e) Tuning the synaptic properties of aligned CNT FETs with adjustment of the potentiating/depressing voltage pulse amplitudes. (f) Reduced pulse amplitude improves linearity and stability of the synaptic response with a slight reduction in dynamic range.

verify that the aligned top-gate CNT FETs can simultaneously provide a sufficiently large on/off ratio (*e.g.*, >10) and hysteresis window (*e.g.*, >0.4 V) by extracting these parameters from a large set of 691 measured devices. In Figure 2e we plot the distribution, and it concentrates around an on/off ratio of ∼40 and a hysteresis window of ∼0.9 V, with a long tail spreading to larger on/off ratios. The tightness of the hysteresis window distribution is a good indicator of uniformity in the charge-trapping dynamics. In short-channel CNT FETs, electronic transport is quasi-ballistic (near-ballistic).[60] This also helps achieve a robust synaptic behavior and large dynamic range, as it enhances the sensitivity of CNT FET conductance to charged defects near the channel. When carriers can travel without being scattered by other channel impurities, Coulomb scattering induced by changes in the charge state of nearby defects can have a large impact on conductance.[47]

In Figure 2f, the energy band diagram across the gate/HfO_2/CNT regions of the device illustrates the trapping mechanisms responsible for hysteresis and for the synaptic behavior of the aligned CNT transistors. With a negative bias applied at the gate, the energy level of near-interfacial traps in the HfO_2 dielectric layer will be shifted upward (due to band bending), and a fraction of them that were initially located below the Fermi level in the CNT channel (E_F) will now be located above E_F. These traps will gradually change their occupancy, since at this biasing condition there is a large hole population in the CNT channel that can occupy the energy levels E_T (*i.e.*, hole trapping), resulting in a net positive change in the charge contribution due to traps. Similarly, when the gate bias is positive, the bands bend in the opposite direction, resulting in a net negative change in the trap charge contribution. We note that the trap energy distribution (relative to E_F) depends on bias (*i.e.*, due to band bending) as well as position. Traps located further away from the interface see a larger shift in their energy level as a function of bias, but are also less likely to have a chance in their occupancy, as the tunneling probability of carriers from the CNT channel decreases exponentially with distance from the interface.[59] Thus, only a fraction of near-interfacial traps having energy levels centered around E_F, will dynamically change their charged state as a function of bias, and affect the electrostatic and transport properties of the device. In CNT FETs, traps along the surface of the dielectric but not directly in contact with the CNT (*i.e.*, surface traps) may also contribute to charging effects.[61] The trap charge state transitions are not instantaneous and can have long-term effects that result in gate hysteresis and memory effects that are responsible for the synaptic behavior of the aligned CNT FETs.

Synaptic Properties of Aligned CNT FETs. The synaptic properties of the aligned CNT FETs are experimentally analyzed using pulsed electrical measurements. As illustrated in Figure 3a, the source terminal of the aligned CNT FETs is connected to a ground reference, while a series of gate-to-source (V_{gs}) and drain-to-source (V_{ds}) voltage pulses are applied to the device under test during the experiment. To characterize synaptic potentiation, a short *positive* V_{gs} pulse with amplitude V_{pot} and width t_w is applied as indicated in Figure 3b. Following the application of the $V_{gs} = V_{pot}$ pulse, a small bias of V_{dsm} is applied between drain and source to measure I_d (at V_{gs} = 0 V), and the process is repeated for a specified number of potentiating pulses. Similarly, synaptic depression is characterized by applying a short *negative* gate-to-source voltage pulse with amplitude V_{dep} and width t_w, followed by a small V_{dsm} bias to measure I_d.

In Figure 3c we plot the synaptic characteristics of an aligned CNT FET measured with 20 potentiating and 20 depressing voltage pulses having amplitudes V_{pot} = 2 V and V_{dep} = −1.4 V, respectively, and t_w = 10 μs. For the measurements of I_d, V_{dsm} = −1.0 V was applied for ∼0.1 s. The same device is measured 10 times (gray solid lines), and the mean is extracted (solid blue line with circles). The results in Figure 3c reveal good repeatability of the synaptic characteristics, a large dynamic range evident by >1 order of magnitude modulation of I_d, and

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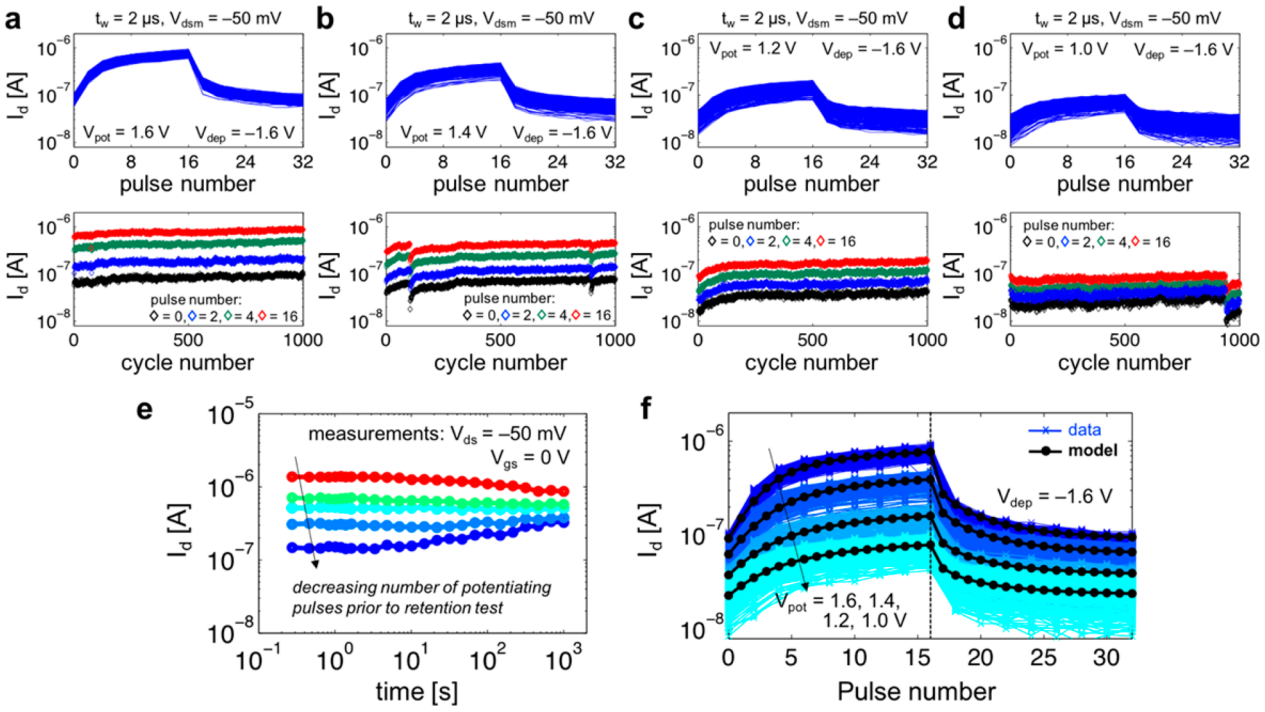

Figure 4. (a−d) Multiple cycles of synaptic properties characterized with repeated (1000) pulsed measurements. Each graph is for a different amplitude of the potentiating voltage pulse ranging from V_{pot} = 1.6 to 1.0 V. Top: I_d *vs* pulse number for all 1000 cycles; bottom: extraction of I_d at four different levels (*i.e.*, after four different number of pulses) *vs* cycle number. (e) Retention test showing samples of the programmed I_d as a function of time immediately following the pulsed programming. (f) Collection of all data from (a)−(d) and model calculations indicating the impact of V_{pot} on the abruptness and dynamic range of the aligned CNT FET conductance modulation.

good analog programmability (*i.e.*, fine synaptic resolution). We note that each potentiating and depressing pulse is of the same amplitude and width, since previous works have used pulse trains with incremental amplitudes and/or widths to improve the synaptic response.[62,63] However, it is not clear how these incremental pre/post-synaptic pulse features can be practically implemented in neuromorphic systems. Compared to these previous works, which are mostly based on filamentary resistive-switching devices (*e.g.*, RRAM), the aligned CNT devices have improved synaptic properties due to the inherent charge-trapping mechanisms responsible for conductance modulation. Filamentary devices generally exhibit an abrupt transition in conductance through a "forming step", during which the creation of the conductive filament is initiated. Following the creation of the conductive filamentary path, only small changes in conductance attributed to the widening of the filament are typically achieved, resulting in a limited dynamic range. In recent work,[11] it was determined that conductance modulation of ∼100% in random network CNT FETs enables better performing neuromorphic system operation, compared to conventional memristors, which typically achieve <30%. Also, that CNT devices with higher semiconducting purity and isolated nanotubes may provide improvements in synaptic performance. Here, we demonstrate that in aligned CNT FETs, where transport is isolated to individual nanotubes with high semiconducting purity, we can achieve >1 order of magnitude conductance modulation, providing significant improvement over random network CNT FETs.

Charge trapping in aligned CNT FETs not only eliminates the need for a forming step but also enables gradual changes in the conductance, resulting in a robust and stable synaptic response. However, in some cases we can still observe a sharp transition after the first depressing pulse (*e.g.*, Figure 3c). In order to eliminate this abruptness, we explore tuning of the synaptic characteristics through adjustment of the pulse amplitudes. In Figure 3d, we show independent tuning of synaptic depression based on measurements with a fixed V_{pot} = 2 V and V_{dep} = −2.0, − 1.3, and −1.0 V (same device). We note that adjusting only V_{dep} results in asymmetric synaptic characteristics. It is not yet clear how this asymmetry may affect the implementation of specific neuromorphic systems or machine learning algorithms. Nevertheless, it is possible to avoid the asymmetry by simultaneously adjusting V_{pot} and V_{dep}, with a slight trade-off in dynamic range as shown in Figure 3e. Figure 3f shows the synaptic characteristics from 10 repeated measurements (gray lines) of the same device using V_{pot} = 1.4 V and V_{dep} = −1.4 V as well as the mean (solid blue line with circles). The results in Figure 3f reveal better linearity (less abruptness) in conductance modulation while maintaining a large (∼1 order of magnitude) dynamic range.

To further explore the endurance, robustness, and tuning of the synaptic properties of aligned CNT FETs, we tested a large number of potentiation/depression cycles in a single device. In Figure 4a (top) we plot I_d measurements from 1000 consecutive synaptic characterization cycles using V_{pot} = 1.6 V, V_{dep} = −1.6 V, t_w = 2 μs, and V_{dsm} = −50 mV. From each cycle we extract I_d after 0, 2, 4, and 16 potentiating pulses and plot them as a function of the cycle number (bottom). The results in Figure 4a illustrate the endurance and robustness of the charge-trapping-based synaptic behavior of aligned CNT FETs. For the same device, we repeat the measurement of 1000 consecutive cycles with V_{pot} = 1.4, 1.2, and 1.0 V, using V_{dep} = −1.6 V for all cases, as plotted in Figure 4b,c,d (top). Similarly, we plot the extractions of I_d after 0, 2, 4, and 16

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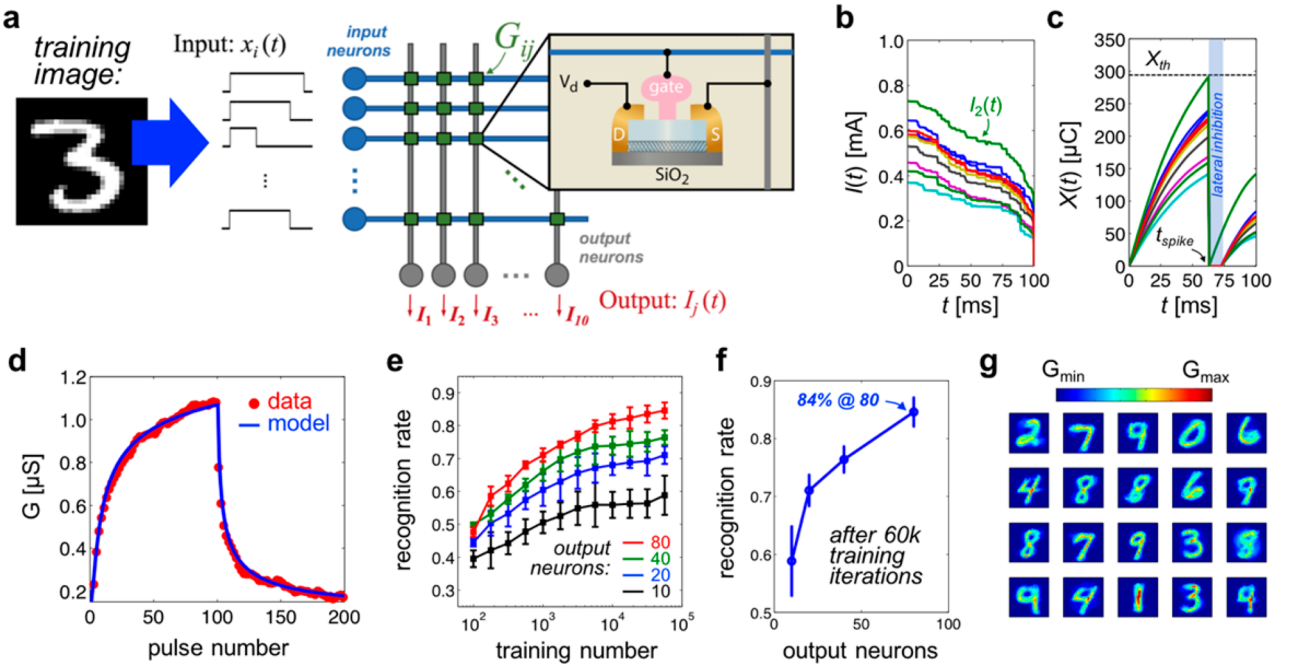

Figure 5. (a) Diagram illustrating the implementation of unsupervised learning for pattern recognition in a spiking neural network with aligned CNT synaptic devices. (b) Simulated time-dependent current in the postsynaptic (output) neurons. (c) Characteristics of output neuron potentials as simulated by an integrate and fire function, indicating the firing of the postsynaptic neuron spike as well as lateral inhibition. (d) Experimental data and model calculations of aligned CNT FET synaptic response used in the simulations of MNIST data set pattern recognition. (e) Recognition rate as a function of training number for arrays with increasing number of output neurons. (f) Recognition rate after 60 000 training cycles as a function of the number of output neurons. (g) Conductance map of 20 output neurons after training.

potentiating pulses for all cases, respectively plotted as a function of the cycle number in Figure 4b,c,d (bottom). These results verify the stability and robustness of the synaptic performance of aligned CNT FETs, as well as the precise tuning capability based on adjusting the potentiating voltage pulse amplitude.

We also verify the long-term retention of synaptic weights in aligned CNT FETs through the time-dependent sampling of I_d following the programming of various states (*i.e.*, after various numbers of potentiating/depressing pulses). Figure 4e plots I_d *vs* time over approximately 4 decades of time (up to 1 ks), indicating only a small loss of the extreme states that correspond to the largest/smallest programmed channel conductance. However, in many neuromorphic computing applications and machine learning algorithm implementations, synaptic weight updating may occur at much faster rates compared to the time scale over which we measure this slight degradation in retention. Moreover, even with this reduction to the window of allowed programmed states, the dynamic range is still sufficiently large (~3×) to enable adequate synaptic weight analog programmability with high resolution. Nonetheless, we expect that this issue may be easily resolved with engineering of the high-*k* dielectric trapping layer and/or introduction of alternative layers with better trapping characteristics.

Finally, in Figure 4f we show a combined plot with all 1000 cycles from each case of V_{pot} (*i.e.*, 1.6, 1.4, 1.2, 1.0 V), to better illustrate the repeatability of the measurements and to clearly indicate the impact V_{pot} on the synaptic response. As shown, a higher V_{pot} results in a larger dynamic range, but also increases the abruptness of the pulse-induced conductance modulation (*i.e.*, conductance is changed more with each pulse). In Figure 4f the color-coded solid lines are experimental data and the solid black lines with circles are calculations based on a recursive model for the aligned CNT FET synaptic characteristics. In the following section we provide more details on the model and describe the impact of conductance modulation abruptness and dynamic range on the unsupervised learning pattern recognition function of spiking neural networks.

Unsupervised Learning with Aligned CNT+CMOS Neuromorphic Systems. Synaptic devices such as the charge-trapping aligned CNT FETs are of great interest for the hardware implementation of large-scale neural networks for neuromorphic computing systems. A popular demonstration of the type of functions that can be efficiently implemented on neuromorphic systems is that of pattern recognition based on unsupervised learning in artificial spiking neural networks. Here, we present simulations of pattern recognition using the MNIST handwritten digit data set based on a simplified spike-timing-dependent plasticity scheme modeled on large arrays of aligned CNT synaptic transistors.[64] We utilize an experimentally verified model of the synaptic characteristics of aligned CNT FETs and investigate the impact of the conductance modulation abruptness and dynamic range on recognition rate and on the learning dynamics of the network.

The implementation is illustrated in Figure 5a: The data set consists of 60 000 training images and 10 000 test images. The training images are presented to the network as input voltage pulses which are applied at the rows of the implemented crossbar array architecture. Here, the input vector represents the intensity of all 28 × 28 pixels from the training image, translated into voltage pulses having a width directly proportional to the intensity of the corresponding pixel. At each cross point of the array, the gate of an aligned CNT

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synaptic transistor is connected to the input row (presynaptic neuron), and the source is connected to the output column (postsynaptic neuron). The drain is biased to a small negative voltage with respect to the source, to enable current flow in the channel of the aligned CNT FETs. The sum of the currents flowing through all of the synaptic devices connected to each column is summed at the postsynaptic neurons. Mathematically, the current in column j can be expressed using Kirchhoff's current law as $I_j(t) = \sum_i x_i(t)G_{ij}$, where $x_i(t)$ and G_{ij} are the input voltage pulse and the conductance of the aligned CNT FET from row i. Figure 5b illustrates the output currents from an array with 10 output neurons during the 100 ms that a training image is presented to the network. In the spiking neural network implementation, G_{ij} is updated based on a simplified spike-timing-dependent plasticity (STDP) scheme.[65] In this STDP scheme, a leaky integrate and fire operation is executed at each output to obtain the neuron potential expressed as $X_j(t)/dt - X_j(t)/\tau = I_j(t)/\tau$. When any of the output neuron potentials exceeds a specified threshold (X_{th}), a postsynaptic spike is triggered, firing the application of voltage pulse at the corresponding column and resetting all $X_j(t)$ to zero. Figure 5c plots $X_j(t)$ corresponding to $I_j(t)$ in Figure 5b, illustrating the triggering of the postsynaptic voltage pulse from the output neuron that first reaches X_{th} (neuron 2 in this case). Also indicated in Figure 5c is the implementation of lateral inhibition that consists of holding $X_j(t)$ at zero for neurons other than the one that has last fired for a short period of time (10 ms in this case), to prevent a different neuron from firing in response to the same stimulus (*i.e.*, a winner-takes-all approach).

The firing of the postsynaptic spike delivers a V_{gs} voltage pulse across the aligned CNT FETs connected to the postsynaptic neuron that has fired, resulting in a charge-trapping-induced update of their channel conductance. This change in the conductance (ΔG) is positive or negative depending on the relative timing of the pre- and postsynaptic spikes. In this implementation, synaptic potentiation (*i.e.*, positive ΔG) occurs for all aligned CNT FETs that have an input pulse width (t_{in}) that exceeds the triggering of the postsynaptic spike (t_{out}), and depression occurs for devices with $t_{in} < t_{out}$. In other words, devices that have an input voltage during the arrival of the output spike will have a small increase in their conductance, and devices without an input voltage during the arrival of the output spike will have a small decrease in their conductance. We note that other implementations aimed at realizing a biologically plausible STDP scheme attempt to achieve a ΔG that is proportional to $\Delta t = t_{in} - t_{out}$. Instead, we adopt a simplified scheme for practical hardware implementation where ΔG is dependent only on the sign of Δt and can be realized with CMOS IC processes, using only square pre- and postsynaptic voltage pulses. Figure 5d shows experimental data and model calculations for ΔG resulting from consecutive potentiating and depressing V_{gs} voltage pulses applied to an aligned CNT synaptic transistor. Calculations are from a recursive model required for spiking neural network simulations where updates in conductance are obtained as

$$\text{potentiation: } \Delta G = \text{pt}(R_{pt})^{\text{pte}} G \tag{1a}$$

$$\text{depression: } \Delta G = \text{dp}(R_{dp})^{\text{dpe}} G \tag{1b}$$

where

$$R_{pt} = (G_{max} - G)/(G_{max} - G_{min}) \tag{2a}$$

$$R_{dp} = (G - G_{min})/(G_{max} - G_{min}) \tag{2b}$$

In eqs 1 and 2, pt, pte, and R_{pt} are obtained from fitting the synaptic potentiation characteristics, and dp, dpe, and R_{dp} are obtained from fitting the synaptic depression characteristics. R_{pt} and R_{dp} are associated with the rates at which the conductance is increased/decreased, given the current state of the device as determined by the difference between the conductance and the max/min values. This modeling approach can be used to explore the effects of the synaptic device characteristics on the neuromorphic system-level performance (*e.g.*, in this case recognition rate). The recursive model is similar to those used in previous modeling work,[11,65] but is formulated for easier interpretation and to better bound conductance to the specified G_{min} and G_{max}, resulting in improved simulation stability.

In Figure 5e, we present the results of the pattern recognition simulations using the experimentally verified model of the aligned CNT synaptic transistors. The results show the recognition rate as a function of the training number for arrays with 10, 20, 40, and 80 output neurons. Each case is simulated five times, and we plot the mean value including error bars for one standard deviation. For each simulation we present a fraction of the training set images and then perform a recognition test using all 10 000 test images. During the test we keep track of spiking activity and determine the recognition rate *a posteriori* by assigning each neuron to the digit for which it spiked the most and calculating the ratio of occurrences that the assigned neuron spiked compared to the total number of spikes for a given digit. The results presented in Figure 5e are the average of all digits. Clearly, the recognition rate improves with training and also improves with increasing number of output neurons, as these provide specialization to different styles of handwriting for the same digits, resulting in improved accuracy of the algorithm. Figure 5f plots the recognition rate as a function of the number of output neurons after 60 000 training steps. In Figure 5g, we plot conductance maps for the case of 20 output neurons, which correspond to the conductance of all of the aligned CNT FETs connected to each column in the network (again after all 60 000 training steps).

In Figure 4f we present experimental data and model calculations demonstrating the impact of the amplitude of the potentiating voltage pulses (V_{pot}) on the synaptic characteristics of aligned CNT FETs. We showed that increasing V_{pot} resulted in a larger dynamic range, but also increased the abruptness of the conductance modulation. In Figure 6 we now show simulation results from the unsupervised learning pattern recognition using model fits to experimental data from aligned CNT synaptic transistors with increasing V_{pot}. We calculate the improvement (Δ) in recognition rate as a function of training number for the case of V_{pot} = 1.0 and 1.6 V and also extrapolate the model to the case of V_{pot} = 2.0 V. The results in Figure 6 show that the increased dynamic range and abruptness in modulation that results from increasing V_{pot} enhances the initial learning rate of the network (*i.e.*, larger slope during the initial training steps). This enhancement can provide a better recognition rate with a smaller number of training steps (*e.g.*, in the case of V_{pot} = 1.6 V). However, the detrimental effects of an excessively abrupt conductance modulation resulting from further increasing V_{pot} can quickly

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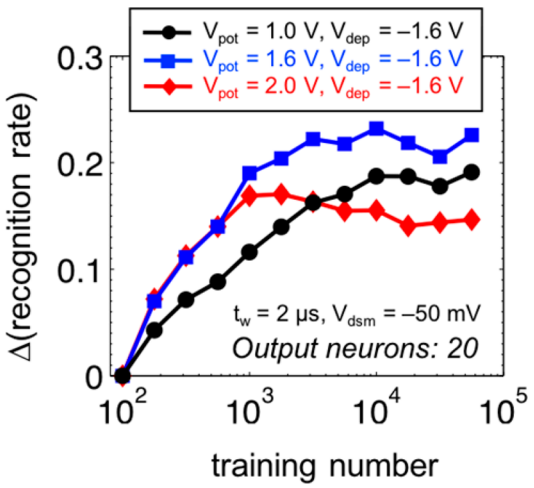

Figure 6. Improvement in recognition rate as a function of training number in aligned CNT FET spiking neural networks with increasing amplitude of potentiating voltage pulses. Learning rate can be optimized to achieve improvements in recognition with reduced number of training cycles.

saturate the improvement in recognition rate (*i.e.*, levels off at a smaller training number), limiting the accuracy achieved in the simulation for V_{pot} = 2.0 V. We note that the tuning of pre- and postsynaptic pulses can be applied globally or selectively on the network to enhance/decrease the learning rate of specific neurons and/or input patterns. Thus, the tuning of the synaptic characteristics of aligned CNT FETs presents opportunities for developing neuromorphic systems and unsupervised learning algorithms with adaptive and/or selective learning properties enabled by control of the pre- and postsynaptic pulses.

CONCLUSIONS

We have presented a synaptic transistor technology for the implementation of large-scale neuromorphic systems, based on the wafer-scale CMOS-compatible processing of CNT FETs with highly aligned nanotubes with high semiconducting purity and density. In this paper we analyze the charge-trapping mechanisms responsible for the synaptic properties of aligned CNT FETs and provide a detailed characterization based on DC and pulsed measurements. We measure a large dynamic range (*i.e.*, >10×) with gradual long-term analog programmability of conductance using potentiating and depressing voltage pulses. The robustness of the device operation and stability of the synaptic behavior are demonstrated with multiple cycles of consecutive potentiating/depressing voltage pulses and extraction of programmed conductance states. We also show tuning of the synaptic characteristics of aligned CNT FETs and establish trade-offs in the abruptness and stability of conductance modulation and the dynamic range. On the basis of the demonstrated robustness of the aligned CNT synaptic transistor we simulate the hardware implementation of an unsupervised learning for pattern recognition in spiking neural networks. The simulations are validated with experimental data from measurement-aligned CNT FET synaptic transistors and used to analyze the recognition rate of handwritten digits from the MNIST database. On the basis of the experimentally demonstrated tuning of the aligned CNT FET synaptic response, we show the impact of conductance modulation dynamic range and abruptness on the learning rate. We show that tuning of the CNT synaptic characteristics enables optimizing the learning rate and achieves higher recognition rate with a lower training number. We also discuss the tuning of aligned CNT synaptic behavior for developing neuromorphic algorithms with adaptive and/or selective learning characteristics.

METHODS

In this work, a recently improved evaporation-driven process, named floating evaporative self-assembly,[56,57] has been utilized by Carbonics Inc. to fabricate highly aligned SWCNT devices at the wafer level. The deposition method starts with a nanotube "ink" in organic solvent dispensed onto a water surface. As the solution spreads, it intersects the receiving substrate that vertically dissects the water−surface, resulting in CNT alignment occurring at the interface. Extracting the wafer at a controlled rate allows CNTs to coat the deposition area in a dense, aligned monolayer. Semiconducting-nanotube inks prepared by selective conjugated polymer sorting agents are used, leading to exceptional (>99.9%) semiconducting purity. This method deposits nanotubes in an unbundled, isolated morphology, making it possible to form robust electrical contacts to each nanotube and to achieve excellent gate-ability. Using standard processing techniques, the nanotube arrays are fabricated into top-gated aligned CNT FETs with high CNT density (>60 tubes/μm) and self-aligned T-shaped gate structure that enhances gate control, helps scaling down the channel length, and reduces parasitic capacitance (details provided elsewhere).[51,58]

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The authors declare no competing financial interest.

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