Radio Frequency Transistors Using Aligned Semiconducting Carbon Nanotubes with Current-Gain Cutoff Frequency and Maximum Oscillation Frequency Simultaneously Greater than 70 GHz

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S1: Transfer curves of self-aligned T-shape gate nanotube radio-frequency (RF) transistors under various drain-to-source biases

Figure S1(a) shows the transfer curves of a representative self-aligned T-shape gate nanotube RF transistor under various drain-to-source biases (V_{DS}) from -0.1 to -1.6 V with a step of -0.3 V. Figure S1(b) shows the corresponding on/off ratio at various V_{DS}. The on/off ratio decreases from ~2000 to ~50 with the increase of V_{DS} from -0.1 to -1.6 V, suggesting that the low on/off ratio for the T-gate RF transistors measured at V_{DS} = -1.5 V might be caused by the drain-induced barrier lowering (DIBL) effect.

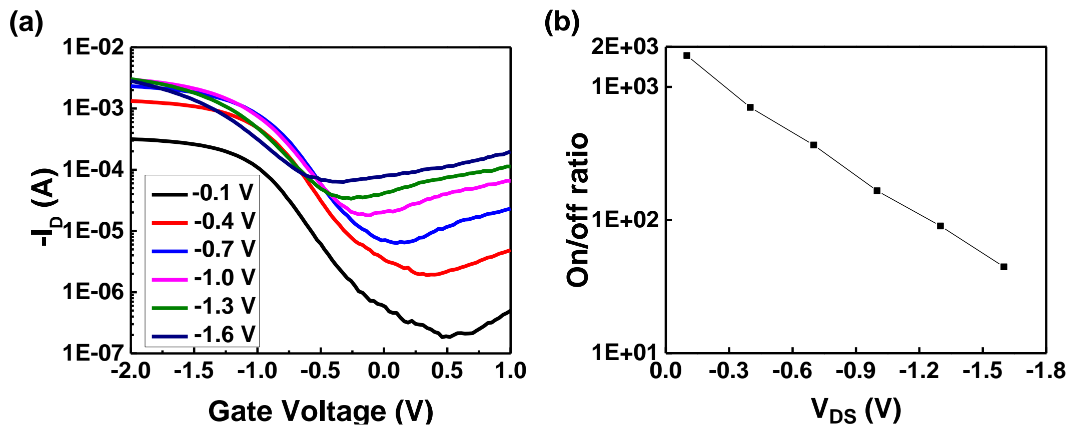

Figure S1 (a) Transfer curves of a representative self-aligned T-shape gate nanotube RF transistor under various drain-to-source biases (V_{DS}) from -0.1 to -1.6 V with a step of -0.3 V. (b) Corresponding on/off ratio at various V_{DS} extracted from (a).

S2: Device de-embedding structure

Figure S2 shows the open and short structures for the device de-embedding structure (DDS). The DDS would remove only the parasitics from the bonding pads but without removing the capacitances associated with the gate, and reveal the performance for real applications.

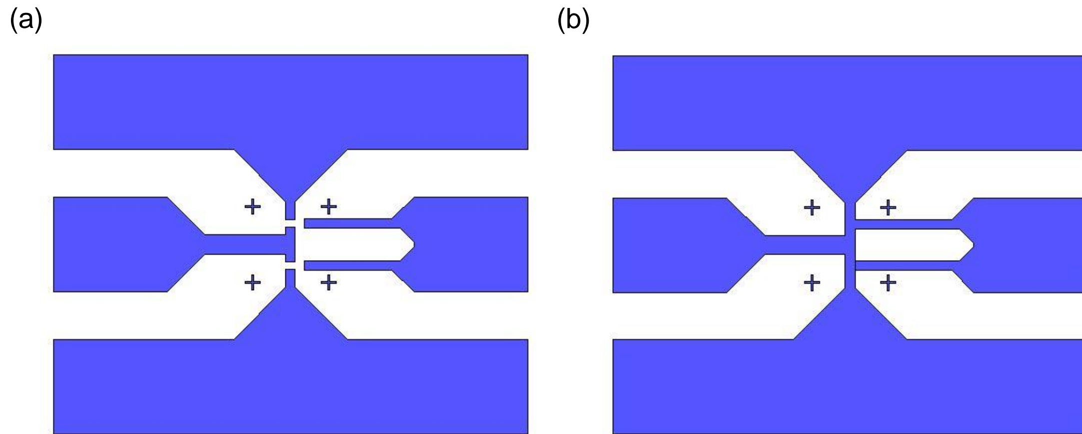

Figure S2 (a) Open structure for DDS. (b) Short structure for DDS.

S3: Intrinsic de-embedding structure

Figure S3 shows the open and short structures for the intrinsic de-embedding structure (IDS). IDS would remove the parasitics from the bonding pads and the fringe capacitances associated with the gate, and reveal the performance upper-limit of material properties.

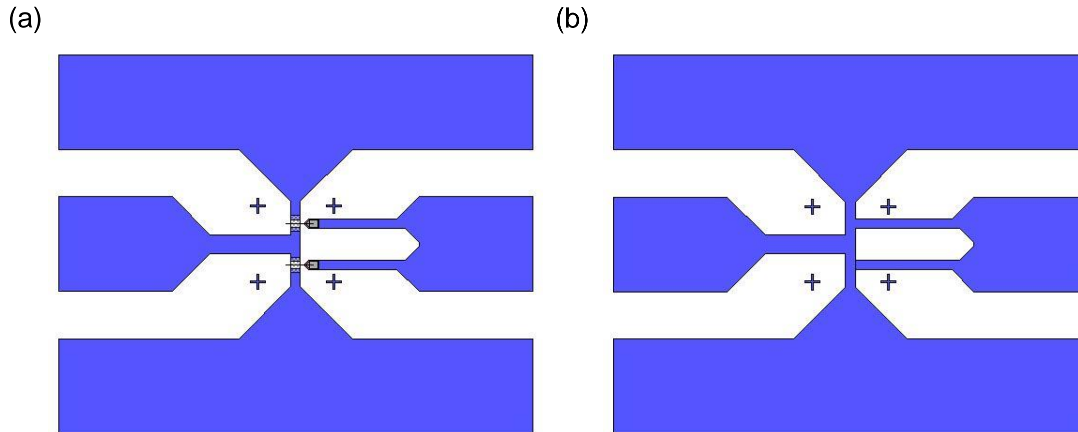

Figure S3 (a) Open structure for IDS. (b) Short structure for IDS.

S4: De-embedding process for the linearity measurement

In order to de-embed out the losses from the wires and connectors for the linearity measurement, we carried out the single-tone test for an on-chip short structure (Figure S2) at frequencies of 1, 4, 8, 12 and 16 GHz. The results for the single-tone test are shown in Figure S4(a). The losses for the wires and connectors are extracted by subtracting input power from the output power, and the results are plotted in Figure S4(b).

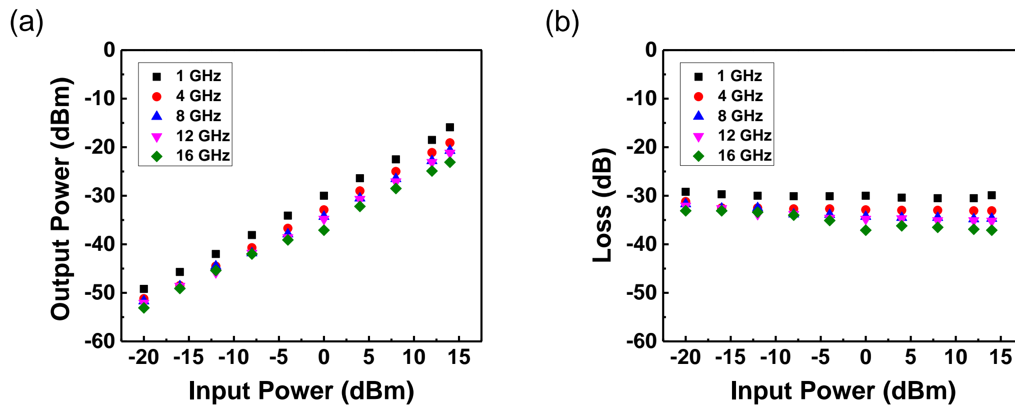

Figure S4 (a) Output power *vs.* input power curves for the single-tone test of an on-chip short structure at frequencies of 1, 4, 8, 12 and 16 GHz. (b) Losses from wires and connectors at frequencies of 1, 4, 8, 12 and 16 GHz.