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Facile Five-Step Heteroepitaxial Growth of GaAs Nanowires on Silicon Substrates and the Twin Formation Mechanism

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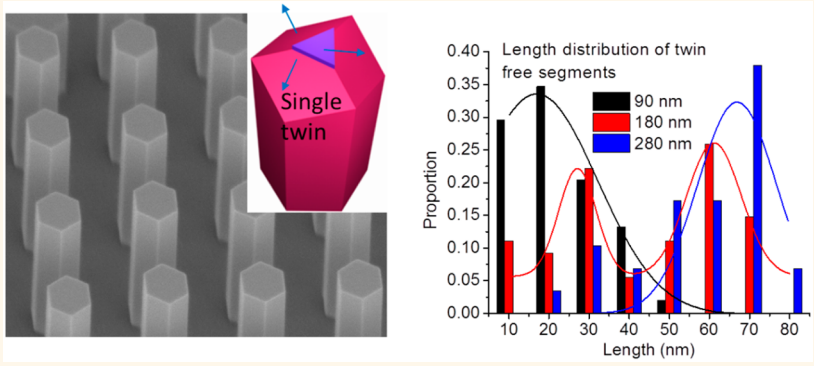
Supporting Information



ABSTRACT: **Monolithic integration of III−V semiconductors with Si has been pursued for some time in the semiconductor industry. However, the mismatch of lattice constants and thermal expansion coefficients represents a large technological challenge for the heteroepitaxial growth. Nanowires, due to their small lateral dimension, can relieve strain and mitigate dislocation formation to allow single-crystal III−V materials to be grown on Si. Here, we report a facile five-step heteroepitaxial growth of GaAs nanowires on Si using selective area growth (SAG) in metalorganic chemical vapor deposition, and we further report an in-depth study on the twin formation mechanism. Rotational twin defects were observed in the nanowire structures and showed strong dependence on the growth condition and nanowire size. We adopt a model of faceted growth to demonstrate the formation of twins during growth, which is well supported by both a transmission electron microscopy study and simulation based on nucleation energetics. Our study has led to twin-free segments in the length up to 80 nm, a significant improvement compared to previous work using SAG. The achievements may open up opportunities for future functional III−V-on-Si heterostructure devices.**

KEYWORDS: *heteroepitaxy, GaAs on Si, nanowires, twin defect, MOCVD, thermodynamics, TEM*

In recent years, semiconductor nanowires have attracted a great deal of research interest due to their unique electronic and optical properties.[1−8] III−V compound semiconductor nanowires possess advantages of high mobility, direct band gap, and the capability of band-gap engineering the properties over a wide range, making them promising candidates for future electronic,[9−17] optoelectronic,[18−28] and energy devices.[29−33] On the other hand, Si is still the dominant material in today's semiconductor industry because of its relatively low cost and mature processing technology. It thus has been a natural desire to integrate III−V semiconductors with Si to enable novel functional devices that can take advantage of the benefits offered by both materials. This technology could substantially influence the integrated circuit industry by the monolithic integration of III−V materials and Si circuitry. Of no less importance to energy research is the development of multijunction solar cells using III−V materials grown on low-cost and sturdy Si substrates.[34−36]

To achieve such integration in a thin film fashion represents a significant technological challenge caused by several problems

Received: November 16, 2015
Accepted: February 1, 2016

DOI: 10.1021/acsnano.5b07232
ACS Nano XXXX, XXX, XXX−XXX

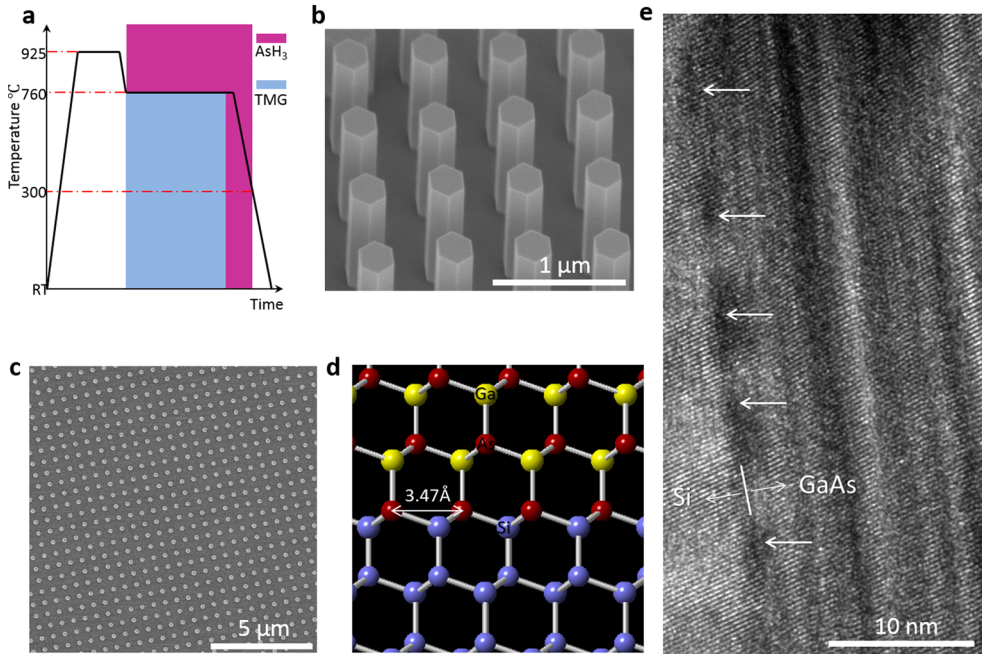


Figure 1. (a) Temperature profile of GaAs nanowire growth on Si (111). Red and blue blocks indicate the time AsH_3 and TMG are supplied, respectively. (b) The 30° tilted and (c) top view SEM images of uniform GaAs nanowire arrays grown on Si. (d) Schematic diagram of a crystal lattice at the GaAs/Si interface, viewed from the [1−10] orientation. (e) HRTEM image taken at the GaAs/Si interface. Arrows indicate sites with misfit dislocation.

intrinsic to the interface of the two dissimilar materials. Mismatches in the lattice constants and thermal expansion coefficients can lead to misfit dislocations or even nonepitaxial growth.[37,38] The polar nature of the bonds in III−V materials makes the growth on nonpolar Si difficult and causes antiphase boundaries (APBs).[39−42] The native oxide layer commonly observed on the Si surface is another major factor hindering the epitaxial growth.[43−45] The use of nanowire geometry for GaAs on Si provides benefits in this integration owing to the small lateral dimension. Strain due to lattice mismatch can be effectively relieved in the lateral directions,[46−49] and the probability of forming APBs is remarkably reduced. High-quality single-crystal III−V nanowires grown on a Si substrate have been successfully demonstrated in recent years.[43−45,50−74] A wide range of applications have also been explored including high-speed transistors,[10] tunnel diodes,[75,76] light-emitting diodes (LEDs),[18,19,28] room-temperature lasers,[20] and solar cells.[77]

The vapor−liquid−solid (VLS) growth method, which was first developed by Wagner and others in 1960s and 1970s,[78] has become the most prevalent approach to grow III−V nanowires on Si substrates. Au is widely used as the catalyst due to the ease of preparation and low reactivity. Vertical nanowire arrays have been successfully obtained through Au-catalyzed VLS in molecular beam epitaxy (MBE)[61,71,74] and metalorganic chemical vapor deposition (MOCVD).[43,58,60,62,63,73] On the other hand, the use of Au during the growth[79−81] leads to the speculation that deep levels acting as recombination centers may be created.[82] Group III atom self-catalyzed VLS growth has thus attracted attention since no foreign metal intermixing is involved in this method.[51−55,57,64−67] However, the metal droplet places constraints on the growth of axial heterostructure with different group III elements. The droplet usually remains after growth due to the properties of VLS growth and is undesired in some applications such as efficient light extraction in LEDs and good ohmic contact formation in solar cells. Significant progress has been made with non-VLS methods, including selective area growth (SAG)[44,45] and oxide-assisted self-induced growth.[68,69] In particular, pioneering work was done by Tomioka *et al.*[44,45] using SAG, where the nanowires were precisely located by a predefined array of openings in a dielectric mask and no catalyst was required. In Tomioka's work, they used a seven-step approach for the epitaxial growth of GaAs nanowires on Si, including (1) ramp-up of the sample temperature, (2) a thermal annealing at 925 °C to remove the native oxide, (3) ramp-down of the sample temperature to 400 °C, (4) surface treatment with only AsH_3 flow at 400 °C, (5) ramp-up of the sample temperature again to the growth temperature, (6) the GaAs growth at 750 °C, and (7) cooling the sample.

The high uniformity of nanowire morphology allows the fabrication of versatile devices in a controllable manner. Photodetectors,[27] LEDs,[83] and solar cells[29,33] have been achieved using nanowires. Nevertheless, rotational twins and polytypism are common defects observed in both VLS- and non-VLS-grown nanowires. These defects are believed to cause altered band structure in nanowires compared to their bulk counterpart. Carrier scattering, local quantum confinement, and nonintrinsic carrier transition processes are incurred due to the band discontinuity between zincblende (ZB) and wurtzite (WZ) regions.[84−88] Understanding the driving force for twin formation and control of its presence has become a topic of intense research. Substantial progress in eliminating twins and polytypism has been achieved for the VLS mode with a general agreement that the thermodynamics at the triple-phase interface line is the dominant factor controlling the defect formation.[51,53,89−97] The understanding of the twin formation mechanism in SAG mode is not fully understood yet and was interpreted from several different perspectives including faceted growth[98,99] and thermodynamics of nucleation.[87,100]

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ACS Nano XXXX, XXX, XXX−XXX

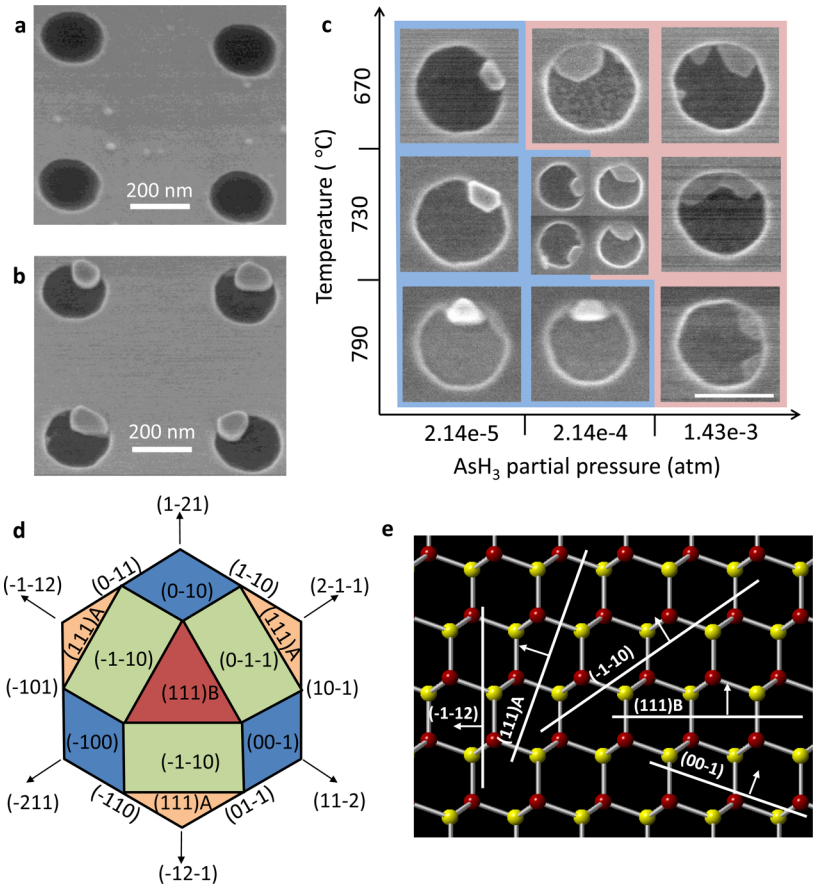

Figure 2. The 30° tilted SEM images at the mask openings on (a) GaAs (111)B and (b) Si (111) substrates after 2 min growth at 790 °C. (c) Top view SEM images of nuclei after 2 min growth at different temperatures and AsH_3 partial pressures; scale bar 200 nm. TMG partial pressure was kept constant at 7.56×10^{-7} atm. (d) Schematic of relevant low-index planes viewed from the ⟨111⟩B direction. (e) Projection of relevant low-index planes on the (1−10) plane in a GaAs zincblende lattice.

Here, we report a facile five-step heteroepitaxial growth of GaAs nanowires on Si (111) substrates using SAG and an in-depth study of the twin formation mechanism. Our five-step approach eliminates the AsH_3 surface treatment step and the associated sample temperature ramping step, which offers simplified process flow and provides 100% nanowire yield and great uniformity. In addition, our in-depth study of the nanowire twin formation mechanism has led to the growth of twin-free GaAs nanowire segments up to a length of ∼80 nm, which represents a significant improvement compared to ∼42 monolayers (∼14 nm) reported in previous work.[98]

RESULTS AND DISCUSSION

We successfully used the facile five-step approach for heteroepitaxial growth of GaAs nanowires on Si (111) substrates using SAG. The growth steps are summarized in Figure 1a. Briefly, after substrate preparation, the Si (111) substrates are immediately loaded into the MOCVD reactor. Step 1 is to ramp up the temperature from room temperature to 925 °C for hydrogen annealing. Step 2 is to keep the temperature stable at 925 °C and anneal the substrates in hydrogen ambient for 5 min to remove native oxides. Step 3 is to ramp down the temperature directly to the desired growth temperature between 700 and 790 °C, and for the case shown in Figure 1a, the temperature is 760 °C. Step 4 is the step when the nanowires grow. Precursors including trimethylgallium (TMG) and arsine (AsH_3) are introduced simultaneously at the beginning of the step, and the temperature is kept at the growth temperature. During this step, the nanowires would grow in the vertical GaAs ⟨111⟩B direction. After the desired growth time (typically ∼1 h), the final step is to close the TMG supply and cool the system while the AsH_3 precursor continues to flow until the temperature is below 300 °C to prevent nanowire decomposition. Detailed substrate preparation and growth steps are described in the Methods. Figure 1b shows a scanning electron microscopy (SEM) image taken at a 30° tilted angle of nanowires grown at 760 °C. All the wires are located uniformly in the predefined template and exhibit a 6-fold symmetric cross section consisting of {1−10} sidewall facets. Figure 1c shows a top view SEM image of the nanowire array. The yield of vertical nanowires is 100%. Compared to the seven-step growth reported by Tomioka *et al.*,[44,45] our five-step growth method could also give 100% yield and similarly high uniformity of nanowire morphology, while our direct heteroepitaxial growth without AsH_3 treatment could significantly simplify the growth temperature profile.

The lattice constants of Si and GaAs are different by 4.1%. GaAs nanowires with a small enough footprint can, however, be grown on Si coherently without generating misfit dislocations (MFDs) at the interface. Such a MFD-free interface was observed by Tomioka *et al.* when they grew GaAs on Si with an actual opening diameter of 19 nm.[44] For larger nanowires, the increased strain energy would lead to MFDs at the interface once the nanowires are beyond a critical size. Previous

DOI: 10.1021/acsnano.5b07232
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calculations based on continuum elasticity have estimated the critical height and diameter of nanowires for MFD generation and shown considerable stress relief through MFDs.[48,101] The nanowires discussed in this paper fall into this category. As shown in Figure 1d, the distance between two adjacent As atoms in the [11−2] direction is 3.47 Å, and the lattice mismatch is 4.1%, so the period of MFD is 3.47 Å/0.041 = 8.46 nm. To examine the crystal structure of our nanowires and the heteroepitaxial interface, we cut a 70 nm thin slice parallel to the {1−10} crystal planes from the center of a nanowire using a focused ion beam (JEOL). High-resolution transmission electron microscopy (TEM) images were taken with a [1−10] zone axis. A high density of twins was observed immediately after the growth started for nanowires grown at 760 °C in Figure 1e. The size of our nanowires is above the critical diameter and height for MFD-free growth, so periodic MFDs are observed at the GaAs/Si interface together with periodic contrast variation on the GaAs side due to strain distribution. The average period of the MFDs is 8.45 nm, which agrees with the calculated value based on the analysis above. Our measured period also agrees with the value calculated by Yuan *et al.* combining molecular-dynamics and quantum-mechanics simulations.[101]

To initiate coherent epitaxial growth of GaAs nanowires on Si, previous studies indicate a nucleation or surface treatment step is often required prior to the nanowire growth. For the Au-catalyzed VLS growth, Kang *et al.* found vertical nanowires can be obtained only with high-temperature nucleation followed by low-temperature nanowire growth.[63] In the case of SAG, Tomioka *et al.* pointed out that the Si surface needs to be soaked in As ambient first to form Si (111):As surface reconstruction, which is an analogue of a GaAs or InAs (111)B surface. To prevent As evaporation from this surface, low-temperature surface treatment in AsH_3 was performed prior to ramping up the temperature for the nanowire growth.[44,45] However, we used direct heteroepitaxial growth without AsH_3 treatment, which simplified the temperature profile of the growth procedure to just five steps (Figure 1a). On the contrary, as shown in the Supporting Information (Figure S1), the surface treatment step at lower temperatures only decreased the vertical nanowire yield. Furthermore, high-yield vertical nanowires could be grown even on a Si surface exposed to dry etching, showing the robustness of our method. In our study, the sizes of the mask openings for samples prepared using electron beam lithography (EBL) and photolithography were around 100 and 200 nm, respectively. One possible mechanism that allows us to grow without low-temperature surface treatment could be the relatively large size of mask openings in our study compared to those reported in other papers.[44,45,63] Because the initial growth adopts a Volmer−Weber (island) mode, as will be shown later, abundant sources captured in large mask openings ensure an adequate local supply of adatoms on the nuclei and prevent them from decomposing.

To better understand the growth behavior at the initial stage, we grew nanowire material using the five-step growth method for only 2 min (defined by the TMG supply time) on both GaAs (111)B and Si (111) substrates and examined their nuclei morphologies under SEM. The SEM images show the nuclei formed in the mask openings after growth at 790 °C and 2.14×10^{-5} atm AsH_3 partial pressure (equivalent V/III ratio = 283) on a GaAs (111)B substrate (Figure 2a) and on a Si (111) substrate (Figure 2b). The material deposited on the GaAs substrate fills the entire opening and maintains a flat surface. In contrast, the nuclei on the Si substrate appear to be islands with crystalline facets. The classic models to depict different film growth mechanisms are[102] layer-by-layer growth (Frank−van-der-Merve, or FM, mechanism), island growth (Volmer−Weber, or VW, mechanism), and the Stranski−Krastanov (SK) method (an initially continuous film that becomes islanded but with a thin continuous "wetting" layer left). The interplay among surface energies of the substrate (γ_s), the film (γ_f), and their interface (γ_i) decides the actual growth mechanism.[99] If the substrate surface energy is smaller than the sum of the two other surface energies, the island growth (VW) occurs because the exposed substrate surface is energetically favorable:

$$\gamma_s < \gamma_f + \gamma_i$$

whereas the reverse inequality,

$$\gamma_s > \gamma_f + \gamma_i$$

is associated with layer-by-layer growth (FM).

Our result agrees with early studies that GaAs-on-Si growth occurs in the VW mode.[103−105] As-passivated Si (*e.g.*, the Si (111):As surface mentioned earlier) was found to be highly inert (low γ_s) due to the existence of As lone-pair states and was even shown to be almost unaffected by exposure to oxygen or air.[106] Previous studies have also shown that the growth temperature (T_g) and the AsH_3 partial pressure (P_{AsH3}) can affect the shape of grown GaAs crystals during SAG MOCVD.[98,107] So we varied T_g between 670 and 790 °C and P_{AsH3} between 2.14×10^{-5} and 1.43×10^{-3} atm while keeping the TMG partial pressure constant at 7.56×10^{-7} atm. Figure 2c shows the top view SEM images of typical nuclei under each growth condition. All the conditions result in VW growth, and a hexagonal cross section emerges after a short time. However, the growth rates along different orientations show strong dependence on both T_g and P_{AsH3}. In general, lateral growth is suppressed under lower P_{AsH3} or higher T_g, while the vertical growth is enhanced under these conditions. We believe this is related to the different T_g and P_{AsH3} dependence of the growth rate for different crystal planes. Figure 2d shows the relevant low-index planes viewed from the ⟨111⟩B direction, and Figure 2e shows their orientations in relation to the zincblende GaAs crystal lattice viewed from the [1−10] direction. In crystal growth, facets are expressed because of their slow growth rate. At higher T_g and lower P_{AsH3} (those within the blue background in Figure 2c), the growth in the ⟨111⟩B direction is faster than in the ⟨1−10⟩ directions, so the adatoms migrate to the top of nuclei and contribute to the vertical growth. The lateral growth is instead suppressed, and clear {1−10} sidewall facets can be seen due to their slow growth. The tilted {−1−10} facets have the same surface atomic configurations as those of {1−10} sidewalls, but due to adatom accumulation at the top, the growth in the tilted ⟨−1−10⟩ directions is still faster than that in the vertical <1−10> directions. The tilted {−1−10} facets are not expressed, and the top surface is usually flat. However, in the extreme case of 790 °C T_g and 2.14×10^{-5} P_{AsH3}, the nuclei tend to be pyramids enclosed by tilted {−1−10} facets, meaning the growth rates in those directions are also significantly reduced. In contrast, when T_g decreases and P_{AsH3} increases, the growth rate in the ⟨111⟩B direction decreases and those in the ⟨1−10⟩ directions increase. The nuclei under these conditions (those within the pink background in Figure 2c) extend further laterally and show much smaller height than those grown under higher T_g and lower P_{AsH3}. The nuclei grown at 670 °C T_g and

DOI: 10.1021/acsnano.5b07232
ACS Nano XXXX, XXX, XXX−XXX

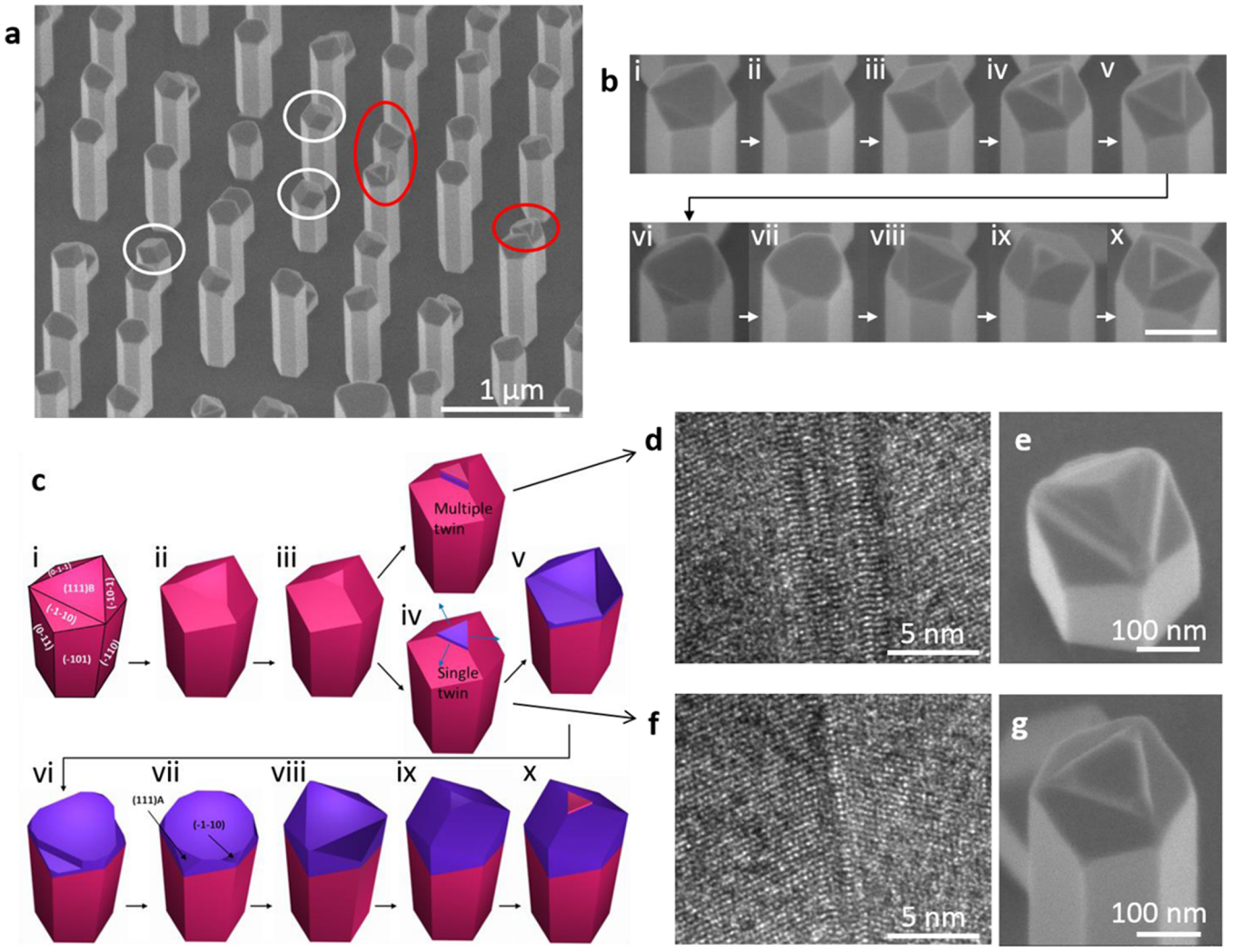

Figure 3. (a) The 30° tilted SEM images of nanowires grown at 850 °C; the initial part was grown at 760 °C to help nucleate. White circles indicate nanowires with a completely pinched-off tetrahedron tip, while red circles indicate nanowires with a triangular-shaped thin mesa surrounded by three tilted {−1−10} facets. (b) SEM images of nanowire tips with different morphologies; scale bar 200 nm. Images are organized in a sequence according to the twin formation model in (c). (c) Schematic of the twin formation process during nanowire growth. (d) TEM image of a region consisting of an even number of twins. The crystals at two sides of the transitional region share the same atomic registry. (e) SEM image of a nanowire tip. After an even number of twins, the wire pinches off. (f) TEM image of a region consisting of an odd number of twins. The crystal at two sides of the transitional region can be considered as rotated by 180° compared to each other. (g) SEM image of a nanowire tip with an odd number of twins.

2.14×10^{-3} P_{AsH3} are not as tall as the silicon nitride mask, while those grown at 790 °C T_g and 2.14×10^{-5} P_{AsH3} are around 100 nm tall. Under low T_g and high P_{AsH3} conditions, due to the increased growth rates in the ⟨1−10⟩ directions, the hexagonal cross sections are less obvious and multiple nuclei are observed. Variation of the growth rates in the ⟨111⟩B direction is believed to be dominated by the surface reconstruction that is related to As surface enrichment and is a strong function of T_g and P_{AsH3}. Ultra-high-vacuum studies by various groups found that at low T_g or high P_{AsH3} a (2×2) reconstruction takes place, which features a chemically stable As-trimer structure leading to reduced growth rate in the ⟨111⟩B direction, and at high T_g or low P_{AsH3} ($\sqrt{19} \times \sqrt{19}$) reconstruction appears.[108−113] Nishida *et al.* reported the same phase transition on the GaAs (111)B surface during MOCVD growth.[114]

The growth condition not only changes the nucleation behavior but also affects the crystal structure in terms of twin defects. Ikejiri *et al.* proposed a hypothetical growth model of GaAs shape evolution in the early growth stage during SAG MOCVD.[115] In our work, we have verified Ikejiri's growth model and can explain the twin formation mechanism by direct observation of nanowire morphologies corresponding to each evolution stage. Using our five-step growth method, the highest nanowire growth temperature was 800 °C. Above this temperature, few GaAs nanowires were observed to grow from the Si_3N_4 mask opening (see Supporting Information, Figure S2a), and we believe the reason is that at temperatures above 800 °C the desorption of the reaction species from the Si_3N_4 and Si surface is so rapid that little deposition of GaAs could occur. However, we were able to grow nanowires at 850 °C by starting the growth at 760 °C for 5 min and then quickly ramping up the temperature to 850 °C, as the growth at 760 °C would lead to GaAs nanowires in the openings, and then even at 850 °C, the reaction species can wet the GaAs nanowires better than the Si_3N_4 and Si surface, thus leading to growth

DOI: 10.1021/acsnano.5b07232
ACS Nano XXXX, XXX, XXX−XXX

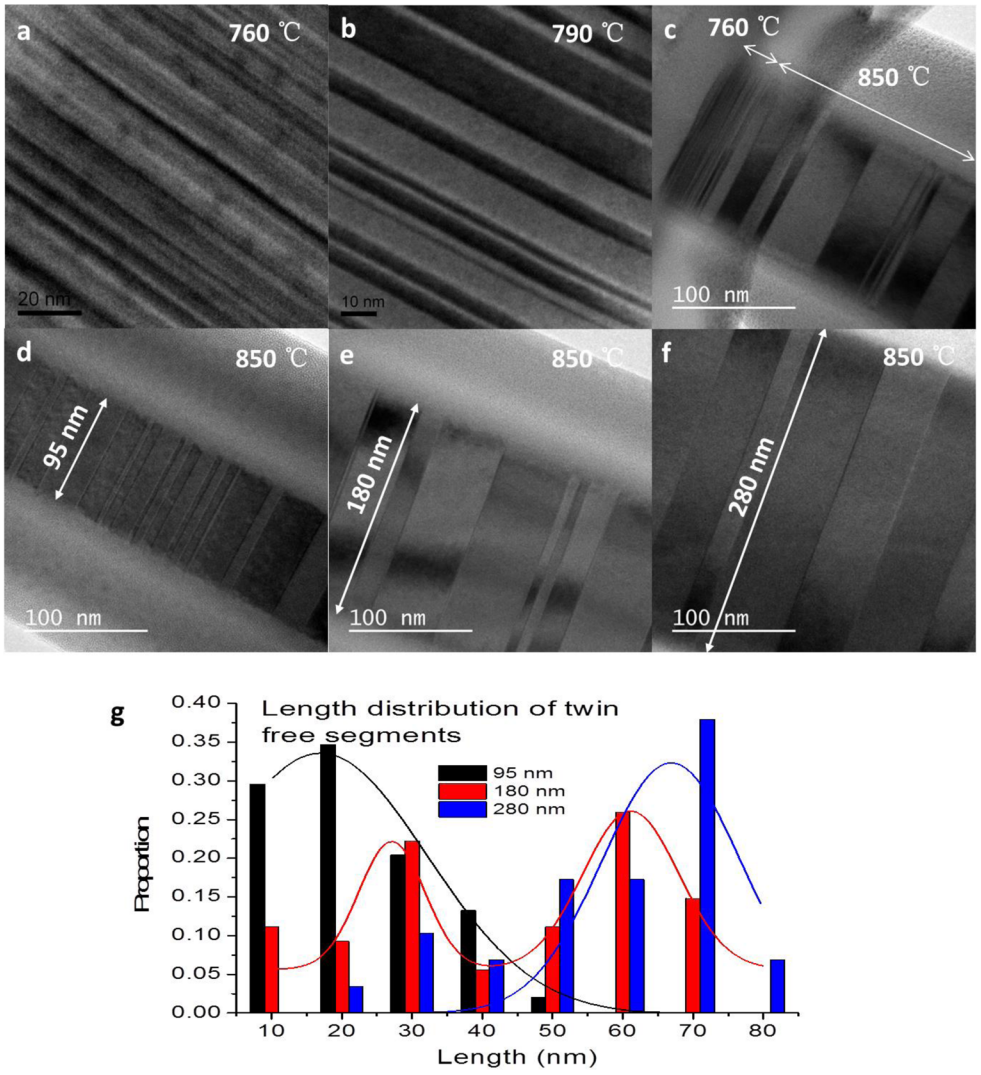

Figure 4. (a–c) TEM images of nanowires grown at different temperatures: (a) 760 °C, (b) 790 °C, and (c) 850 °C. The initial segment in (c) was grown at 760 °C in order to nucleate. (d–f) TEM images of nanowires grown at 850 °C with different diameters: (d) 95 nm, (e) 180 nm, and (f) 280 nm. (g) Histogram showing length distribution of twin-free segments of nanowires grown at 850 °C with different diameters.

even at 850 °C. Yet, as shown in Figure 3a, nanowires become much less uniform in height probably due to the longer Ga diffusion length at higher temperature, and the increased desorption rate may also influence the nonuniformities observed during growth at temperatures above 800 °C. Uneven nanowire tops appear with tilted {−1−10} facets and other low-index facets to various degrees. Some nanowires have a completely pinched-off tetrahedron tip (enclosed in white circles in Figure 3a), while some others have a triangular-shaped thin mesa surrounded by three tilted {−1−10} facets (enclosed in red circles in Figure 3a). On the basis of the various nanowire tip morphologies (Figure 3b), we demonstrate the various growth fronts and the mechanism driving the twin formation. At a temperature as high as 850 °C, the growth rate in the ⟨−1−10⟩ directions is extremely low. When a nanowire grows in the vertical ⟨111⟩B direction, the three tilted {−1−10} facets extend toward the center from three corners at the tip. Hence, the top (111)B facet is intersected by these three facets and appears to be a triangle (Figure 3c, stage i). This triangle keeps shrinking, while the {−1−10} facets further extend (Figure 3c, stage ii). When the triangle reaches a certain critical dimension, the probability of forming a rotational twin, upon the deposition of the next layer, would be dramatically increased (Figure 3c, stage iii). The critical dimension of the triangle is related to the change of the Gibbs free energy for the growth of the next bilayer of the triangular area. In smaller triangles (*i.e.*, larger peripheral/area ratios), the smaller peripheral energy density of the rotated stacking, compared to that of the normal zinc-blende stacking, makes twin formation energetically more favorable. Mathematical details of the nucleation–growth model will be provided later in this article. If no twin forms, the tip will pinch off and the nanowire growth terminates. Otherwise the triangular (111)B facet will stop shrinking but expand laterally as a mesa instead after a twin is introduced (Figure 3c, stage iv).[98,99] When a twin is formed at the interface of the nucleus and the substrate, the crystal lattice of the nucleus can be considered to be rotated by 60° (or 180° given the 3-fold symmetry) azimuthally in relation to that of the substrate. The tilted ⟨−1−10⟩ directions of the substrate are thus no longer the same slow-growth directions for the nucleus, and the lateral growth rate in those directions become considerable. The twinned mesa will fill up all the space above the original {−1−10} facets, making the nanowire top flat (Figure 3c, stages v to vii). Sometimes another slow-

DOI: 10.1021/acsnano.5b07232
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growing facet, the (111)A facet, will appear temporarily before the mesa forms a complete flat hexagonal top (Figure 3c, stage vii). When the growth proceeds, three {−1−10} facets of the newly grown crystal above the twin will start to emerge at the three corners, different from those where the original {−1−10} facets stem. At this point, the (111)B facet starts to shrink again and the growth will repeat the whole process mentioned above. Through this repeating growth sequence, quasiperiodic twins are introduced during the nanowire growth. We also notice that around the critical size of the (111)B triangle the twinned mesa is metastable. After the first twin forms, multiple consecutive twins are also highly likely to take place. If even numbers of the twins form before the mesa eventually stabilizes, the new stable crystal shares the same lattice orientation as the original crystal underneath the first twin (TEM image in Figure 3d). Thus, three {−1−10} facets emerge from the edges of the triangle mesa and would finally pinch off the tip (Figure 3e). Similar to the effect of a single twin, an odd number of twins will rotate the lattice by 60° (TEM image in Figure 3f) and allow the stabilized mesa to expand laterally (Figure 3g).

According to the growth model, the twin density or length of a twin-free segment is determined by how soon a flat hexagonal (111)B top surface shrinks to the triangle of critical dimension. In other words, the critical triangle size and the nanowire diameter together determine the length of a single twin-free segment. Figure 4a to c are TEM images of nanowires grown at different temperatures, and the different crystal orientations between two segments separated by a twin are manifested by the brightness contrast. Distinct twin densities indicate strong temperature dependence of the growth characteristics. For nanowires grown at 760 °C (Figure 4a), twins form every few monolayers, while twin-free segments can extend longer than 10 nm in nanowires grown at 790 °C (Figure 4b and Supporting Information Figure S3). The difference is even more striking in Figure 4c, where we have the initial part grown at 760 °C and later part grown at 850 °C. An abrupt interface exists, across which the twin density changes dramatically. A strong correlation between the growth temperature and the twin density is demonstrated. As one can see in the Supporting Information (Figure S4), the twins in the initial part are so dense that in many cases they form every monolayer, which makes the crystal effective in the wurtzite structure. As will be discussed in detail later, higher temperature features a smaller critical dimension, while in the case of lower temperature, the probability of forming a twin is considerable even when the (111)B facet is fairly large.

Because the probability of forming a twin increases when the tip is around the critical dimension, a larger diameter would also favor fewer twins, as it takes longer for the tip to reach that critical size. Our observation of twin-free segments on nanowires with different diameters grown at the same temperature is consistent with the observation by Yoshida *et al.*[98] Yoshida's work indicates that the thickness of the twin-free segments decreases as the nanowire diameter decreases. They used nanowires with 200 and 380 nm diameters and showed that the twin occurrence probability per monolayer for the 200 nm diameter nanowires is higher than that for 380 nm diameter nanowires. The largest thickness of twin-free segments is ∼42 monolayers, corresponding to ∼14 nm in length. In our work, nanowires were all grown at 850 °C with 95, 180, and 280 nm diameters controlled by the size of the opening in the silicon nitride mask. Figure 4d to f are the TEM pictures of these nanowires with different diameters (95 nm for Figure 4d, 180 nm for Figure 4e, and 280 nm for Figure 4f). Although they were all grown at the same temperature, the length distributions of twin-free segments are substantially different. As shown by the statistics in Figure 4g, the length of the twin-free segment becomes larger with increasing diameter. The average twin-free lengths for nanowires of 95, 180, and 280 nm diameters are 17.9, 39.1, and 53.1 nm, respectively. Gaussian peak fittings are superimposed on the histogram to show that the peaks shift toward larger twin-free length with increasing diameters. The nature of the twin peaks for the 180 nm nanowire is not fully understood at this point. The longest twin-free segment comes from our 280 nm sample, with a twin-free length of 80 nm. This twin-free length of 80 nm in GaAs nanowires using SAG is a significant improvement compared to previous work.[98] We attribute our improvement in the twin-free length to the unusually high growth temperature (850 °C) we can achieve.

On the basis of the growth model mentioned earlier, the maximum length of a twin-free segment occurs when the tip is completely pinched off. According to the geometry of the tetrahedron enclosed by three {−1−10} facets, the maximum length would be 33.6, 63.6, and 99 nm for nanowires of 95, 180, and 280 nm diameters. All the lengths we measured are below the theoretical limit, with only one exception, for the 95 nm nanowire, as can be seen in Figure 4g (one data point is between 40 and 50 nm). This discrepancy could be due to the fact that the TEM sample might not have been cut right through the center of the nanowire, so the actual diameter is larger than what we observed. We also assumed zero growth rate in the ⟨−1−10⟩ directions, while in the real situation a finite growth rate cannot be ruled out.

To interpret the effects of growth temperature and diameter, we have calculated the twin-free segment length probability distribution $P(h)$ using a simple nucleation−growth model.[87] We considered a hexagonal GaAs nanowire with diameter D, in which a new twin-free segment starts to grow at height $h = 0$ to form a tetrahedral island on the (111)B top surface. At height h, the next GaAs bilayer of area $A(h)$ can grow with either the zinc-blende (zb) or fault (f) stacking.[87] The change of the Gibbs free energy for the growth of the next bilayer of area A is given by

$$G_0^{\lambda}(A) = [\varepsilon_{\text{area}}^{\lambda} - \mu_{\text{gas}}(T)]A + \varepsilon_{\text{edge}}^{\lambda}\sqrt{A} \quad (\lambda = \text{zb or f}) \tag{1}$$

where $\varepsilon_{\text{area}}^{\lambda}$ and $\varepsilon_{\text{edge}}^{\lambda}$ are the areal and peripheral energy densities of the bilayer and $\mu_{\text{gas}}(T)$ is the chemical potential of the vapor, which depends on the temperature T in addition to the vapor pressures of the reactant gases.[87] $G_0^{\lambda}(A)$ takes a maximum value, $G_*^{\lambda} = G_0^{\lambda}(A^*)$, at a critical area A^*. We note that $\mu_{\text{gas}}(T)$ decreases with increasing temperature, so the critical area A^* also decreases with increasing temperature, leading to increased twin-free segments. The Gibbs free energy used to obtain the twin statistics is then

$$G^{\lambda}(h) = \begin{cases} G_0^{\lambda}(A(h)) & (A(h) \le A^*) \\ G_*^{\lambda} & (A(h) > A^*) \end{cases}$$
$$(\lambda = \text{zb, or } \lambda = \text{f when } A(h) > A^*) \tag{2}$$

In the case of fault bilayers (where the twin boundaries are λ = f and $A(h) \le A^*$), we also need to take into account the twin−twin interaction,

$$G^{\text{f}}(h) = G_0{}^{\text{f}}(h) + \varepsilon_{\text{int}}(h)\,A(h) \tag{3}$$

DOI: 10.1021/acsnano.5b07232
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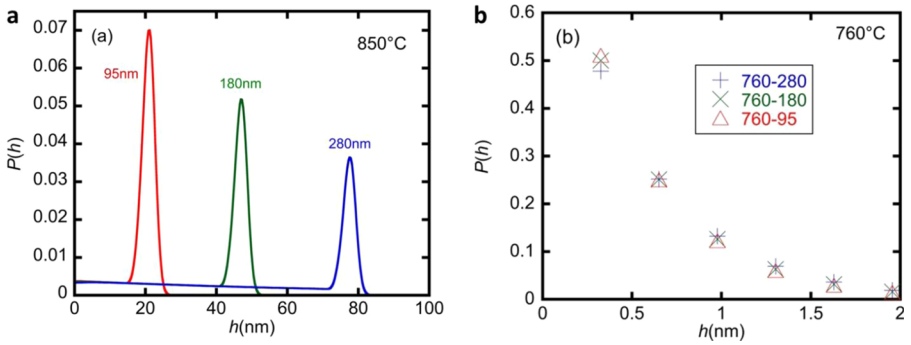

Figure 5. Probability distribution of the twin-free segment length in GaAs nanowires of diameters 95, 180, and 280 nm at (a) 850 °C and (b) 760 °C.

where $\varepsilon_{int}(h)$ is the twin−twin interaction energy density.[116] The probability to find a twin at height h is calculated as

$$p(h) = \frac{\exp[-G^{f}(h)/k_{B}T]}{\exp[-G^{f}(h)/k_{B}T] + \exp[-G^{zb}(h)/k_{B}T]} \quad (4)$$

where k_B is the Boltzmann constant, and $G^{zb}(h)$ and $G^{f}(h)$ are calculated using eqs 2 and 3, respectively, as the twins occur at $A(h) \leq A^*$. The probability for the first occurrence of a stacking fault at the nth bilayer is then

$$P(n\Delta) = \prod_{i=1}^{n-1} [1 - p(i\Delta)]p(n\Delta) \quad (5)$$

where Δ is the distance between consecutive bilayers.

Figure 5 shows the calculated $P(h)$ for three diameters, D = 95, 180, and 280 nm, at temperatures T = 850 °C and T = 760 °C. At T = 850 °C, the calculated distribution in Figure 5a exhibits a sharp peak for every diameter, where the peak position is an increasing function of D. Accordingly, the average twin-free segment length is 19, 37, and 53 nm for D = 95, 180, and 280 nm, in reasonable agreement with the experimental observations. In contrast, at a lower T = 760 °C, when the twin-free segment is expected to be much shorter, the distribution is nearly independent of D and decays rapidly to zero within the first few bilayers, as can be seen in Figure 5b.

CONCLUSION

We have reported facile five-step heteroepitaxial growth of GaAs nanowires on Si (111) substrates using SAG MOCVD. Highly uniform nanowire arrays could be obtained without low-temperature surface treatment in arsine before nanowire growth. The effects of growth temperature and arsine partial pressure were carefully studied during the initial nucleation process for GaAs nanowires on Si. We are able to grow nanowires at unusually high temperature (850 °C) and obtain a variety of tip morphologies to demonstrate the twin formation mechanism. A twin-free length up to 80 nm in our GaAs nanowires grown at 850 °C with 280 nm diameter is a significant improvement compared to previous work. The temperature dependence as well as diameter dependence were well interpreted by a mechanism of faceted growth and nucleation thermodynamics. The results deepen our understanding of twin defects frequently observed in nanowires and could open up great opportunities of heterostructure devices requiring epitaxial III−V material on a Si substrate.

METHODS

Nanowire Growth. A silicon nitride layer was first deposited on double-side polished epi-ready Si (111) substrates using plasma-enhanced chemical vapor deposition. EBL (Raith eLine Plus) or photolithography (ASML S500/300 DUV Stepper) followed by dry (CF_4) or wet etching opens up an array of openings in the silicon nitride layer. No difference in vertical nanowire yield was observed between dry and wet etching. Uniform nanowire arrays could even be obtained on substrates with CF_4 overetched into Si by 5 nm. After resist strip-off and oxygen plasma cleaning, samples were quickly dipped in 7:1 buffered oxide etchant for 3 s, blown dry with nitrogen, and immediately loaded into MOCVD reactor. Nanowires were then grown in a vertical Thomas Swan MOCVD showerhead reactor at 0.1 atm pressure. Trimethylgallium and arsine were used as the precursors for Ga and As. The total flow rate of the carrier gas was 7 standard liters per minute, and partial pressures for TMG and AsH_3 are 7.56×10^{-7} and 2.14×10^{-4} atm unless otherwise stated. Prior to actual nanowire growth, the substrate was annealed in hydrogen ambient for 5 min at 925 °C. We found this step to be essential, as growth with hydrogen annealing at lower temperature results in an increased number of irregular growths (see Supporting Information Figure S5). The temperature was then decreased to nanowire growth temperature between 700 and 790 °C, and the TMG and AsH_3 precursors were introduced simultaneously. After growth the TMG was interrupted, while AsH_3 continued to flow until the temperature is below 300 °C to prevent decomposition of the GaAs at high temperature.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b07232.

Details on GaAs nanowire arrays grown on Si with different hydrogen annealing temperatures, with and without low-temperature surface treatment, SEM images of Ga diffusion at different growth temperatures, distribution of twin-free segment length in nanowires grown at 790 °C, and a high-resolution TEM image at the interface of Si and GaAs for 850 °C growth temperature with 760 °C buffer growth sample (PDF)

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Notes

The authors declare no competing financial interest.

DOI: 10.1021/acsnano.5b07232
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ACKNOWLEDGMENTS

This material is based upon work supported as part of the Center for Energy Nanoscience (CEN), an Energy Frontier Research Center (EFRC) funded by the U.S. Department of Energy, Office of Science and Office of Basic Energy Sciences, under Award Number DE-SC0001013. Computing resources were provided by the USC Center for High Performance Computing and Communications. M.Y. was funded by a USC Provost's Ph.D. Fellowship.

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