

An RTD/Transistor Switching Block and Its Possible Application in Binary and Ternary Adders

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Abstract—We propose and demonstrate both a binary and ternary adder circuit based on a resonant tunneling diode (RTD) and a bipolar transistor. The basic switching cell consists of an RTD in series with the base of a bipolar transistor. The RTD is used to set a threshold voltage for the switching of the transistor.

I. INTRODUCTION

THE peaked current–voltage (I – V) characteristic of Esaki tunnel diodes allows implementation of both binary and multistate logic with fewer devices than conventional transistor circuits. The simplest demonstration of this is when a resistor acts as a load for a tunnel diode (Fig. 1). If the resistor has a larger value than the average negative differential resistance (NDR) the load line intersects the RTD I – V characteristics more than once, allowing two stable operating points for the circuit exist.

The application of the NDR characteristics of Esaki tunnel diodes to digital switching circuits was recognized and demonstrated shortly following the first demonstration of the tunnel diode [1]. However, the large junction capacitance and difficulty in fabrication of uniform Esaki tunnel diodes proved to be a stumbling block for integrated circuits [2], [3].

Precisely controlled semiconductor heterostructure epitaxial growth techniques have lead to the development of the resonant tunneling diode (RTD) which has a similar peaked I – V characteristic [4], [5]. Multiple RTD's can be integrated in series to produce a multiple peaked structure [6]. RTD's do not suffer from the same problems as Esaki tunnel diodes and have been used to implement a number of different circuit designs [7]–[10].

In addition to discrete RTD's, integration of RTD's with conventional transistor structures into a single three-terminal device has been demonstrated [11]–[13]. The advantage of this approach is the decoupling of the output from the input that is associated with three-terminal operation while retaining the peaked I – V characteristics. The disadvantage is that of increased fabrication complexity for certain configurations.

We propose and demonstrate a simple yet flexible switching configuration using a single discrete RTD and a single transistor. In this configuration, the RTD is responsible for the multiple switching but does not set the operating logic levels.

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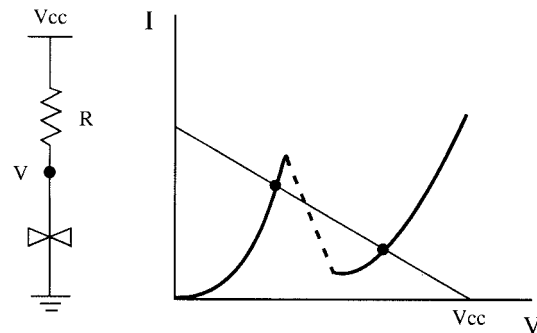


Fig. 1. I – V characteristics of an RTD using a single load resistor. The NDR region of the RTD allows two stable operating points to exist for the same circuit. The point lying on the NDR region is not stable.

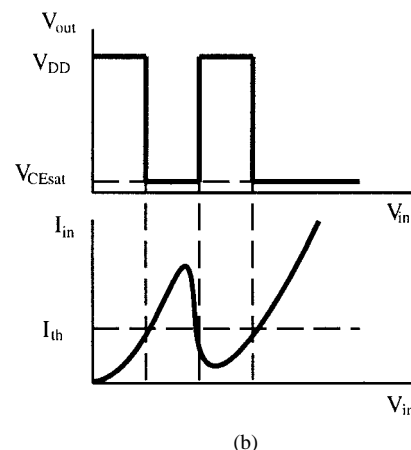
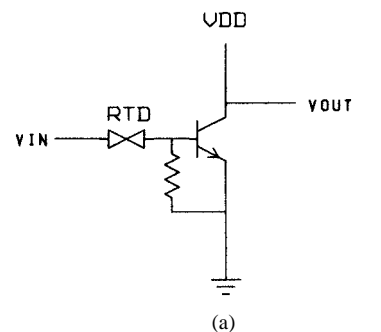


Fig. 2. (a) Schematic of the switching block. (b) Transfer function of the switching block compared with the RTD transfer function.

This approach eliminates uncertainty in logic levels due to fluctuations in individual RTD characteristics, increasing the noise margin for each state.

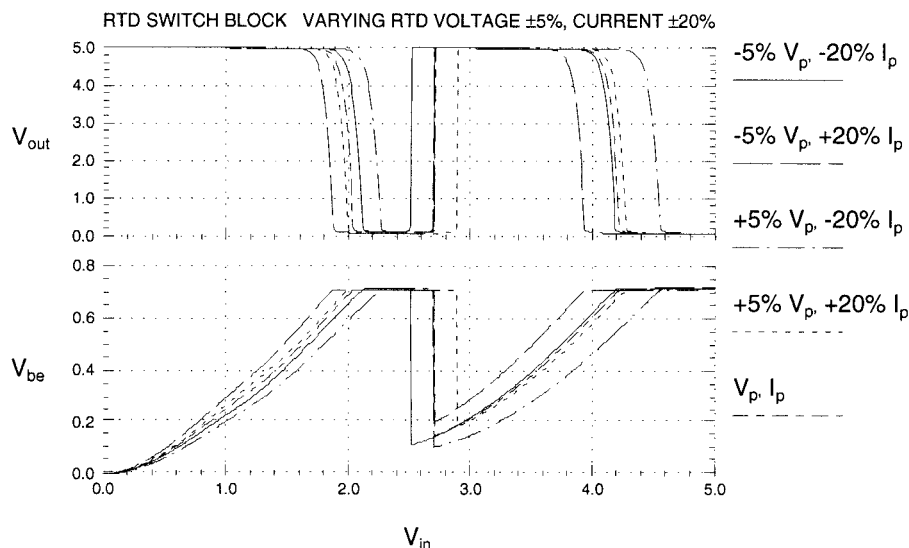


Fig. 3. Simulation of the output voltage ($V_{DD} = 5$ V) and the transistor base-emitter voltage for different RTD $I-V$ characteristics. The peak current/voltage of the RTD was varied by $\pm 20\%$ ($\pm 5\%$).

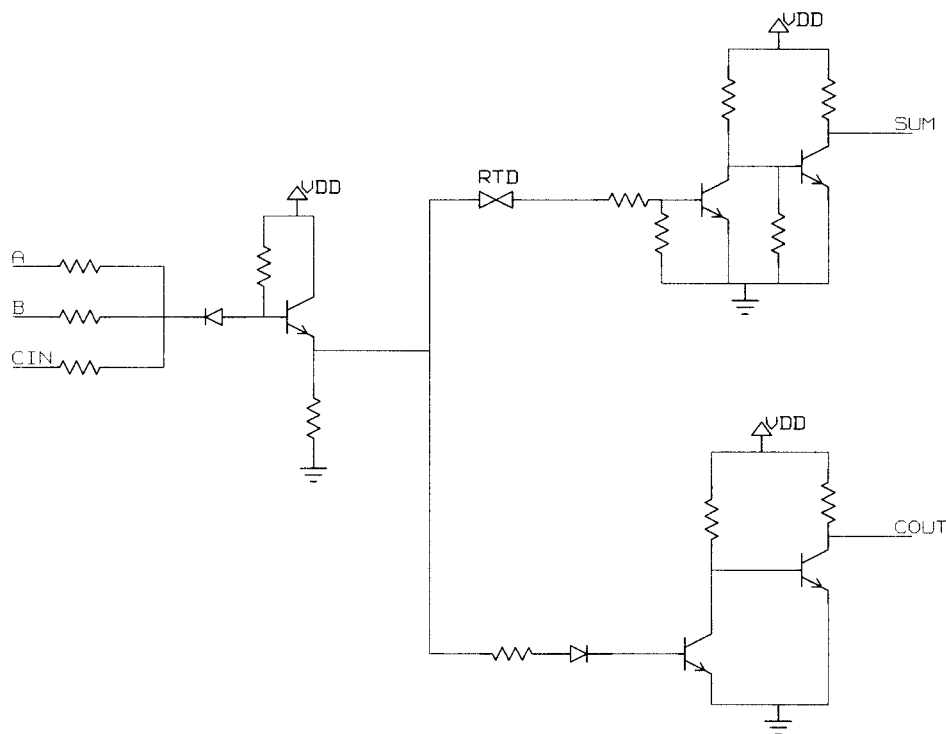


Fig. 4. Schematic of a full binary adder using the RTD/transistor switching block.

II. RTD/TRANSISTOR SWITCHING BLOCK

The basic switching block is shown in Fig. 2(a). A schematic of the transfer function is shown in Fig. 2(b). The multiple switching results from the nonlinear RTD $I-V$ characteristics, while the transistor acts as both an output buffer to the RTD, and a source of gain. An input buffer (not shown) is required for a constant input impedance.

When V_{in} is zero, the transistor is off, and V_{out} will be V_{DD} . As V_{in} is increased, the voltage across the transistor base-emitter junction will linearly increase as determined by the shunt resistance, assuming the base impedance of the transistor is much greater than the shunt resistance. Once the

input current is large enough that the voltage drop across the shunt resistor is equal to the turn-on voltage for the base-emitter junction, the transistor will begin to draw the excess input current, the transistor will be forced into saturation, and V_{out} will be forced to V_{CEsat} .

At some point, the voltage drop across the RTD will increase such that it is operating in the NDR region (i.e., the dynamic resistance will increase), and the input current will drop sharply, turning off the transistor, thus switching V_{out} back to V_{DD} . When the input current again exceeds the threshold value, the transistor will turn on, and V_{out} will switch back to V_{CEsat} .

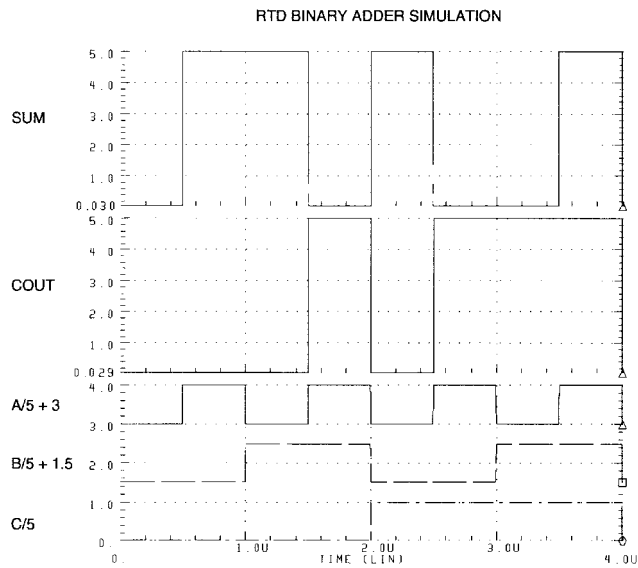


Fig. 5. Simulation of the full adder. The inputs A,B,C scaled to fit on the same set of axes.

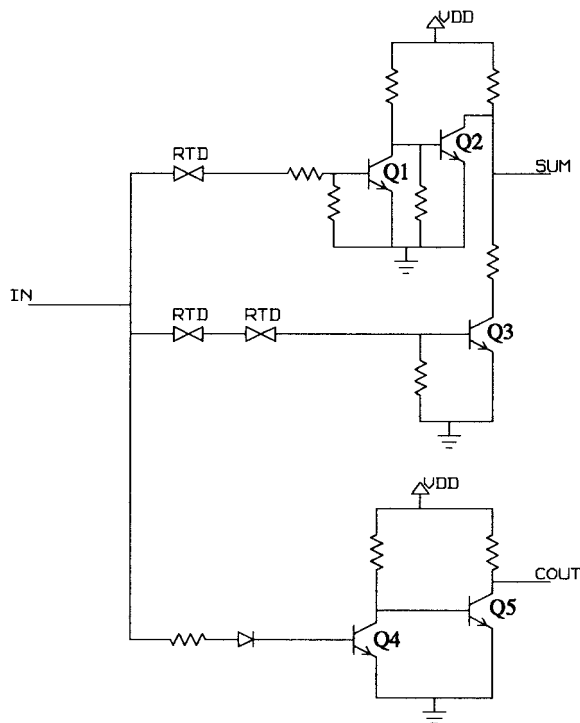


Fig. 6. Schematic of a ternary adder. V_{DD} for the carry output is half that for the sum output.

Small fluctuations on the order of a single monolayer in the epitaxial structure used to form an RTD can cause relatively large fluctuations in both its peak current and peak voltage characteristics [14], [15]. The uncertainty of these parameters reduces the robustness of RTD circuits using resistive and RTD loads. The threshold nature of the switching element described here helps to reduce the effects of those fluctuations. The voltage at which the threshold is reached can be set by choosing the appropriate value for the shunt resistor.

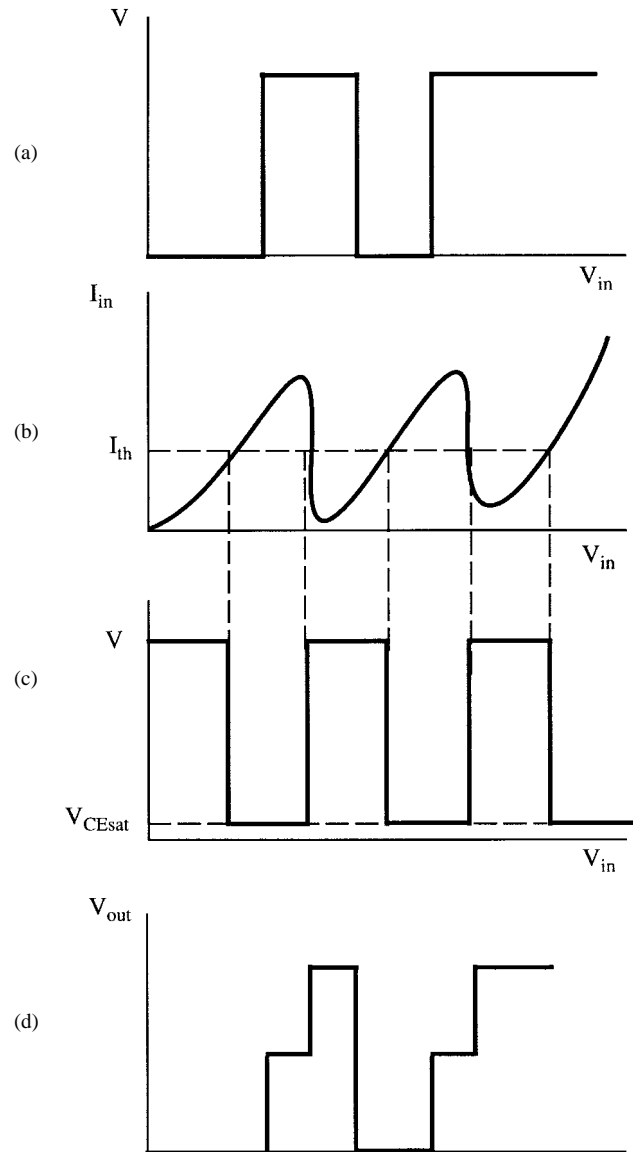


Fig. 7. Various transfer function schematics for transistors in the ternary adder circuit. (a) Schematic of transfer function of Q2. (b) Input current to switching block with two RTD's in series (i.e., Q3). (c) Collector voltage for Q3. (d) Sum voltage for the circuit.

Fig. 3 shows the output of the switching block for different RTD $I-V$ characteristics. The peak current (voltage) can vary by as much as $\pm 20\%$ ($\pm 5\%$) and still produce the same output voltage for input voltages of, for example, 1.25, 2.5, 3.75, and 5 V which are easily producible by using a resistive ladder network to generate V_{in} . Because the output voltages are generated by sources external to the RTD, there is no uncertainty in operating voltage levels resulting from fluctuations in the RTD $I-V$ characteristics, and hence, errors are not propagated through a circuit consisting of a number of switching blocks in series.

A disadvantage to the switching block as described is that it relies on forcing the output of a transistor into hard saturation. This can be eliminated while still obtaining identical functionality, at the cost of more transistors, by replacing the transistor with an emitter coupled pair.

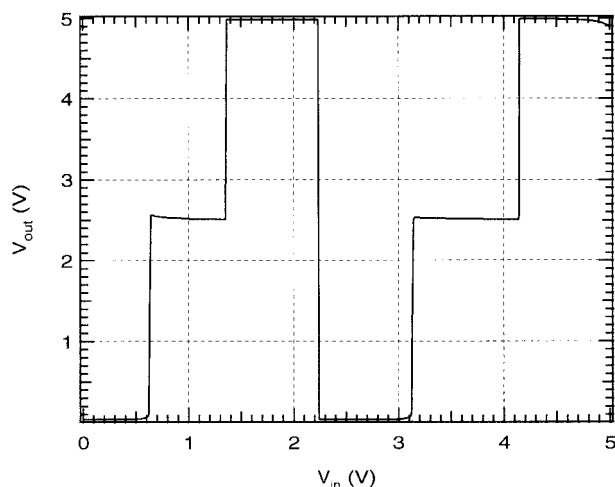


Fig. 8. Measured transfer function for the ternary adder circuit.

III. ADDER CIRCUITS

A. Binary Adder

The usefulness of this switching block is demonstrated in Fig. 4, which is a full adder, including carry bit. The simulated output is shown in Fig. 5. A full adder, built using conventional architectures requires 25 ~ 30 transistors. The circuit shown here uses five, plus one RTD. Of those five, three function as buffers and/or inverters. The sum bit is simply the switching element with an inverter to give the correct polarity. The carry bit is a saturable amplifier. Advantages of the reduced device count are more functionality for the same on chip area, or reduced fabrication tolerances for a given amount of functionality area density.

With proper choice of output stages, the lower output voltage could be set very near to 0 V, implying a large on/off voltage ratio. It is important to note that this does not achieve the same low power dissipation as is generally associated with efforts to increase the peak/valley current ratio of RTD's. This is because in the circuit, even when the output voltage is low, there is still current flowing through the RTD (and the shunt resistor). Thus the valley current of the RTD is still the limiting factor to low power dissipation.

B. Ternary Adder

Increasing the number of logic levels used in a circuit can further reduce the number devices required for a given functionality and/or complexity of the device interconnect scheme [16]. An RTD based ternary adder has previously been demonstrated [17]. That circuit was a clock based circuit where the output voltages were determined directly by a resistive load line on an RTD.

We demonstrate a ternary adder using two switching blocks, one with a slight modification with respect to the other. The circuit, shown in Fig. 6, has the same advantages as those described for the binary adder. The first block consists of Q1, and an inverter, Q2. The transfer function for this stage only is shown in Fig. 7(a). When two appropriately sized RTD's are connected in series, a multiple peaked $I-V$ characteristic is

obtained, as shown in Fig. 7(b). This adds an extra switching cycle to the transistor Q3. The thresholds are set such that Q3 initially switches before Q1 (and hence Q2). The full circuit transfer function is obtained as follows: When Q1 is off, Q2 is on and the sum is low, regardless of Q3. When Q1 is on, and Q2 is off, the output is high if Q3 is off. However, if Q2 is off and Q3 is on, the output is midway between high and low, assuming the collector resistors for Q2 and Q3 are equal. The *measured* transfer function for the circuit is shown in Fig. 8.

IV. CONCLUSION

We have demonstrated the switching characteristics of a simple switching block based on a single RTD and a single transistor. The configuration switches when a threshold current through the RTD is obtained, decreasing the variability from RTD peak current and voltage fluctuations. The switching block was used to build both a binary and a ternary adder with a minimum number of active circuit elements.

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