Random telegraph signals and noise behaviors in carbon nanotube transistors

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(Received 3 July 2006; accepted 3 November 2006; published online 11 December 2006)

A random telegraph signal appears at a smaller absolute gate bias for a larger absolute drain-source bias in a carbon nanotube transistor. Its mechanism is attributed to a defect located in the drain side of the Schottky barrier carbon nanotube transistor with Ti/Au as contact material. Furthermore, room temperature random telegraph signal is presented for both semiconducting and metallic carbon nanotubes, indicating the need to include random telegraph signal as a noise source for carbon nanotube transistors. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2402224]

Due to the small diameters of carbon nanotubes (CNTs), CNTs are very sensitive to charges including oxide defects and air molecules. Large $1/f$ noise has been observed in the CNT devices.[1,2] It is also shown that single defect centers could have a pronounced effect to modify carrier transport by changing carrier mobility in long carbon nanotube field effect transistors (CNT-FETs), whose transport is diffusive. Random telegraph signal (RTS) is observed as a result of random charging and discharging of defects when the defect levels are close to the Fermi energy of the CNTs.[3,4] This kind of RTS characteristics is quite similar to the RTSs in standard metal-semiconductor oxide field effect transistors (MOSFETs). However, CNT-FETs are quite different from MOSFETs. One important feature is the presence of Schottky barriers (SBs) in the metal-carbon nanotube junctions.[5–8] Both gate bias and drain-source bias could strongly modulate the width and thus the resistance of SBs, and they in turn will affect the transport of CNT-FETs. Being different from planar metal-semiconductor contacts, there is a weak Fermi level pinning effect for metal-CNT Schottky contacts due to the one-dimensional geometry of CNTs.[9] This property gives an opportunity to improve the CNT-FET performance by selecting suitable work function metal materials for source/drain contacts.[10] In this letter, we will focus on specific RTS behaviors, which are different from those in standard MOSFETs. First, due to the difference in the band diagram especially near the drain region, RTS in CNT-FETs shows different gate and drain-source dependences compared to standard MOSFETs if defect centers are located near the drain side of CNT-FETs. Furthermore, we report room temperature RTSs for both semiconducting and metallic CNTs confirming the generality and importance of RTS in CNT-FETs.

Back side gated CNT-FETs are fabricated by the standard chemical vapor deposition method.[11] The nanotubes were synthesized on a Si substrate with 500 nm oxide as gate dielectric. The process produces nanotubes with diameters of 1–3 nm and lengths of several microns. Photolithography was applied to define the electrodes on top of the nanotubes with 4 μm distance, followed by Ti/Au deposition as contacts.

Figure 1(a) plots the source-drain current (I_{ds}) as a function of the gate bias, showing p-FET characteristics. A RTS appears at the gate bias ranging from −33 to −26 V, strongly depending on the drain-source bias. As shown by the red arrow, the gate bias in which the RTS appearance shifts to a smaller absolute value for a larger absolute drain-source bias. This behavior often happens for the RTS in CNT-FETs; however, this cannot be explained by the prin-

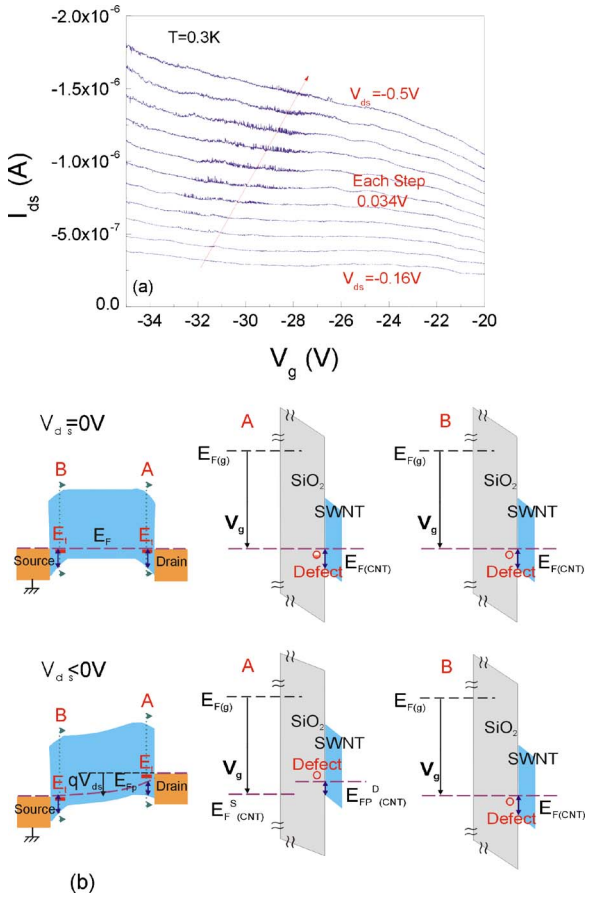

FIG. 1. (Color online) (a) drain-side RTS as a function of gate bias at drain-source biases from −0.16 to −0.5 V with −0.034 V each step, showing that the RTS appears at a smaller absolute gate voltage for a larger absolute drain-source bias. (b) Band diagrams for both along and perpendicular directions at $V_{ds}=0$ V and $V_{ds}<0$ V with the same V_g, illustrating the mechanism of the drain-side RTS in the Schottky barrier CNT-FET.

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ciple of standard MOSFETs. In MOSFETs, only the RTS switching rate shows a strong dependence on the drain-source voltage for a small drain-source bias due to the carrier heating effect.[12,13] Even with the consideration of the effective channel potential, the RTS should appear in a larger absolute gate bias for a larger absolute drain-source bias,[14] and this is opposite to the experimental results. In order to explain the controversial results, it is necessary to note that there are SBs present in the back side gated CNT-FET since Ti/Au was used as the contact material. Thus, in this kind of SB CNT-FETs, RTS could be classified into two types depending on the defect physical locations along the channel: in the channel region and near the contact region. For a defect center located in the channel region, RTS will behave similarly to that in standard MOSFETs.[15] However, the observed RTS belongs to the case that a defect is located near the drain-side Schottky contact. In our experiment, at $V_g = -32$ V and $V_{ds}=0$ V, the energy level of the defect is below the Fermi level of the CNT-FET, and no RTS could be observed, as shown in the top of the Fig. 1(b). When a negative drain-source voltage is biased, the drain-source voltage drops mainly near the drain side, where the energy difference between the quasihole Fermi level and the valence band edge will decrease dramatically, since there will be more chances for holes to transport through the drain Schottky contact, as shown in the bottom of Fig. 1(b). The energy difference from the defect level to the oxide valence band edge and the valence band offset of single-walled nanotube (SWNT)/oxide do not change with biasing. Therefore, the quasihole Fermi level moves downwards with respect to the SWNT valence band edge in the oxide interface near the drain side. Meanwhile, the band bending for the SiO_2 becomes smaller due to the less effective channel potential, so that the defect level moves slightly downwards with respect to the SWNT valence band edge in the oxide interface. Because RTS defects are normally located very close to the interface, the change of defect energy could be less than the change in the quasihole Fermi level for the same drain-source bias in the CNT-FETs. Thus the quasihole Fermi level could align with the defect level, and the RTS appears at a suitable V_{ds} ($V_{ds}=-0.228$ V) [the third curve from the bottom in Fig. 1(a)]. For an even larger negative V_{ds}, the local quasi-Fermi level will be pushed below the defect level, and in order to align these two levels, a smaller gate bias is needed, as indicated in the bottom of Fig. 1(b). Quasihole Fermi level near the source side or along the channel will be affected slightly by V_{ds}, and therefore the defect near the source side or along the channel shows no RTS regardless of V_{ds}.

To further confirm that the physical location of the defect center is in the drain side of the original setup (case 1), we compare the RTS appearance in three other bias arrangements. Electrodes I and II are swapped with V_{ds} kept the same (case 2), as shown in the bottom of the green dash curve in Fig. 2(a). The original RTS disappears after the swap. This is because small drain-source voltage drops near the "new" source side, and therefore, neither the quasihole Fermi energy nor the defect level changes much. Note that here we define the source as the grounded electrode. If the $V_{ds}=0.27$ V is biased to the swapped device (case 3), the RTS reappears except for the sign of the current, as illustrated in the upper green dash curve. This is because in this situation the band diagram along the channel region is almost the same as that in case 1 except for minor effective channel

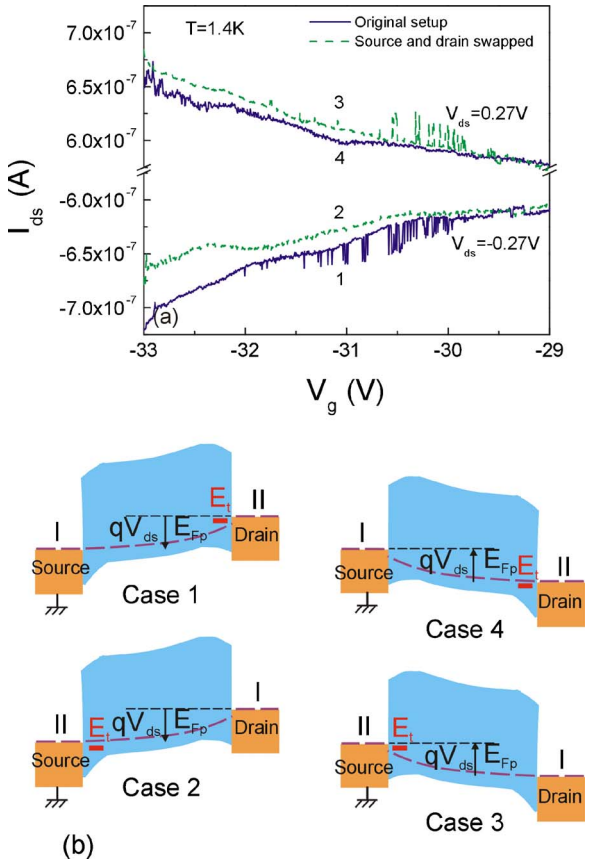

FIG. 2. (Color online) (a) Source-drain current as a function of gate voltages. Case 1: electrode I grounded as source and electrode II biased at $V_{ds}=-0.27$ V; case 2: electrode II grounded and electrode I biased at $V_{ds}=-0.27$ V; case 3: electrode II grounded and electrode I biased at $V_{ds}=0.27$ V; and case 4: electrode I grounded and electrode II biased at $V_{ds}=0.27$ V. (b) Corresponding band diagrams for the four cases.

potential difference shown in Fig. 2(b). For the original setup, applying $V_{ds}=0.27$ V will remove the RTS, shown by the upper blue solid curve (case 4). These results are consistent with the picture that the RTS is due to the defect center located in the drain side of the original setup.

Another RTS is observed at room temperature from a similar CNT-FET over a large range of gate bias, as illustrated in Fig. 3(a), indicating that the defect center is located at the interface of the CNT and SiO_2. The CNT-FET is inspected under scanning electron microscopy and it is shown that there are four SWNTs across the source and drain electrodes, which leads to the large device current. Figure 3(b) shows the fast switchings in CNT-FET up to a couple of tens of microseconds; the finite rising and falling times (~ 2 μs) in the top picture of Fig. 3(b) are due to the finite bandwidth limitation of our operational amplifier (500 kHz). The observation of the RTS at room temperature with fast switching rate further sheds light on the potential RTS applications as a tool for material and device characterization as well as a sensitive probe for the understanding of fundamental physics.[4] We also examine a SWNT with a diameter of 3 nm, whose atomic force microscopy (AFM) image is shown in Fig. 4(a). The *I-V* characteristic of CNT-FET is plotted in Fig. 4(b), showing a metallic behavior with no gate modulation. A giant RTS can be clearly observed up to 80% of the total source-drain current for $V_{ds}=-1$ mV. The RTS does not reveal drain-source bias dependence from -0.3 V to -1 mV [Fig. 4(b) (b) (I)–(II)] as described previously for the

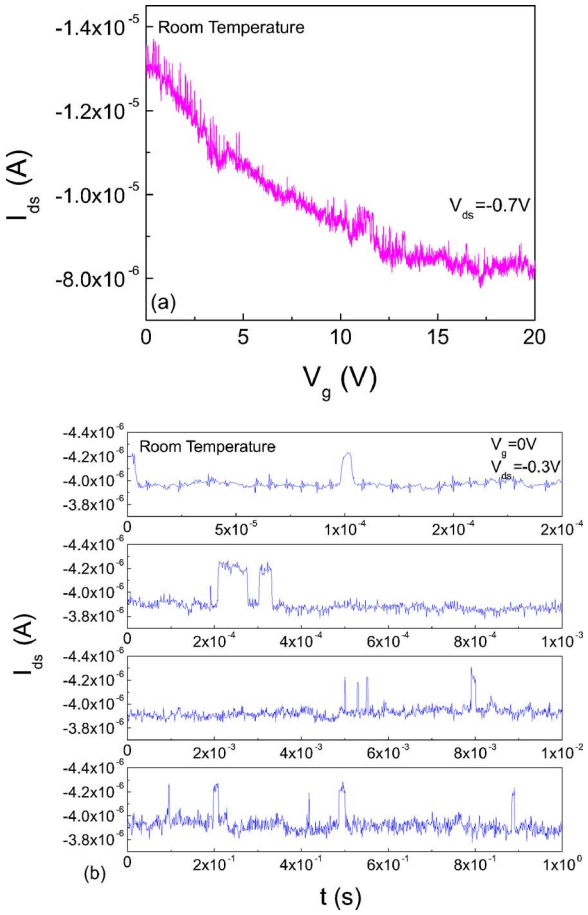

FIG. 3. (Color online) (a) Room temperature RTS appearing at a wide range of gate bias for a semiconducting CNT-FET. (b) The time dependent data illustrating a fast switching behavior for the room temperature RTS.

drain-side RTS. The RTS remains observable after the source-drain swapping [Fig. 4(b) (IV)] in agreement with the model of the defect center located in the channel region. In addition to the giant room temperature RTS, at least one more RTS could be clearly observed particularly from Fig. 4(b) (II). The observation of the giant RTS in the metallic carbon nanotube further confirms that the degradation of carrier mobility is the major contribution for individual defect fluctuations in long CNT-FETs, while the effects of the change of the carrier number and the shift of threshold voltage in CNT are minor.[3] Furthermore, it is shown that stochastic variation limit, which is the assumption of $1/f$ noise,[16] is inaccurate for describing the variability effect in small devices such as CNT-FETs. The observations of room temperature RTSs for both semiconducting and metallic CNTs suggest the need to include RTS as an important noise source for CNT-FET and other nanodevice modeling.

In summary, the random telegraph signals were studied with the emphasis on the unique characteristics in the carbon nanotube transistors. One of the major differences between the back-gated carbon nanotube field effect transistors from the standard metal oxide semiconductor field effect transistors was the presence of Schottky barriers near the source and/or drain contacts. A drain-side RTS was observed and its mechanism was attributed to the quasihole Fermi level modulation near the Schottky barriers by the applied drain-source bias. Moreover, room temperature RTSs in a semiconducting CNT-FET with a fast switching rate and a metallic CNT-FET with a giant switching amplitude up to 80% of the total current were reported, which seems to suggest the possible application for using RTS in nanodevices as a sensitive metrology tool.

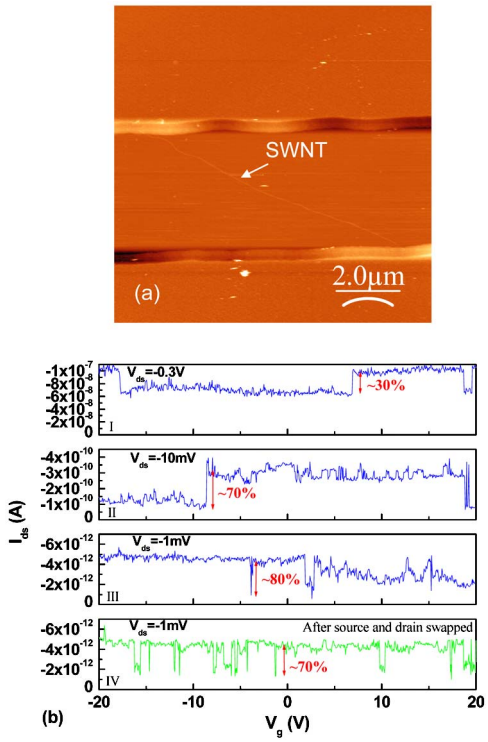

FIG. 4. (Color online) (a) AFM image of a SWNT with a diameter of 3 nm. (b) Room temperature I_{ds}-V_g for the CNT-FET at various drain biases: V_{ds} =−0.3 V (I), V_{ds}=−10 mV (II), and V_{ds}=−1 mV (III), measured in, and the source-drain current after swapping the source and drain electrodes (IV).

This work was in part supported by the MARCO Focus Center on Functional Engineered Nano Architectonics (FENA).

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