Study of Random Telegraph Signals in Single-Walled Carbon Nanotube Field Effect Transistors

Fei Liu, *Student Member, IEEE*, Kang L. Wang, *Fellow, IEEE*, Chao Li, and Chongwu Zhou

***Abstract*—Random telegraph signals (RTSs) are observed in the single-walled carbon nanotube (SWNT) field-effect transistors. The RTS mechanism is studied in detail. It is shown that trapping/detrapping due to the defects in the oxide is the main reason for RTSs in the carbon nanotube field-effect transistors (CNT-FETs). The amplitude of the RTSs in CNT-FETs is mainly attributed to mobility modulation. The defect causing the RTSs is a hole-type Coulomb repulsive center located near the valance band of the SWNT.**

***Index Terms*—Carbon nanotube (CNT), random telegraph signal (RTS).**

I. Introduction

ONE-DIMENSIONAL (1-D) nanoscale devices, such as carbon nanotubes (CNTs) and various nanowires, have been synthesized [1]–[3]. These kinds of 1-D self-assembled devices can be grown, in principle, on top of any substrates without misfit dislocations. CNT and nanowire field-effect transistors (FETs) offer the potential of low cost high-performance devices with improved subthreshold slope and transconductance over Si metal oxide semiconductor field-effect transistors (MOSFET) [4]. However, to date, due to the lack of control of orientation, uniformity, and the presence of spurious charges, large-scale integration remains a problem. From the noise point of view, based on Hooge's empirical formula [5]

$$\left\langle \frac{\Delta\sigma}{\sigma} \right\rangle = \frac{2\times 10^{-3}}{N_{\rm tot}} \cdot \frac{\Delta f}{f} \tag{1}$$

where $N_{\rm tot}$ is the total density of mobile carriers and f is the center frequency, it is predicted that flicker noise ($1/f$ noise) increases with the down-scaling of device size. Large $1/f$ noise may significantly effect the low-frequency performance of small devices and thus increase phase noise of radio frequency (RF) circuits. For example, in mixed signal technologies, base-band low-frequency noise can be up-converted to produce amplitude modulation and phase modulations and degrades the spectral purity of the carrier [6], [7]. In the time domain, $1/f$ noise is related to random jumps between two or several conductance levels, caused by the trapping and detrapping of carriers, i.e., so-called random telegraph signals (RTSs) [8], [9]. As the channel width scales down, the RTS effect becomes large. In this paper, the physical model of RTSs in 1-D CNT-FET devices will be described. After that, the mechanism of RTSs in 1-D CNT-FETs will be analyzed. Then, the stability and uniformity of the CNT-FETs will be discussed.

Manuscript received September 1, 2005; revised February 13, 2006. The review of this paper was arranged by Associate Editor A. Toriumi. This work was supported in part by the MARCO Focus Center on Functional Engineered Nano Architectonics (FENA).

F. Liu and K. L. Wang are with the Device Research Laboratory, Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA (e-mail: feiliu@ee.ucla.edu).

C. Li is with Atomate Corporation, Santa Barbara, CA 93103 USA.

C. Zhou is with the Department of Electrical Engineering, University of Southern California, Los Angeles, CA 90089 USA.

Digital Object Identifier 10.1109/TNANO.2006.880906

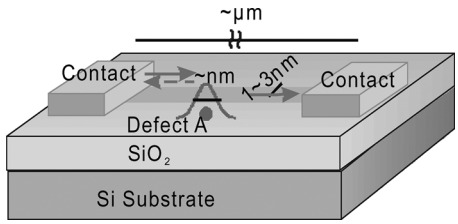


Fig. 1. Schematic drawing of CNT-FET (p-channel) with one defect inside SiO_2.

II. RTSs in Single-Walled CNT-FETs

CNT-FETs used in this paper are backside gated. They were fabricated on a highly doped p-type silicon substrate covered by a thermal oxide layer 200∼500 nm thick. Single-walled carbon nanotubes (SWNTs) were synthesized following a standard chemical–vapor deposition (CVD) method [10]. These nanotubes have diameters varying from 1∼3 nm and lengths of several micrometers. Photolithography was used to define electrodes on top of the nanotubes with 4-μm distance between two electrodes, followed by Ti/Au deposition as metal contacts. The schematic drawing of the measured devices is shown in Fig. 1.

Fig. 2(a) shows a standard p-type semiconducting CNT-FET (sample 1) characteristic with a threshold voltage of -3.3 V at 4.2 K, except there are jumps at the gate bias of roughly -26 V, as emphasized by a circle. The inset enlarges this range to show the detail. Typical time dependence of the source–drain current at $V_{ds} = -0.3$ V measured at every 0.3 s for a total time interval of 400 s is indicated in Fig. 2(b). The emission and capture time constants with respect to the gate voltage are obtained by calculating the statistic average time constraints from the time-dependent RTS at a temperature of 4.2 K with $V_{ds} = -0.3$ V and V_g varying from -24.4 to -27.6 V. The results are plotted in semi-log format in Fig. 2(c).

The observed two-level fluctuations with the current switching amplitude of 50 nA show that only one defect with single charge state contributes to the RTS. When a negative V_g bias is applied, the Fermi energy of the CNT moves towards its valence band, and the SiO_2 band is also adjusted with respect to the Fermi level as shown in Fig. 2(d). At a small negative gate bias, the defect energy level is well below the CNT Fermi level, and no hopping/tunneling can happen.

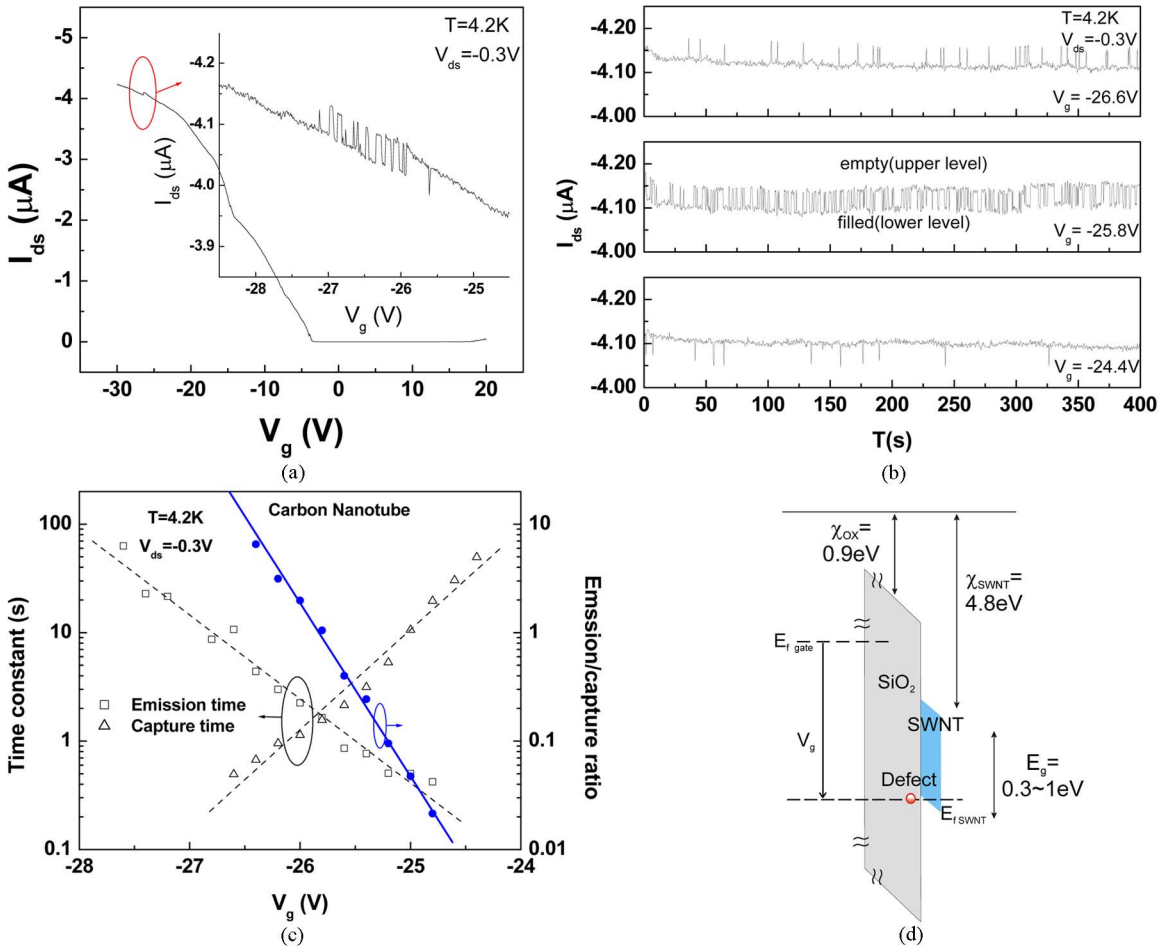


Fig. 2. (a) Current as function of V_g at $T = 4.2$ K and $V_{ds} = -0.3$ V showing a typical p-type FET characteristic. There are RTS jumps at V_g about -26 V due to single defect in SiO_2. These jumps are enlarged in (a) for clarity. (b) Typical time dependence of source–drain current (RTS) due to single defect observed for total time period of 400 s with $V_{ds} = -0.3$ V under three different gate biases, -24.4, -25.8, and -26.6 V, respectively. (c) Statistic of emission/capture time constants and emission/capture ratios for single defect level as function of gate bias. Emission/capture ratio follows detailed balance relation. (d) Energy band diagram illustrates alignment of Fermi energy with one defect level as gate bias is varied.

When $V_g < -25$ V, the defect level and the CNT Fermi level move close to each other so that hopping and tunneling happen. The higher state (larger absolute value of source–drain current) corresponds to the defect in its neutral state; the lower state corresponds to the defect in positive/negative charged state [indicated in the bottom of Fig. 2(b)]. This is because when the defect is charged, the current level becomes lower due to Coulomb scatterings. With a larger negative gate bias, the hole density in the SWNT increases, so that the carrier capture time (τ_c) decreases

$$\tau_c = 1/nv\sigma \tag{2}$$

where n is the hole density per unit volume in the SWNT, v is the average hole velocity, and σ is the average capture cross section. From emission and capture time constants in Fig. 2(c), the capture and emission process can be determined. The higher absolute current level happens when the defect is neutral; the lower absolute current level happens when the defect is positively charged by a hole. The defect is a hole-type Coulomb repulsive center. Furthermore, as shown in Fig. 2(d), the electron affinity energy of SWNT is about 4.8 eV [11], and the bandgap of semiconducting SWNTs is approximately $1/d$, where d is the diameter of the SWNT in nanometers. The SWNT has a bandgap in the range of 0.3∼1 eV, depending on its diameter. The defect locates near the valance band of the SWNT in the energy space.

The defect level moves further up with respect to the CNT Fermi level by applying a larger negative gate bias; the probability of observing the filled state is enhanced. At a gate voltage of -25.8 V, the Fermi energy of CNT and the defect energy align with each other. The probabilities of the defect to be charged and empty are almost equal, i.e., the statistics of occurrences at the high and low current levels are almost the same as shown in the middle of Fig. 2(b). From the gate bias from -25.8 to -27 V, the defect level has a greater probability to be filled in [the top of Fig. 2(b)] until the defect is completely occupied by a hole. According to the detailed balance relation, the emission/capture ratio of a hole for the defect state is

$$\frac{\tau_e}{\tau_c} = \frac{1}{g \cdot \exp\left(\frac{E_T - E_F}{k_B T}\right)} \tag{3}$$

where g is the energy degeneracy of the trap, E_T is the defect energy, E_F is the Fermi energy of the SWNT, k_B is the Boltzmann constant, and T is the carrier temperature, which may be higher than the ambient temperature due to carrier heating at large

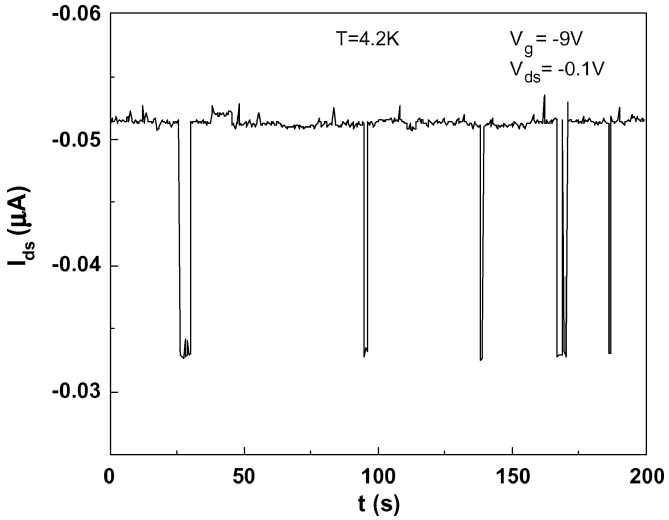


Fig. 3. RTS in CNT-FET with 40% of total current at 4.2 K with bias of $V_g = -9$ V and $V_{ds} = -0.1$ V.

source–drain biases. Thus, the relation between the change of the defect energy level with respect to the SWNT Fermi energy and the ratio of emission and capture time constants as a function of gate bias is [8]

$$\frac{\partial(E_T - E_F)}{\partial V_g} = k_B T \frac{\partial \ln\left(\frac{1}{g}\cdot\frac{\tau_c}{\tau_e}\right)}{\partial V_g}. \tag{4}$$

This indicates that the gate dependence of the emission and capture ratio is related to the gate dependence of $E_T - E_F$. Moreover, the gate dependence of $E_T - E_F$ is determined by the defect location, i.e., the left term of (4) is larger for a deeper defect (located deep inside oxide) than for a shallower defect. Since the RTS appears in the strong inversion of the CNT-FET (sample 1), the change of the Fermi energy due to the change of gate bias is small; the distance of the defect away from the CNT and SiO_2 interface could be obtained approximately using

$$x = h * \frac{k_B T \cdot \left[\ln\left(\frac{1}{g}\cdot\frac{\tau_c}{\tau_e}\right)\Big|_{V_{g1}} - \ln\left(\frac{1}{g}\cdot\frac{\tau_c}{\tau_e}\right)\Big|_{V_{g2}}\right]}{V_{g1} - V_{g2}}. \tag{5}$$

From Fig. 2(c), the spatial location of the defect is roughly 1 nm underneath the CNT/SiO_2 interface.

As shown in Fig. 2(a), the switching amplitude is about 1% of the total current. Another RTS from a similar CNT-FET (sample 2) with an amplitude of 20 nA (40% of the total source–drain current) is observed at 4.2 K [in Fig. 3(a)]. After the scanning electron microscopy (SEM) inspection, it is found that the CNT-FET (sample 1) have two carbon nanotubes between two electrodes, while the CNT-FET (sample 2) has one carbon nanotube. The number of the channels between two electrodes is one of the reasons for the RTS amplitude difference in these two cases, which is also confirmed from other CNT-FET samples. Normally, the switching amplitude of RTSs in the CNT-FETs is much larger than that in MOSFETs [12] because of the small diameters of SWNTs ($\sim$2 nm). The other possible reason for the difference in the switching amplitude could be attributed to the different defect location and scattering strength. If a defect is near the surface of the CNT/SiO_2 interface, the Coulomb potential will significantly perturb hole transport in the CNT and create a large switching amplitude. The change of current resulting from this defect charging/discharging can be expressed as

$$\frac{\Delta I}{I} = \frac{\Delta n}{n} + \frac{\Delta \mu}{\mu} \tag{6}$$

where I, n, and μ represent the current, the mobile carrier density, and the carrier mobility, respectively. Both the degradation of effective mobility and the decreasing of the number of carriers in the CNT may contribute to the decreasing of the current. An unscreened Coulomb scattering matrix due to one defect at (x_i, y_i, z_i) in a quantum wire from a carrier initially with wavevector k_x in channel m is [13]

$$\begin{aligned} M(q_x) &= \left\langle k'_x, n \left| V_i^0(r,x) \right| k_x, m \right\rangle \\ &= \frac{e^2}{4\pi\varepsilon} \int dz \int dy \varphi_n^*(y,z)\varphi_m(y,z)\frac{1}{L} \\ &\quad \times \int dx \frac{e^{-i(k_x - k'_x)x}}{\sqrt{(x-x_i)^2 + (y-y_i)^2 + (z-z_i)^2}} \\ &= \frac{e^2}{4\pi\varepsilon} \int dz \int dy \varphi_n^*(y,z)\varphi_m(y,z) K_0 \\ &\quad \times \left(|q_x|\sqrt{(y-y_i)^2 + (z-z_i)^2}\right) \end{aligned} \tag{7}$$

where $q_x = k_x - k'_x$, φ is the carrier wave function, ε is the dielectric constant, K_0 is the zeroth order modified Bessel function, and L is the normalization length of 1-D wire. Considering one two-channel and the forward–backward transport in the SWNT, the scattering rate is [13]

$$\begin{aligned} \frac{1}{\tau_m(k_x)} &= \frac{e^4}{4\pi^2\varepsilon^2\hbar^3} \\ &\quad \times \sum_{n=1,2} \left[\frac{m_n^*}{|k'_x|}\left(\left|M\left(k_x - k'_x\right)\right|^2 + \left|M\left(k_x + k'_x\right)\right|^2\right)\right] \end{aligned} \tag{8}$$

where m_n^* is the effective mass of the carriers. It is known that the screening length of the Coulomb potential in the semiconductor is on the order of several nanometers because of the charge screening of the channel holes [14]. Since a typical SWNT has a diameter of about 1$\sim$3 nm. Thus, the Coulomb potential from a single defect lying very close to the CNT interface can almost block off the transport channels. This fact is in clear contrast to the lateral current transport in the two-dimensional (2-D) case in most previous reports, where the channel width is on the order of submicrometers to several micrometers; the 2-D transport allows carriers to avoid the defect potential and bypass through unperturbed regions. Therefore, the RTS amplitude is mainly due to mobility modulation for the long CNT-FETs.

In the following, the envelope ratio of the RTS differential conductance will be studied experimentally from one of the semiconducting SWNTs, where nonballistic (diffusive) transport is present in the devices. Fig. 4(a) shows the current and (b) corresponding source–drain differential conductance (dI_{ds}/dV_{ds}) for the CNT-FET (sample 2) as a function of V_{ds} for different V_g at the temperature of 4.2 K with a V_{ds} scanning rate of 1 mV/s. The current and differential conductance spectra

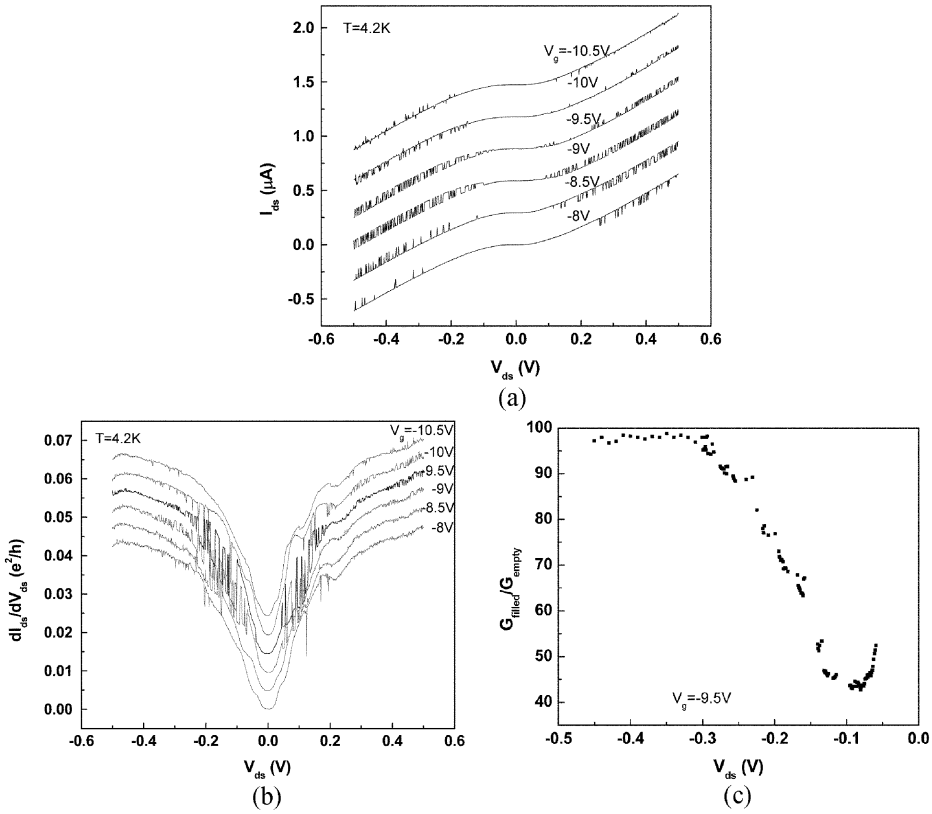


Fig. 4. (a) Current and (b) conductance of p-channel CNT-FET as function of V_{ds} for different gate biases at $T = 4.2$ K with V_{ds} scanning rate of 1 mV/s. (c) Differential conductance ratio of filled and empty states, extracted from RTS at $V_g = -9.5$ V.

show, simultaneously, the switching behavior. The curves were offset by 20% of the maximum amplitudes for clarity. The current was measured after the amplification of the signals using a standard operational amplifier, and dI_{ds}/dV_{ds} signals were obtained by a standard lock-in method with a sinusoidal *AC* voltage modulation of 1 kHz and a time constant of 300 ms. It is observed that the RTS amplitude first increases with increasing $|V_{ds}|$ until $|V_{ds}| > 0.2$ V; then, the amplitude saturates and decreases for a larger $|V_{ds}|$. Furthermore, the differential conductance ratio (the envelop ratio of differential conductance of filled state to empty state) increases to almost close to 100% for $|V_{ds}| > 0.3$ V shown in Fig. 4(c). It is known that when V_{ds} increases, the effect of longitudinal electrical field increases, so that the possibility for a hole to go through the single defect barrier increases. The differential conductance ratio shows a strong dependence on the source–drain voltage bias; which further confirms that the degradation of mobility due to the extra Coulomb repulsive scattering is the main contribution for the RTS amplitude.

For a short CNT-FET, where the length of the CNT is smaller than the carrier mean free path but larger than the Coulomb blockade length ($L_{\rm CB} < L < L_{\rm mfp}$), the ballistic transport will happen. The transmission coefficient for carriers to go through a single defect Coulomb potential is $T_{\rm defect}(E) = G_{\rm filled}(E)/G_{\rm empty}(E)$, where E is the energy of the hole in a SWNT. In this case, the charging/discharging modulates the maximum differential conductance through single transport channels, and E is directly related to the applied V_{ds}. For the nonballistic case, this transmission coefficient fluctuation could result from mobility fluctuation. However, in this case, E is much smaller than qV_{ds} due to many other scatterings.

The gate-dependent emission and capture characteristics of RTSs show that the mechanism of the observed RTSs in the CNT-FETs is similar to that of conventional MOSFETs in their origins. They are due to the trapping and detrapping of the defect centers inside the gate dielectric or in the interface of gate dielectric and CNT channels. However, the data show that the narrow channel devices are extremely sensitive to the quality of the gate oxide and its interface. RTSs are related to $1/f$ noise; CNT-FETs suffer from large low-frequency noise [15]. The $1/f$ noise performance of the devices degrades greatly when the oxide traps and interface traps are created or increased by electrical stress or radiation. Furthermore, the reliability of devices depends on the quality of 1-D nanotubes, gate dielectrics, and interfaces. Due to the ultra-small diameters of the 1-D FETs, only a few defects (1$\sim$100) are present underneath each nanotube, assuming the defect density of $10^{10} \sim 10^{12}$ cm$^{-2}\cdot$eV^{-1}; thus, the variation of the number of defects affects the device performance dramatically. Hence, a highly uniform gate dielectric free from the spurious charges and interface defects is critical. Clever device designs to minimize these spurious charge effects are equally important, and they may include the use of many nanowires (tubes), which effectively increases the channel width, and/or the use of novel architectures incorporating error correction functionality. One example may be nanowire cellular automata [16].

III. Conclusion

In summary, RTSs were studied in the single-walled CNT-FETs. The physical mechanism of the RTSs was due to the hopping/tunneling of carriers between the conducting channels of the SWNTs and the defect levels. The defects were hole-type Coulomb repulsive centers located near the valance band of the SWNTs in the energy space and at the interface and/or several nanometers underneath SWNT in the real space. The contribution of the current fluctuations is mainly due to mobility modulation, and the large amplitude of the RTSs is analyzed to be due to the small diameters of the SWNTs.

Acknowledgment

The authors would like to thank Dr. S. G. Thomas for helpful discussions.

References

[1] T. W. Odom, J. L. Huang, P. Kim, and C. M. Lieber, "Atomic structure and electronic properties of single-walled carbon nanotubes," *Nature*, vol. 391, pp. 62–64, 1998.

[2] M. H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, and P. Yang, "Room-temperature ultraviolet nanowire nanolasers," *Science*, vol. 292, pp. 1897–1899, 2001.

[3] D. Zhang, C. Li, S. Han, X. Liu, T. Tang, W. Jin, and C. Zhou, "Electronic transport studies of single-crystalline In2O3 nanowires," *Appl. Phys. Lett.*, vol. 82, pp. 112–114, 2003.

[4] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and P. Avouris, "Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys. Lett.*, vol. 80, pp. 3817–3819, 2001.

[5] F. N. Hooge, "$1/f$ noise is no surface effect," *Phys. Lett.*, vol. 29A, pp. 139–140, 1969.

[6] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van derWel, G. Hoogzaad, E. van Tuijl, and B. Nauta, "Intrinsic $1/f$ device noise reduction and its effect on phase noise in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 9, pp. 1022–1025, Sep. 1999.

[7] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 331–343, Feb. 1996.

[8] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, "Discrete resistance switching in submicrometer silicon inversion layers: Individual interface traps and low-frequency ($1/f$?) noise," *Phys. Rev. Lett.*, vol. 52, pp. 228–231, 1984.

[9] F. Liu, M. Q. Bao, H. J. Kim, K. L. Wang, X. L. Liu, C. Li, and C. W. Zhou, "Giant random telegraph signals in the carbon nanotubes as a single defect probe," *Appl. Phys. Lett.*, vol. 86, pp. 163102-1–163102-3, 2005.

[10] J. Kong, H. T. Soh, A. M. Cassell, C. F. Quate, and H. J. Dai, "Synthesis of individual single-walled carbon nanotubes on patterned silicon wafers," *Nature*, vol. 395, pp. 878–881, 1998.

[11] S. Suzuki, C. Bower, Y. Watanabe, and O. Zhou, "Work functions and valance band states of pristine and Cs-intercalated single walled carbon nanotube bundles," *Appl. Phys. Lett.*, vol. 76, pp. 4007–4009, 2000.

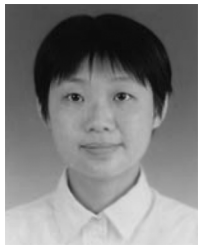
[12] M. B. Weissman, "$1/f$ noise and other slow, non-exponential kinetics in condensed matter," *Rev. Mod. Phys.*, vol. 60, pp. 537–572, 1988.

[13] H. Ahmed, M. Pepper, and A. Broers, *Transport in Nanostructure*. Cambridge, MA: Cambridge Univ. Press, 1997, p. 67.

[14] M. J. Kirton, M. J. Uren, S. Collins, M. Schulz, A. Karmann, and K. Scheffer, "Individual defects at the Si:SiO_2 interface," *Semiconduct. Sci. Technol.*, vol. 4, pp. 1116–1125, 1989.

[15] P. G. Collins, M. S. Fuhrer, and A. Zettl, "$1/f$ noise in carbon nanotubes," *Appl. Phys. Lett.*, vol. 76, pp. 894–896, 2000.

[16] Y. Cui and C. M. Lieber, "Functional nanoscale electronic devices assembled using silicon nanowire building blocks," *Science*, vol. 291, pp. 851–853, 2001.



Fei Liu (S'05) received the B.S. degree in electronic engineering from Tsinghua University, China, in 2002, and the M.S. degree in electrical engineering from University of California, Los Angeles, in 2004. She is currently pursuing the Ph.D. degree in electrical engineering at University of California.

Her research interests include variability issues and metrology in the nanodevices.

Kang L. Wang (M'66-F'91) received the B.S. degree from National Cheng Kung University, China, in 1964, and the M.S. and Ph.D. degrees from the Massachusetts Institute of Technology (MIT), Cambridge, in 1966 and 1970, respectively.

From 1970 to 1972, he was an Assistant Professor at MIT. From 1972 to 1979, he worked at the General Electric Corporate Research and Development Center as a Physicist/Engineer. In 1979, he joined the Electrical Engineering Department, University of California, Los Angeles (UCLA), where he is a Professor. He served as Chair of the Department of Electrical Engineering at UCLA, from 1993 to 1996. He also serves as the Director of the Marco Focus Center on Functional Engineered Nano Architectonics-FENA, an interdisciplinary research center. He was also named the Director of the newly established Western Institute of Nanoelectronics (WIN)—a coordinated multiproject research institute with UC Los Angeles, Stanford University, UC Berkeley, and UC Santa Barbara. His research interests include semiconductor nanodevices and nanotechnology; self-assembly growth of quantum structures and cooperative assembly of quantum dot arrays; Si-based molecular beam epitaxy, quantum structures, and devices; nanoepitaxy of hetero-structures; spintronics materials and devices; electron spin and coherence properties of SiGe and InAs quantum structures for implementation of spin-based quantum information; and microwave devices. He has held more than 15 patents and has published over 300 papers.

Dr. Wang has received many awards, including Guggenheim Fellow; TSMC Honor Lectureship Award; Honoris Causa at Politechnico University, Torino, Italy; Semiconductor Research Corporation Inventor Awards; a European Material Research Society Meeting Best Paper Award; and a Semiconductor Research Corporation Technical Excellence Achievement Award. He serves on the editorial board of the *Encyclopedia of Nanoscience* and *Nanotechnology* (New York: American Scientific).

Chao Li received the Ph.D. degree from the University of Southern California, Los Angeles, in 2005.

She has done extensive work on the synthesis and nanoelectronic applications of nanowires and carbon nanotubes. In addition, she has also worked on the chemical and biosensing applications of nanowires and nanotubes, including the detection of a prostate-specific antigen. She has published over 30 papers in peer-reviewed journals, and her work has been reported by *Physics Today*, *MRS Bulletin*, American Institute of Physics, National Science Foundation, National Cancer Institute, and the Royal Society of Chemistry. She is currently a Process Engineer at Atomate Corporation, Santa Barbara, CA.

Chongwu Zhou received the Ph.D. degree from Yale University, in 1999.

From 1999 to 2000, he worked as a Postdoctoral Fellow at Stanford University, Stanford, CA. In 2000, he joined the faculty at University of Southern California, Los Angeles, where he currently holds an Associate Professor position in the Department of Electrical Engineering—Electrophysics. His current research interests include the synthesis and device applications of nanowires, carbon nanotubes, and molecular wires. He has published over 60 scientific papers in prestigious journals. His work has received approximately 3000 citations and has been reported by *Scientific American*, *Physics Today*, *MRS Bulletin*, and *Science*.

Dr. Zhou has received many awards, including an National Science Foundation CAREER Award, in 2002, and a National Aeronautics and Space Agency TGiR Award.