Emerging Memory Devices

Nontraditional Possibilities Based on Nanomaterials and Nanostructures

With MP3 player capacity at more than 60 GB, digital camera memory surpassing 1 GB, and standard personal computers boasting over 1 GB random access memory (RAM), the old Commodore 64s (64 KB RAM) and 3 1/2-in floppy drives (1.44 MB) make us wonder how did we ever survive? New memory technologies such as FLASH have had a huge impact on consumers, as have traditional static RAMs (SRAM) and dynamic RAMs (DRAM). But the main culprit of the continual technological revolution is by far scaling.

SRAM stores data in flip-flops that are made up of four to six transistors. SRAM is fast and does not require frequent refreshing, but it does take up valuable Si real estate. It is considered the fastest RAM available and is usually employed as an on-chip cache. DRAM, on the other hand, is made up of one transistor and one capacitor but requires refreshing to maintain capacitor charge. Fewer elements mean more memory per unit chip area. Today's popular breed of DRAM, known as synchronous DRAM (SDRAM), is found in most computer systems as primary memory storage. SDRAM can run at much higher clock speeds than conventional memory as it synchronizes itself with the CPU's bus. The DRAM market in 2004 was worth over US$26.8 billion, coming close to the lucrative microprocessor market at US$30.5 billion. Catching up fast, at a market value of US$15.6 billion in 2004, is the popular FLASH (NAND)-based memory, aggressively dominating the memory market in growth. Toshiba Corp. developed the first NAND FLASH as a solid-state replacement for magnetic memory. FLASH is made up of one transistor with a specially engineered floating gate that maintains charge states. The FLASH revolution has enabled consumers to enjoy the pleasures of portable MP3 players and digital cameras with abundant storage. Growth in each memory sector is expected to increase well into 2008. The International Technology Roadmap for Semiconductors (ITRS) and the Semiconductor Research Corporation (SRC) Memory Task Force reports such growth rates cannot be sustained due to scaling issues.

Exotic solutions such as three-dimensional integration, stacking [1], distributed memory, processor in memory (PIM), memory in processor (MIP) [2], [3], and other new architectures being reported in the literature may somewhat sustain Moore's law for memory beyond 2008 based on existing

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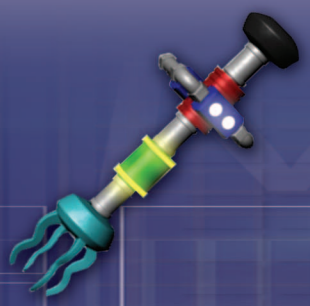

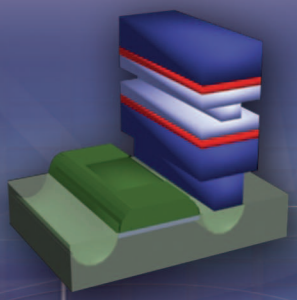

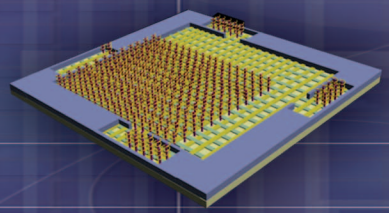

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memory devices. To make true leaps in sustaining memory growth, industry and academia are searching for new and novel memory devices. Numerous emerging memory devices based on nanomaterials and nanostructures have been well identified by the ITRS [4], the SRC Memory Task Force [5], and the European Roadmap for Nanoelectronics [6]. In an effort to collate possible memory device alternatives, the ITRS Roadmap identifies six emerging research memory areas beyond traditional RAM and FLASH devices. These include phase change memory, floating body DRAM, nano floating gate memory, single electron memory, insulator resistance change memory, and molecular memory, which are also positively reviewed in [7]. In addition, there have been various review papers [8]–[15] comparing and investigating alternative memory devices that include ferroelectric RAM, magnetic RAM, organic RAM, CNT electromechanical nonvolatile memory, programmable metallization cell (PMC) memory, magnetic tunneling junctions (MTJ) RAM, and thyristor RAM.

> SRAM is fast and does not require frequent refreshing, but it does take up valuable Si real estate.

Each memory type provides its unique advantages and challenges. However, for the "next" memory device to be considered as a silver bullet solution it would need to possess the following attributes: 1) fast access time, 2) nonvolatility, 3) infinite read/write cycles, 4) low power, and 5) a wide operating temperature range. From a manufacturing perspective, additional attributes are also required such as 6) scalability, 7) low cost, 8) manufacturability, 9) variability (of nanodevice feature size), and 10) integration ability with the Si platform. At this time, the silver bullet solution to this wish list is still unknown. As we delve further into the nanoregime, we are presented with ever-increasing material options, processes, and fascinating mechanisms never before made possible.

In an attempt to merge the unprecedented opportunity of nanotechnology with the industry's imminent scaling and power dissipation challenges, the Center on Functional Engineered Nano Architectonics (FENA), sponsored by the Semiconductor Industry Association (SIA), Semiconductor Equipment and Materials International (SEMI), and the Department of Defense (managed by DARPA), aims to engineer nontraditional memory alternatives based on nanomaterials and structures that may go beyond existing CMOS memory devices. Nanomaterial engineering provides opportunities that have never before been possible such as the ability to self-assemble, develop controlled composite nanomaterials, and manipulate alternative state variables. Such attributes should also translate into simplified production with dramatically reduced costs. This article will provide a taste of the exotic and nontraditional memory possibilities that have emerged from the FENA Center.

EMERGING MEMORY DEVICES

The list of emerging memory devices and concepts based on novel nanomaterials and nanostructures developed by FENA is presented in Table 1. The table includes memory concepts that are the outcomes of FENA's devices, nanomaterials, nanostructures, and computational research. We present the new memory devices together with data on current devices such as DRAM, which represents the largest volatile memory market, and FLASH, which represents the largest solid-state nonvolatile memory market. The table presents both demonstrated values (in bold and brackets) and projected parameter

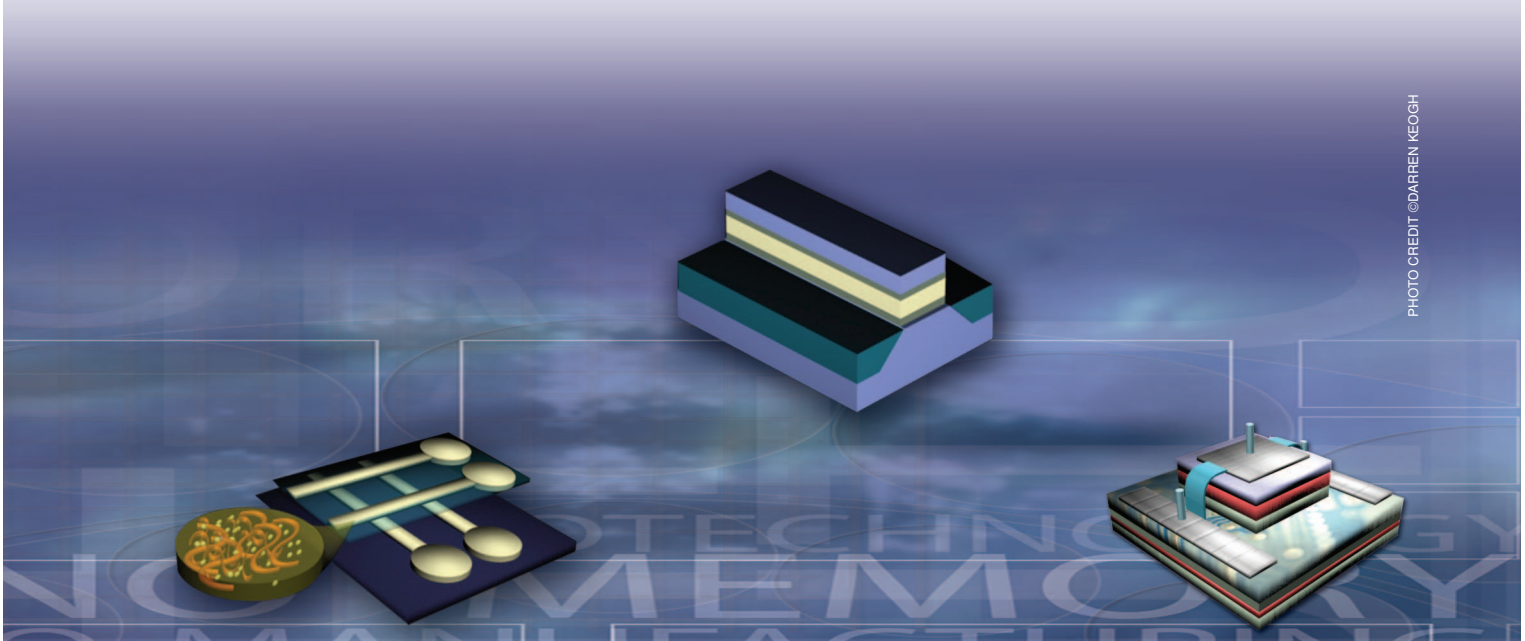
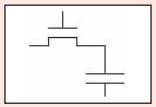
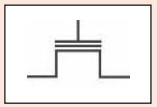
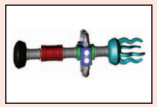
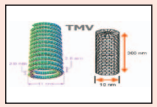
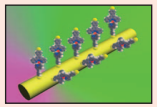
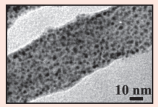
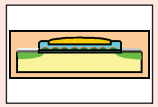
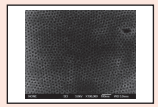
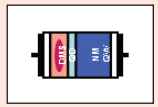


Table 1. Projected/experimental parameters of FENA emerging research memory devices.

Storage Mechanism	Present-Day Baseline Technologies (Taken from ITRS 2005 Edition)		Moleculer–Based Memories							
			Rotaxane Memory (F. Stoddart and W. Goddard	Virus Memory (Y. Yang and C. Ozkan)	Nanowire Memory (C. Zhou)	Polymer Memory (R. Kaner and Y. Yang)	Single Electron Memory (J. Liu)	Phase-Charge RAM (Y.H. Xie)	Spin Memory (K.W. Kim)
									
Device Type, Material Used	Standalone DRAM (2005) 80-nm node	NOR Flash-(2005) 130-nm node	Rotaxanes or Catenanes	Protein Virus Nanowires with Platinum Nanoparticles	Nanowires; In_2O_3, Si with Redox Active Molecules	Polyaniline Nanowires with Au Nanoparticles	Floating Gate Using $CoSi_2$/Si Hetero-Nanocrystals	GeSbTe Templated Self-Assembled PS-PI Block Copoly.	Spin State Variable Using High Temp DMS
Read Time	**(<15 ns)**	**(14 ns)**	~ns	—	<80 ns	~25 ns	<80 ns	<50 ns	<80 ns
Write Time	**(<15 ns)**	**(1 μS)**	~μS	~1 μs	**(~25 ns)**	~25 ns	**(~0.4 μS)**	<50 ns	~1 ns
Retention Time	**(64 ms)**	>10 years	**(minutes)**	**(days)**	**(600 hours)**	**(weeks)**	10–20 years	>10 years	>years
Write Cycles	Infinite	**(>100,000)**	~100 **(<35)**	~1,000	**(~1,000)**	**(>10,000)**	>100,000	>1 billion	>100,000
On/Off Ratio	**(<10,000)**	**(<10,000)**	**(~2 – 11)**	<10,000 **(~1000)**	**(~10,000)**	**(~1000)**	~10,000	>100	Unknown
[a] Scalability ceil size in μm^2	32 nm Node $6F^2$ ≈ 0.0061	45 nm Node $10F^2$ ≈ 0.021	**(0.007 μm^2)** <0.0001 μm^2	**(0.01 μm^2)** <0.0001 μm^2	<0.0001 μm^2	**(0.04 μm^2)** <0.0001 μm^2	**(1 μm^2)** <0.0011 μm^2	~0.04 μm^2	<0.0001 μm^2
Limiting Scaling Factor	High-k Material	Oxide Thickness	Molecule Stability and Self-Assembly Variability	Variability of Metal Particle Size and Density	Molecule Stability and Self-Assembly Variability	Variability of Metal Particle Size and Density	Dot Density Fluctuation	Density Limited by Thermal Proximity Effect	Curie Temp of DMS
General Advantages	High Density, Economical	Nonvolatile	Ultra High Density	Low Cost, High Density, Bio Compatible	Low Cost, Flexible, High Density	Low Cost, High Density, Fast	High Density, CMOS Compatible	Nonvolatile, Stable, Scalable	High Density, Low Power, Scalable
Challenges	Scaling, Gate Leakage, Capacitor Formation	Scaling, Oxide Thickness, Power Dissipation	Speed, Stability, On/Off Ratio, Temp Influence	Material Stability Integration, Scaling	Integration and Material Stability	Material Stability, Integration, Temp Influence	Dot Density Fluctuation, Scaling	Large Write Current, New Materials and Process	Material, High Curie Temp
Fabrication Technique	Lithography	Lithography	Litho and Self-Assembly	Self-Assembly, Wet Synthesis	Litho and Self-Assembly	Self–Assembly, Wet Synthesis	Litho and Self-Assembly	Polymer Template and Litho	Litho

[a] *Cell Size* = αF^2, where α is the cell size factor and F is the half pitch node. DRAM cell size is 8 F^2 and 10 F^2 for NOR Flash. The nodes and years (DRAM – year 2013, NOR Flash – 2010) were selected as the first "red bricks" appear indicating manufacturing solutions are presently NOT known (*ITRS* 2005 Edition, Process Integration Devices and Structures Section, pp. 31 and 34).

values (normal). Advantages and key challenges are also highlighted together with the corresponding fabrication methods. Each type of memory will be described.

> DRAM is made up of one transistor and one capacitor but requires refreshing to maintain capacitor charge.

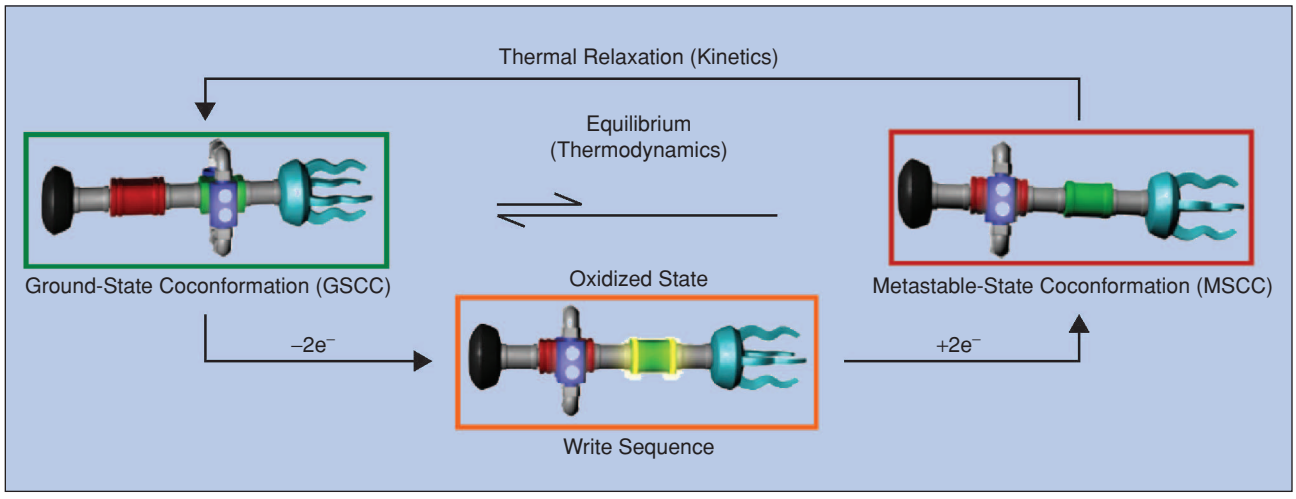
MOLECULAR MEMORY

The ITRS [4] has identified molecular-based memory as an emerging technology, utilizing molecular-level components, which promises the ultimate dimensional limit for memory. Integration of the components into memory devices typically involves molecular assembly, rather than patterning two-dimensional semiconductor surfaces with doped regions. Hence, molecular electronics rely on assembly from the bottom up.

Bistable electrochemically switchable catenanes and rotaxanes [16]–[18] form a recent class of molecules successfully used for molecular memory. Their ON and OFF states can be distinguished by a 300–1,000% difference in current between two Si nanowires, and the half-life of the ON state in the device environment is ~15 min. Since the mechanical motion is an activated redox process, these devices exhibit a well-defined, hysteretic current-voltage response. As shown in Figure 1, in the OFF (ground) state, the tetracationic cyclobis (paraquat-*p*-phenylene) ring ($CBPQT^{4+}$) encircles the electron-rich tetrathiafulvalene (TTF) unit (green). Oxidation of the TTF unit produces its dication (TTF^{2+}), which results in coulombic repulsion of the $CBPQT^{4+}$ ring to the neutral dioxynaphthalene (DNP) site (red). A two-electron reduction of the TTF^{2+} back to its neutral form results in a metastable ON state in which the $CBPQT^{4+}$ has not yet returned to the more favorable TTF station. Appropriate modification of the molecular structures and elements may be designed to change the switching kinetics and thermodynamics for different memory applications and to interface the molecules with a vast array of device platforms, such as Si surfaces, carbon nanotubes, nanowires, metal oxides, or other desired materials. More recently, these molecules have been demonstrated in a 64-b crossbar array on Si electrodes [19]. The advantages of molecular-based memory devices are their low power consumption, self-assembly (low cost), and true molecular size allowing for ultimate density. Challenges such as temperature sensitivity, molecular stability, speed, and reliability still require further attention.

A well-known method of achieving a memory effect is to employ redox-active elements. As with the catenane and rotaxane material systems, the redox mechanism involves electrons being transferred from one element to another such that a donor element gives up an electron (oxidized) to an accepting element (reduced). This process usually requires an external stimulus, such as an electric field or change in temperature, that will provide energy for electron detachment from its host (donor) to trigger an on-demand redox reaction. The benefit of fusing this operating principle with nanomaterials opens the door to fast, stable, and high-performance memory devices. In addition to catenanes and rotaxanes, FENA researchers are investigating redox memory based on conductive polymer nanowires [20], functionalized nanowires, and carbon nanotubes [21]–[23].

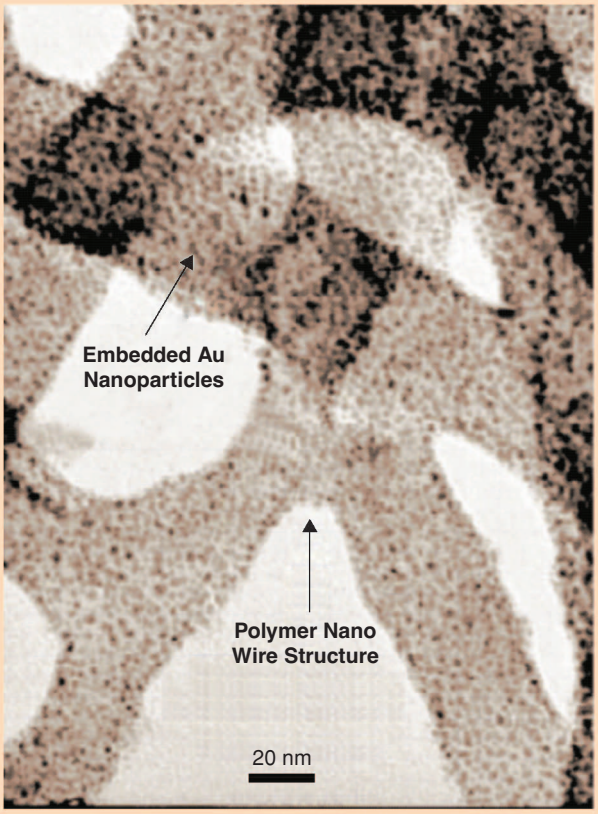
Conductive polymers are suited for high-volume manufacturing as they can be formed into thin films for large areas. Our unique material engineering comes about by forming polyaniline into controllable nanowires with blended gold nanoparticles, as shown in Figure 2(a). The nanowires have an average diameter of 30 nm, and the embedded gold particles are less than a few nanometers in diameter. Charge is stored in the metal particles provided by donor molecules within the polymer that enables the memory effect. Simple fabrication techniques such as spin on and electrode patterning make this device extremely simple and potentially low cost, as illustrated in Figure 2(b). In this system, the memory effect is a result of the electric-field-induced



1. The rotaxane molecule consists of two separate interlocked components which are not covalently bonded but linked via mechanical bonds. (Figure courtesy of the laboratories of F. Stoddart at UCLA.)

charge transfer between polyaniline nanowires and gold nanoparticles such that electrons are transported from the imine nitrogen of the polyaniline to the polyaniline/gold interface. The mechanism does not require a continuous current, which makes this a stable, nonvolatile memory device with retention times demonstrated beyond several days with an on/off ratio >1,000. The retention time of the memory is determined by the charged gold nanoparticles slowly discharging (relaxing) back into the polyaniline nanowire. More research is required to understand this mechanism to enable optimization of nanomaterial to minimize nanoparticle charge decay. Although advantages such as nonvolatility and low cost are evident, further investigation is required into the materials' stability and temperature influence, which often plague polymer/organic-based devices.

> Each memory type provides its unique advantages and challenges.



2. TEM image and device structure. (a) TEM image of the polyaniline nanowire/gold nanoparticle composite. The black dots are 1-nm gold nanoparticles contained within 30-nm diameter polyaniline nanowires. (b) The structure of the polyaniline nanowire/gold nanoparticle bistable memory device. (Figure courtesy of the laboratories of R.B. Kaner and Y. Yang at UCLA.)

Going beyond the traditional bistable memory, we are also exploring possibilities for multilevel memory devices based on redox-active molecules containing multiple redox centers that are fabricated on a nanowire backbone. A challenge in developing multilevel memory devices is the need to include additional charge-sensing circuitry to detect the various memory levels. Our research has tackled both challenges by employing functionalized nanowires that offer high surface area to allow self-assembled packing of iron-terpyridine redox molecules for high stability and maximum storage density. Figure 3 shows a simple memory device that can be programmed into eight levels. The nanowire-based memory has been demonstrated with on/off ratios exceeding 10,000 and retention times greater than 600 h. Similar to the polymer-based memory, it is believed the retention time is a function of the charge relaxation from the iron-terpyridine redox molecules back into the nanowires. Our memory utilizes a small active area of 0.02 μm^2 (2-μm channel length by 0.01-μm nanowire width). Such a small active area designed with the appropriate cell may achieve a super-high b/cm^2 density as 8 b/cell would be used.

Other than polymer-based materials, novel memory devices are also being developed for bio-based information processing. As a first, we have achieved a biomemory device derived from the tobacco mosaic virus (TMV) nanowires coated with Pt nanoparticles measuring 10 nm [24]. The device is fabricated via a simple solution process with an active composite layer sandwiched by two Al electrodes. Figure 4(a) shows a TEM image of the TMV nanowire with ordered platinum nanoparticles, and Figure 4(b) shows the I–V memory characteristics and device structure. The memory effect is a result of charge trapping in the nanoparticles for the ON state and tunneling process in the OFF state. Our preliminary results have shown an ON/OFF ratio greater than 10^3. Such results of exotic bionano fusion open doors to future applications and devices that will help embrace information processing in the bionano regime.

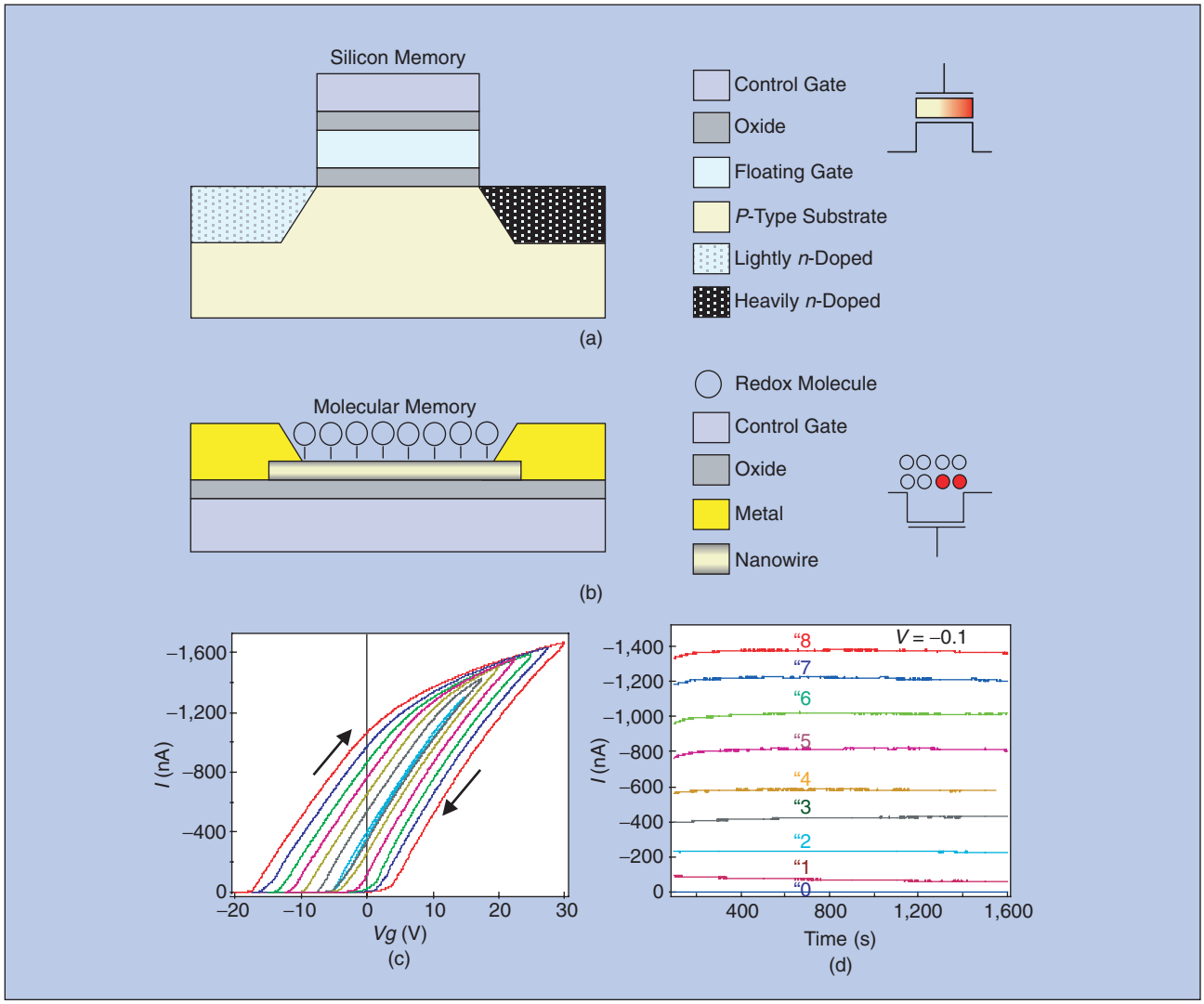
SPIN-BASED MEMORY

Magnetic materials show some promise in enabling the semiconductor industry to move to very small cell sizes. A great deal of media and research activity has been focused in this area, particularly on magnetic RAM (MRAM) [25]–[27].

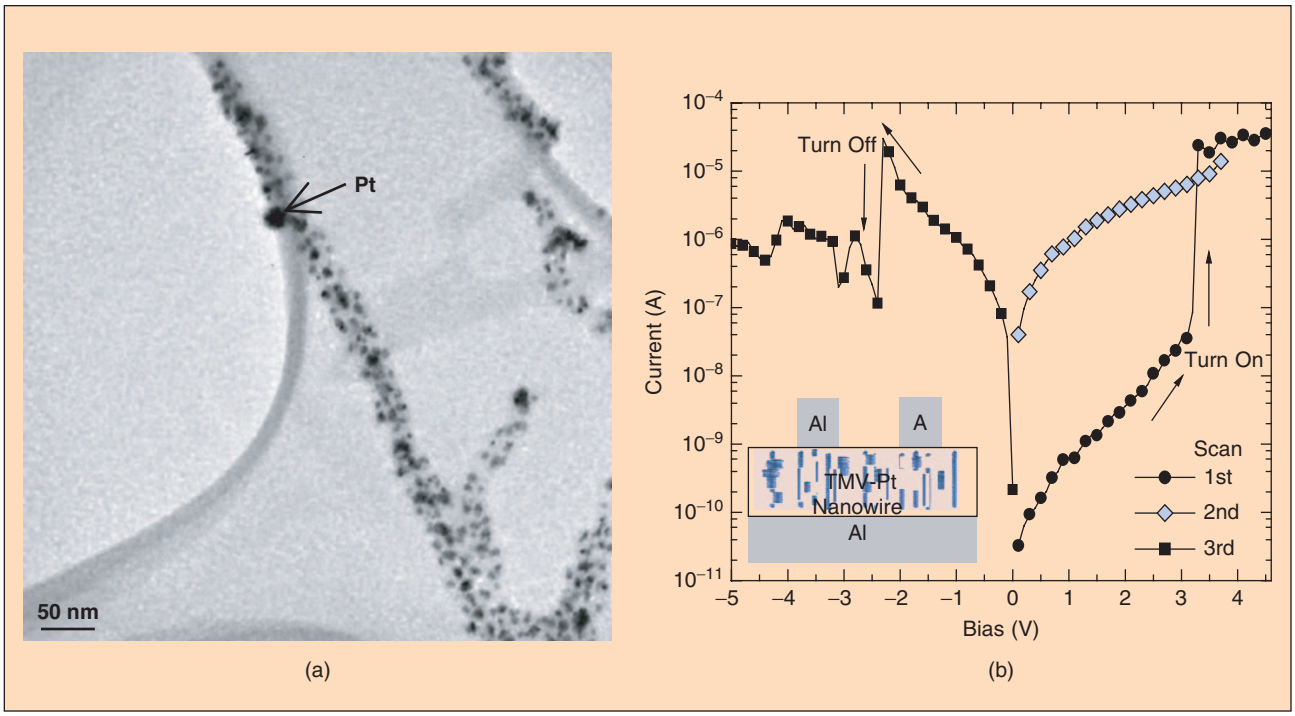
Spintronics enable information representation to be based on angular spin momentum rather than electron charge. It is hoped that by employing spin as a state variable, power dissipation could be dramatically reduced. The challenge rests in developing a spin-based memory cell that can be integrated on a Si substrate. Dilute magnetic semiconductors (DMSs) provide a path to such an ambitious task. One interesting spin memory device proposed [28]–[30] is the bistable double-quantum well structure mediated by a magnetic phase transition as presented in Figure 5. A gate electrode is also needed to control the hole transfer between the quantum device (QD) and the reservoir.

The ITRS has identified molecular-based memory as an emerging technology.

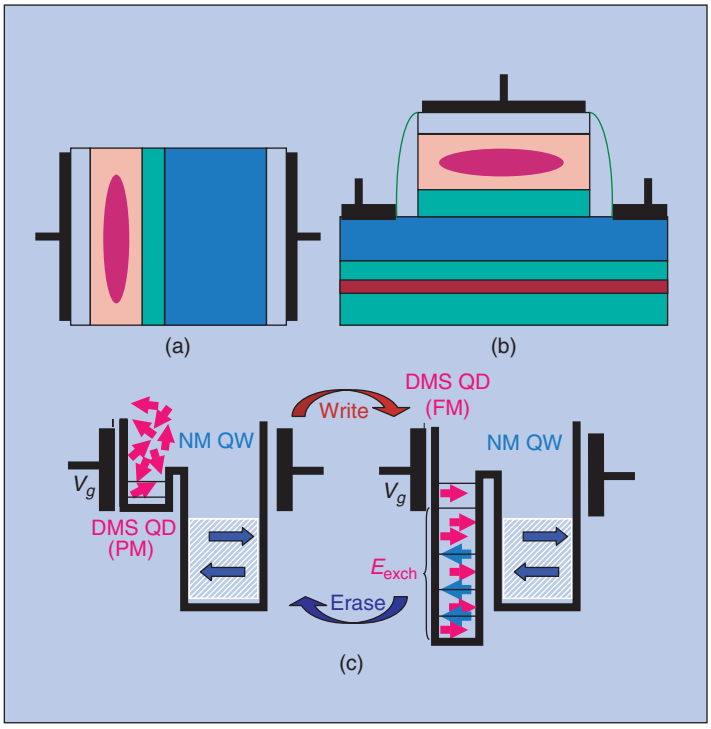
The basic operating principle is as follows: The DMS QD can be prepared initially in a paramagnetic (PM) state by depopulating holes through proper bandgap engineering with the neighboring reservoir and barriers. When a proper bias is applied to the gate electrode, holes from the reservoir can be transferred to the DMS QD via tunneling or overbarrier injection. As the hole density in the DMS QD surpasses a certain threshold, the layer undergoes a PM to ferromagnetic (FM) transition, thus writing the spin memory. When a reverse bias pulse is applied, the holes are drained out of the FM DMS QD into the reservoir and the DMS will return to the PM state, thus erasing the spin memory. Owing to the insulating barrier



3. Schematic diagram compares design and operation for a conventional silicon FLASH memory and the proposed molecular memory for multilevel nonvolatile data storage. (a) Schematic of a silicon FLASH memory, (b) schematic of the proposed molecular memory, and (c) I-V_g hysteresis loops obtained by sweeping gate voltage from $-n*2.5$ V to $10+n*2.5$ V and then back to the starting value. n is the index of levels from 2 (the innermost curve) to 8 (the outermost curve). (d) Current recorded over time after the device was written into states 0 (the bottom curve) to 8 (the top curve). Little degradation in the stored signal was observed over 1,500 s with a source-drain bias of V = –0.1 V. (Figure courtesy of the laboratories of C. Zhou at USC.)



4. (a) TEM image of TMV nanowire with ordered platinum nanoparticles. Pt nanoparticles of size 10–15 nm are uniformly attached at the surface of the virus wire. (b) I–V characteristics of TMV memory device. Forward bias scan shows the device turn-on at 3.1 V and reverse scan indicates that the device turns off at −2.4 V. The inset shows the schematic device structure with active layer of dispersed Pt nanoparticles functionalized TMV nanowires. [Figure courtesy of the laboratories of Y. Yang (UCLA) and C. Ozkan (UCR).]



5. Nonvolatile spin memory device. (a) Schematic diagram consisting of a DMS QD and a nonmagnetic (NM) QW (hole reservoir) separated by a barrier layer. (b) Suggested layout in the pillar form for easy read-out. (c) Operating principle of the nonvolatile spin memory device. Hole-mediated PM (left; 0) to FM (right; 1) transition in the DMS QW can be controlled by the gate bias V_g, and the exchange interactions (E_{exch}) give rise to the desired nonvolatility by strongly confining the holes in the FM DMS QD. (Figure courtesy of the laboratories of K.W. Kim at North Carolina State University.)

between the gate electrode and the active memory region, the write/erase current should be very low. Another advantage is its scalability, which is potentially down to a few hole levels by reducing the size of the DMS QD. Moreover, the FM-PM transition in the DMS QD can be readily detected by a variety of techniques that are also potentially scalable. Preliminary calculations indicate a robust window of operation in the system parameter space where the bistability is possible even in scaled devices [28]–[30]. Estimations of its lifetime also predict the feasibility of room-temperature operation once the critical temperature for the phase transition can be sufficiently improved. Hence, a key step is to develop DMS materials with a Curie temperature that is substantially higher than room temperature.

NOVEL FLOATING GATE MEMORY

A floating gate device is a modified MOS transistor that has an additional electrically isolated gate, called a floating gate, that lies below the standard control gate and above the transistor channel. The floating gate memory device stores information by holding electrical charge within the floating gate. Adding or removing charge from the floating gate changes the threshold voltage of the cell, thereby defining whether the memory cell is in a programmed or erased state. Much research interest is being focused on improving and optimizing the floating gate sandwich consisting of the floating gate (usually polysilicon), insulating material

(usually SiO_2), and control gate (usually a metal). The design of this sandwich is of great interest as it directly affects the speed (R/W time) and nonvolatility (retention time) of the memory cell. To maximize these parameters, the silicon nanocrystal floating gate is replaced by the $TiSi_2$/Si hetero-nanocrystal gate. The deep quantum well in $TiSi_2$ and the additional barrier of Si allow significantly prolonged retention characteristics. This also provides more charge sites for tunneling electrons through the oxide. However, concerns such as a nanocrystal reaction with oxides, thermal stability (during annealing), and defects hamper the device performance. FENA research has shown promising results in employing hetero-nanocrystals of $TiSi_2$ that overcome challenges plagued by other heteronanocrystal-based memory [31], [32]. The charge-loss rate in the $TiSi_2$/Si device is ten times less than that of a Si dot device, and we have found that the device has a wider memory window than the Si dot counterpart. This may be because an additional barrier of Si and a deep well of $TiSi_2$ exist, resulting in the stored charge finding it that much more difficult to leak. Figure 6 shows the structure of our heterostructure floating gate.

PHASE CHANGE MEMORY

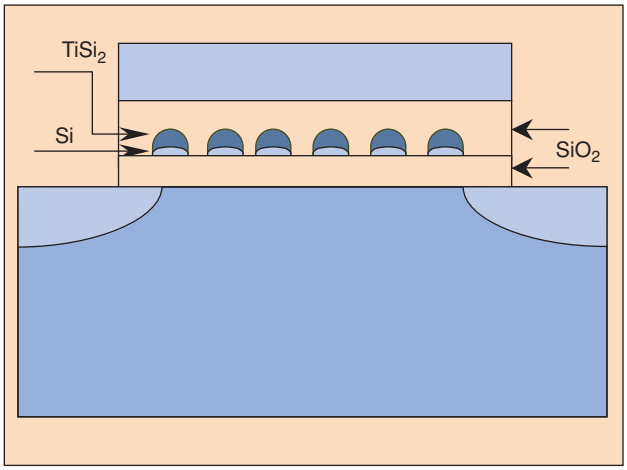
Another memory alternative pursued by major chip manufacturers including Intel and Samsung is phase-change RAM (PRAM) [33], [34]. The operating principle is based on phase-change materials that can reversibly switch between crystalline and amorphous phases through thermal processes, resulting in a change in electrical resistivity. To switch from crystalline to amorphous, a short 10–20 ns pulse at about 2–4 V is applied, while from amorphous to crystalline, a pulse of 50–100 ns at 1–2 V is used to anneal the material.

Current R&D efforts in PRAM technology focus on lowering reset current, increasing the set/reset speed, and understanding the failure mechanisms of the device which include being stuck in one of the two states [33]. Recent progress in this field such as R_{high}/R_{low} ratios of 100–1,000 and the reset current at 0.2 mA [35] have been achieved.

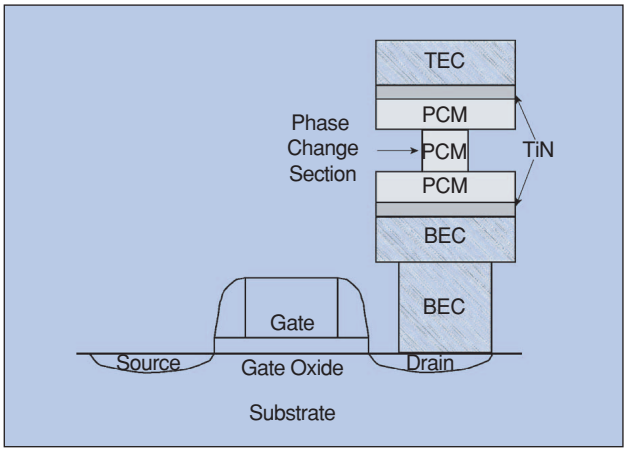
We have identified a novel PRAM device structure [36] that allows the resistance and the power needed for the reset operation to be controlled independent of one another, as presented in Figure 7. Such a device geometry offers greatly expanded design flexibility. The power minimization consideration calls for the PRAM device structure to be in the nanometer dimension. Our advances have resulted in devising a novel structure with unique features so that the phase change material undergoes the set/reset process in maximum isolation with little contact from other materials to reduce alloying induced device failure. We are conducting experiments aimed at understanding the microstructural evolution by observing the set/reset process in the nanoscale volume of the PCM using real-time in situ TEM of materials such as chalcogenide alloys. Diblock copolymer patterning is employed for device fabrication in the nanometer range; an example template used to fabricate our PRAM structures is shown in Figure 8. This templating method has been developed by FENA and is now applied to various applications such as PRAM.

DISCUSSION AND CONCLUSIONS

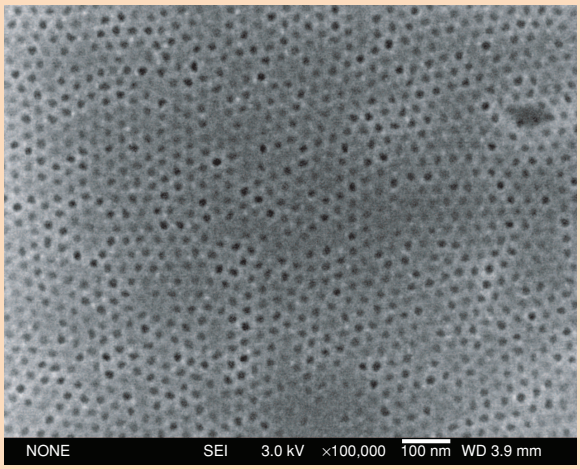
Each memory device presented has its unique range of advantages and challenges, which are summarized in Table 1. DRAM and FLASH have radically different characteristics; hence, they are used for different applications. Accordingly, the search for memory devices beyond CMOS comes with an important caveat: different memory for different applications. For example, the hybrid memory approach based on TMV may hold promise for a high-throughput neural network, even though cell size and speed are slower than today's CMOS-based memory devices. In most cases, independent of the application, memory device evolution follows Moore's law in increasing storage capacity (b/cm^2). One way of achieving this is to reduce the physical dimensions of the cell. Increasing cell functionality is another



6. Hetero-nanocrystal memory device made up of $TiSi_2$/Si resulting in charge loss ten times less than conventional Si dot devices. (Figure courtesy of the laboratories of J. L. Liu at University of California at Riverside.)



7. Schematic drawing of the novel PRAM cell geometry. The section of the PCM that undergoes phase change has the smallest cross-sectional area and is in contact only with the same PCM, not with other materials such as the bottom electrode contact (BEC) and the top electrode contact (TEC). U.S. patent pending. (Figure courtesy of Y.H. Xie laboratories at UCLA.)



8. Nanometer holes transferred from self-assembled PS-PI to Si_3N_4 on Si (001) substrate used to fabricate the PRAM devices. This method was developed by FENA. (Figure courtesy of the laboratories of Y.H. Xie at UCLA.)

way. If we were to continue scaling and reducing cell size, our future path towards high-density memory would be made up of cells with several atoms or a cluster of molecules, similar to the presented rotaxanne and catenane molecules. The major limitation would be the nanodevice footprint or the pitch of nanowiring used for device connection, which would probably depend on the lithography process. The same limitation would also apply for most of the redox-based memories presented such as the nanowire memory, TMV memory, and polymer memory. However, this may not be the only factor as the ITRS 2005 edition indicates "we are now in a new era in which there are multiple significant drivers of scaling," and as such, the "technology node." The technology node, which was defined as the smallest half-pitch of contacted metal lines, is no longer used as a simple indicator of overall industry progress in integrated circuit feature scaling. In this spirit, Figure 1 highlights the unique limiting factors of scaling beyond already identified restrictions such as the smallest patternable footprint.

Increasing b/cm^2 by increasing functionality has also been shown to be possible, similar to the multilevel memory device presented in Figure 3. The key is to engineer stable charging sites over a wide enough temperature range without compromising on/off ratios that may increase bit errors. Other state variables such as material-phase change and spin-based memory offer possibilities beyond charge-based memory. Phase change holds great promise as its speed, stability, and power consumption have improved. It's indeed a viable manufacturable memory technology, but it is primarily limited due to thermal proximity effects. Spin-based memory is also of great importance. MRAM has been a great success story as it combines nonvolatility, endurance, and speed. By further harnessing and understanding spin and magnetic-phase transitions based on our proposed double-quantum well structures, we aim to increase speed and density even further while reducing power dissipation by leveraging spin as a state variable rather than electron charge.

So far, there seems to be no clear winner that can compete with either DRAM or FLASH memory devices. We may find ourselves in a situation where the ultimate memory device may turn out to be a hybrid structure in which more than one technology is integrated heterogeneously over Si substrates similar to the CMOL concept invented by Likharev [37], [38]. However, some observations are clear. Devices based on new materials will create various challenges to Si integration and manufacturing. Furthermore, new nanostructures, such as nanowires, viruses, and nanotubes, combined with new assembly processes such as self-assembly and bio/polymer templating, offer compelling advantages that may soon be employed in manufacturing processes but still must show improved variability, stability, and specificity characteristics. Although the related high-volume manufacturing aspects of such materials/devices exceed the scope of this article, these aspects should be identified and investigated as part of the fundamental research studies of emerging memory devices. Manufacturing feasibility with lower costs and higher yields determine semiconductor companies' ability to market the devices and improve performance, reliability, and integration. FENA's research path will continue to focus on improving our presented memory devices, and integrating with logic elements, while exploring other emerging memory devices based on nanomaterials, nanostructures, and the next generation of low-cost assembly techniques.

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