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Novel Nanotube-on-Insulator (NOI) Approach toward Single-Walled Carbon Nanotube Devices

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ABSTRACT

We present a novel nanotube-on-insulator (NOI) approach for producing high-yield nanotube devices based on aligned single-walled carbon nanotubes. First, we managed to grow aligned nanotube arrays with controlled density on crystalline, insulating sapphire substrates, which bear analogy to industry-adopted silicon-on-insulator substrates. On the basis of the nanotube arrays, we demonstrated registration-free fabrication of both top-gated and polymer-electrolyte-gated field-effect transistors with minimized parasitic capacitance. In addition, we have developed a way to transfer these aligned nanotube arrays to flexible substrates successfully. Our approach has great potential for high-density, large-scale integrated systems based on carbon nanotubes for both micro- and flexible electronics.

Since discovered by Ijima in the early 1990s,[1] single-walled carbon nanotubes have become attractive new materials with many important potential applications.[2] Beginning in 1998 when the first single-walled carbon nanotube field effect transistor (CNTFET) was built,[3] great progress has been made to understand the transistor operation [4] and to improve the performance.[5−8] Early approaches toward fabricating nanotube transistors include dispersing nanotubes onto prefabricated electrodes, or locating the predispersed nanotubes using various microscopes and then patterning the electrodes via e-beam lithography.[3] Alternatively, a chemical vapor deposition (CVD) technique has been developed by Dai et al. to grow nanotubes off patterned catalyst islands, followed by defining metal contacts aligned to the catalyst.[9] These techniques are truly enabling and have led to enormous success in the past, although one common feature is the need of alignment (or registration), for example, between the electrodes and the nanotubes, or between the electrodes and the catalyst islands. In addition, nanotube transistors made in the past are usually constructed atop Si/SiO_2 substrates, with a drawback of having rather large parasitic capacitance between the bonding pads and the underlying silicon substrate.

In this paper, we present a high-yield, registration-free nanotube-on-insulator (NOI) approach for fabricating nanotube devices based on aligned single-walled carbon nanotubes grown atop a-plane sapphire substrates.[10] One distinct advantage of this NOI approach is that patterning of the source and drain electrodes is a registration-free process because the aligned nanotubes are all over the sapphire substrate. In addition, this approach is in close analogy to the industry-adopted silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) approach, and they share one common feature of possessing minimized parasitic capacitance. We have demonstrated both top-gated and polymer-electrolyte-gated field-effect transistors successfully using this approach. Furthermore, these aligned nanotube arrays can be transferred to flexible substrates and thus hold great promise for future flexible electronics.

Schematic diagrams of logic gates based on SOI and NOI techniques are shown in Figure 1 to illustrate the similarity between them. SOI technology has been a subject of research for decades, and has become commercially important since it was adopted by IBM for Power PC microprocessors in 1998.[11] The simple SOI circuit shown in Figure 1a can be fabricated by defining transistors at the desired locations, removing silicon from unwanted areas, and then patterning the interconnects. One characteristic of this SOI approach is that single-crystalline silicon is all over the underlying substrate, which enables the patterning of devices at any desired location. In addition, the source and drain of a SOI transistor reside atop the underlying silicon oxide instead of *n*- or *p*-well in traditional silicon devices. This leads to substantially lower source/drain capacitance, smaller parasitic delay, and lower dynamic power consumption for SOI transistors. As a result, SOI has become particularly attractive because it offers high device performance and low power consumption.

The potential of having aligned carbon nanotube arrays is illustrated in Figure 1b. Like SOI, we can fabricate NOI

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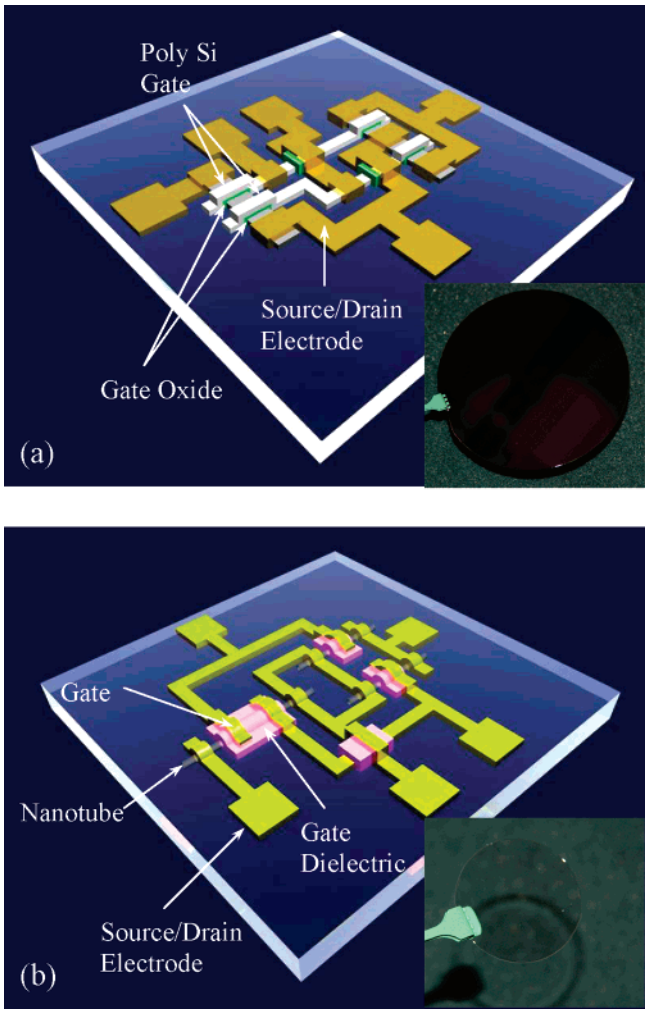

Figure 1. Schematics of (a) a silicon-on-insulator logic gate and (b) a nanotube-on-insulator logic. The insets are photographs of an SOI wafer and an NOI wafer, respectively.

transistors at any desired location on the sapphire substrates (Figure 1b inset) by patterning the source/drain electrodes, thus eliminating the time-consuming positioning step essential for approaches for nanotube devices reported previously. Unwanted carbon nanotubes can be removed easily by O_2 plasma, and interconnects between devices can be subsequently easily patterned. In addition, the source and drain metal contacts of the NOI transistors will reside on bulk sapphire substrates. This is in sharp contrast to traditional nanotube devices with metal electrodes and large bonding pads residing on Si/SiO_2 substrates, which carried significant parasitic capacitance between the electrodes and the silicon substrate. For example, even with 500-nm-thick oxide, a 100 $\times$ 100 μm^2 metal pad gives a parasitic capacitance of 0.7 pF, whereas the gate capacitance for a nanotube of 4 μm in length and 2 nm in diameter with 10 nm oxide is $\sim$0.4 fF, lower than the parasitic capacitance by 3 orders of magnitude. Indeed, ring oscillators made of traditional nanotube transistors on Si/SiO_2 substrates were observed previously to switch at 3 kHz, and this slow switching is most likely a victim of the parasitic capacitance.[12] By fabricating nanotube transistors on sapphire substrates, the NOI approach boasts minimized parasitic

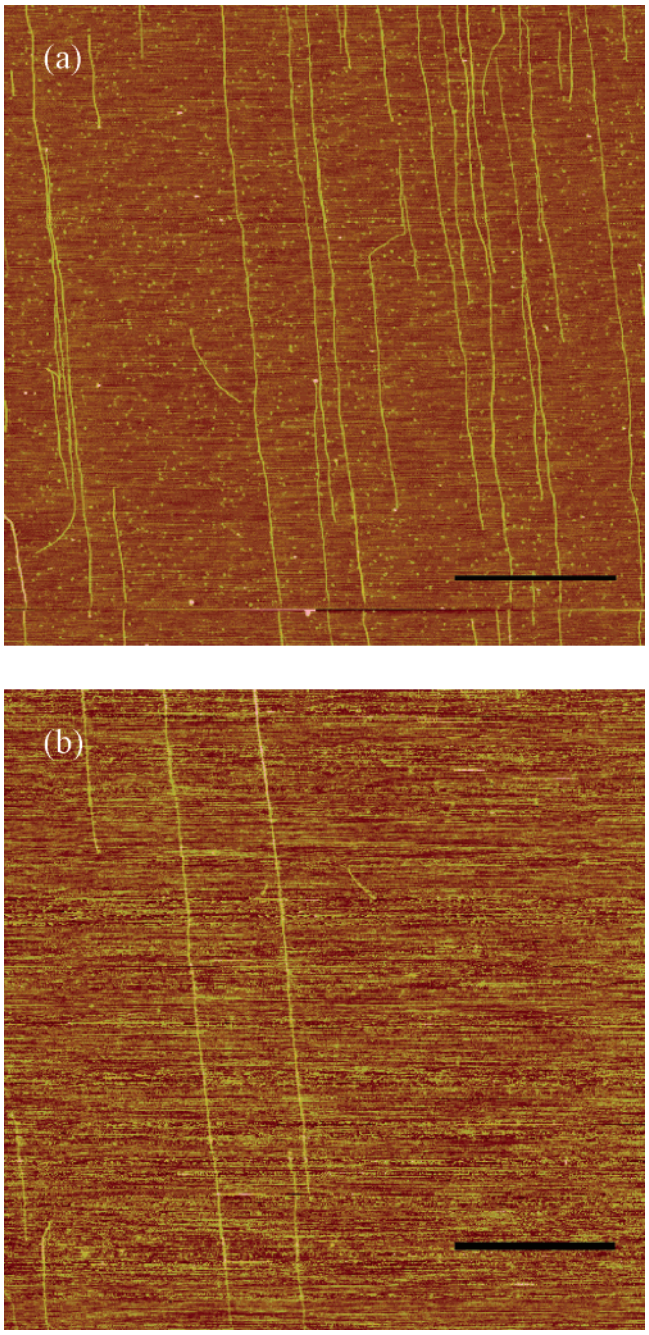

Figure 2. AFM images of two NOI samples with different nanotube densities. The scale bars in both images represent 1.25 μm.

capacitance and may enable both large-scaled integration and high-frequency switching.

Key to our success is a novel chemical vapor deposition (CVD) technique we have developed to synthesize high-density aligned carbon nanotube arrays on a-plane and r-plane sapphire substrates.[11] In a typical process, an a-plane sapphire substrate was first cleaned thoroughly with supersonic bath in acetone for about 10 min, followed by oxygen plasma for further cleaning. The substrate was subsequently incubated in ferritin solution (Sigma Aldrich) for about 10 h and rinsed with deionized water. The substrate was then transferred to a high-temperature furnace and calcinated for 5 min at 700 °C. AFM studies showed that a layer of catalyst

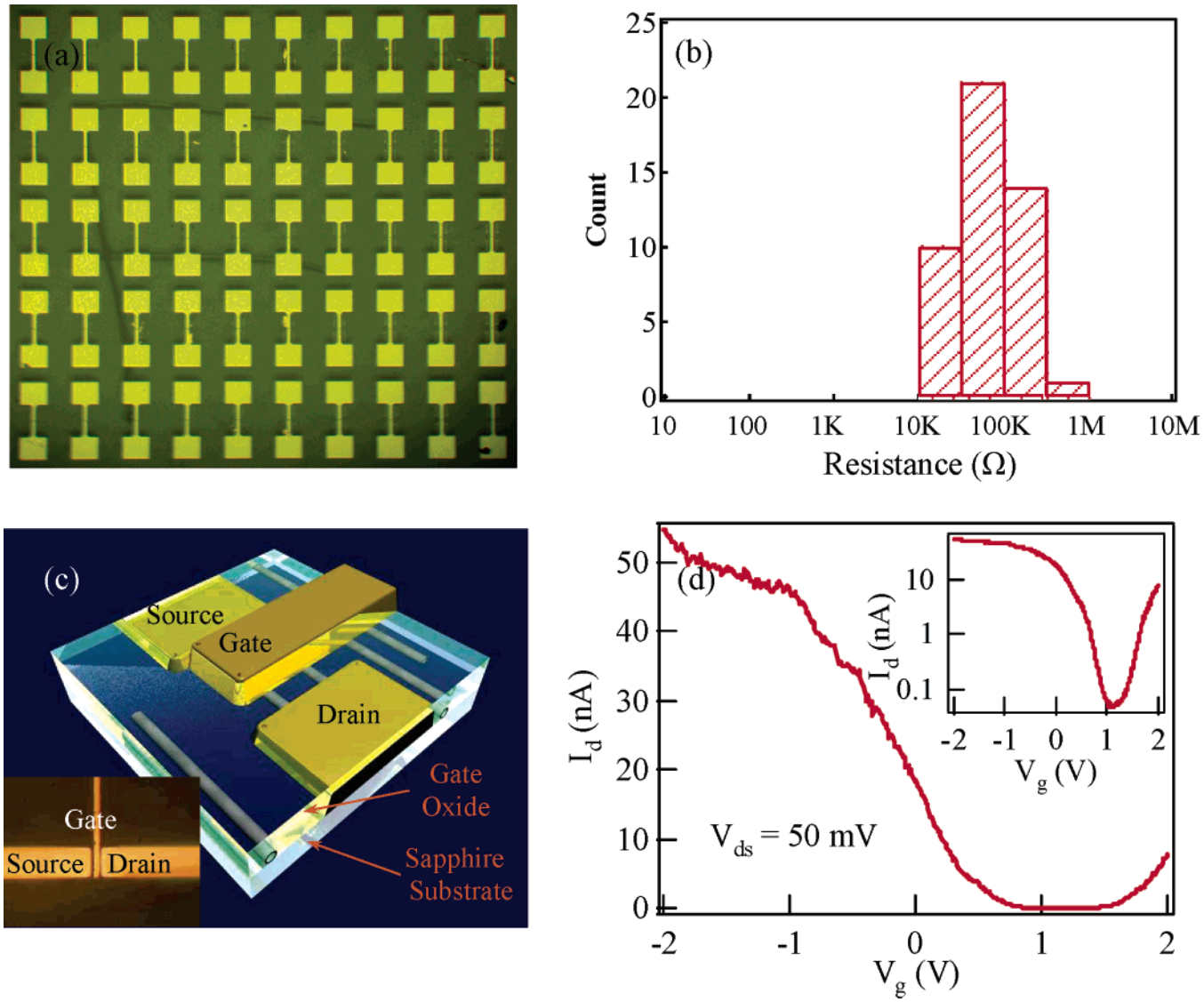

Figure 3. (a) Photograph of an NOI chip showing 50 devices with pairs of source/drain electrodes. (b) Histogram of the resistance of the NOI devices. (c) Schematic diagram of a top-gated NOI transistor. The inset is a photograph of the transistor. (d) $I-V_g$ curve of a top-gated NOI transistor exhibiting ambipolar behavior. $V_{ds} = 50$ mV. Inset: $I-V_g$ curve in logarithm scale.

particles with narrow diameter distribution was formed after the calcination. Following the calcination, the sample was heated to 700 °C in hydrogen atmosphere to reduce the catalyst particles, and then the temperature was raised to 900 °C while flowing 10 sccm ethylene, 800 sccm hydrogen, and 2000 sccm methane to grow the carbon nanotubes. After the sample cooled to room temperature, AFM was used to confirm the growth of an aligned nanotube array and revealed a narrow diameter distribution of 1.4 ± 0.3 nm. Figure 2 displays two SEM images of the aligned single-walled carbon nanotubes, which grew along the direction normal to the *c* axis on a-plane sapphire. The density of the nanotubes can be controlled by tuning the concentration of the ferritin catalyst. When the as-bought ferritin solution was diluted by a factor of 500 and then used for the ferritin incubation step, we obtained a nanotube density of ~1.5 tubes/μm^2 as shown in Figure 2a. When a dilution ratio of 1:5000 was used, we observed a much lower nanotube density, ~0.3 tube/μm^2, as shown in Figure 2b.

The aligned nanotube arrays offer us a viable way to fabricate a large quantity of carbon nanotube devices with the reduced complication of locating nanotubes and making alignment between the nanotube and the metal contacts. For the fabrication of nanotube transistors, we first used photolithography to define an array of Ti/Au contacts as the source and drain electrodes with the conduction channel parallel to the aligned nanotubes, as shown in Figure 3a. This registration-free process delivered a high yield of potential devices: electrical measurements of the source/drain electrode pairs revealed that 98% of the devices were connected by carbon nanotubes and exhibited significant conduction. We note that this high yield is achieved without any special static charge protection. Interestingly, we found that there was no conduction (or cross-talking) between adjacent devices shown in Figure 3a. This can be understood easily because almost all of the nanotubes were aligned in the vertical direction in Figure 3a; hence, no conduction path could be found between the devices in one row. Figure 3b

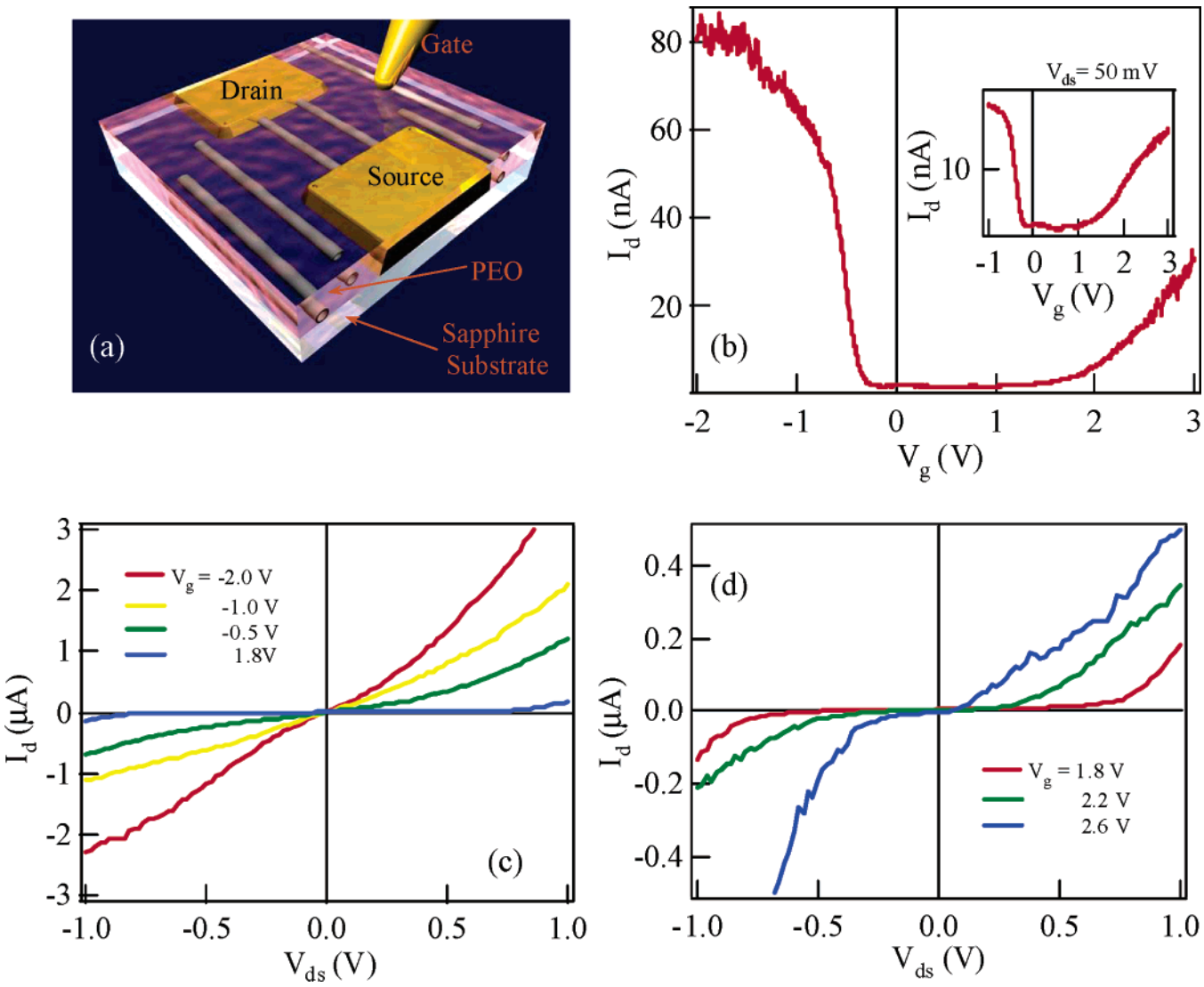

Figure 4. (a) Schematic diagram of a polymer-electrolyte-gated NOI transistor. (b) $I-V_g$ curve of the polymer-gated transistor. Inset: $I-V_g$ curve plotted in logarithm. (c) $I-V$ curves of the transistor in the p regime. (d) $I-V$ curves of the transistor in the n regime.

displays a histogram of the resistance of the devices shown in Figure 3a. All of the devices except one exhibited a resistance between 10 and 300 kΩ. This distribution can be narrowed significantly by using NOI samples with very high nanotube densities, and we have observed nanotubes densities as high as 40 nanotubes/μm by using a high-density ferritin catalyst.

Following patterning of the source and drain electrodes, 500-nm silicon oxide was thermally vaporized onto the substrate as the gate dielectric, and then top-gate electrodes were deposited onto the oxide layer above the channels by lithography. The top-gated device structure is shown in Figure 3c, with the source and drain electrodes contacting the nanotubes directly, gate oxide deposited throughout the substrate, and the top gate electrodes defined above the conducting channel of the nanotubes. A top-view photograph of a typical device is shown in the inset of Figure 3c. For some devices, the electrical breakdown technique[13] was applied to selectively remove the metallic nanotubes by passing a high current through the device while keeping a high positive gate voltage to deplete the semiconducting nanotubes. These top-gated nanotube devices exhibited very good transistor characteristics. Figure 3d displays the current versus gate voltage (I_d-V_g) curve of a typical device showing pronounced ambipolar transport at room temperature, as evident in the observed p-type behavior for V_g < 0.8 V and n-type behavior for V_g > 1. 5 V. The transconductance of this device can be derived to be 36 nS in the p region and 25 nS in the n region. The number of nanotubes bridging source and drain electrodes can be estimated to be ~5. It is well known that the performance of nanotube transistors with Ti/Au contacts is limited by the Schottky barriers at the contacts. We therefore expect that these transconductance values can be improved significantly by using different metals (e.g., Pd) to eliminate the Schottky barriers and/or by improving the quality of the dielectric layer. Furthermore, from the logarithm plot of the $I-V_g$ curve in the inset of Figure 3d, we can extract the subthreshold swing of this device as 220 mV/dec in the p region and 250 mV/dec in the n region, respectively. These values are reasonably close to the ideal subthreshold swing of 60 mV/dec for MOSFETs,

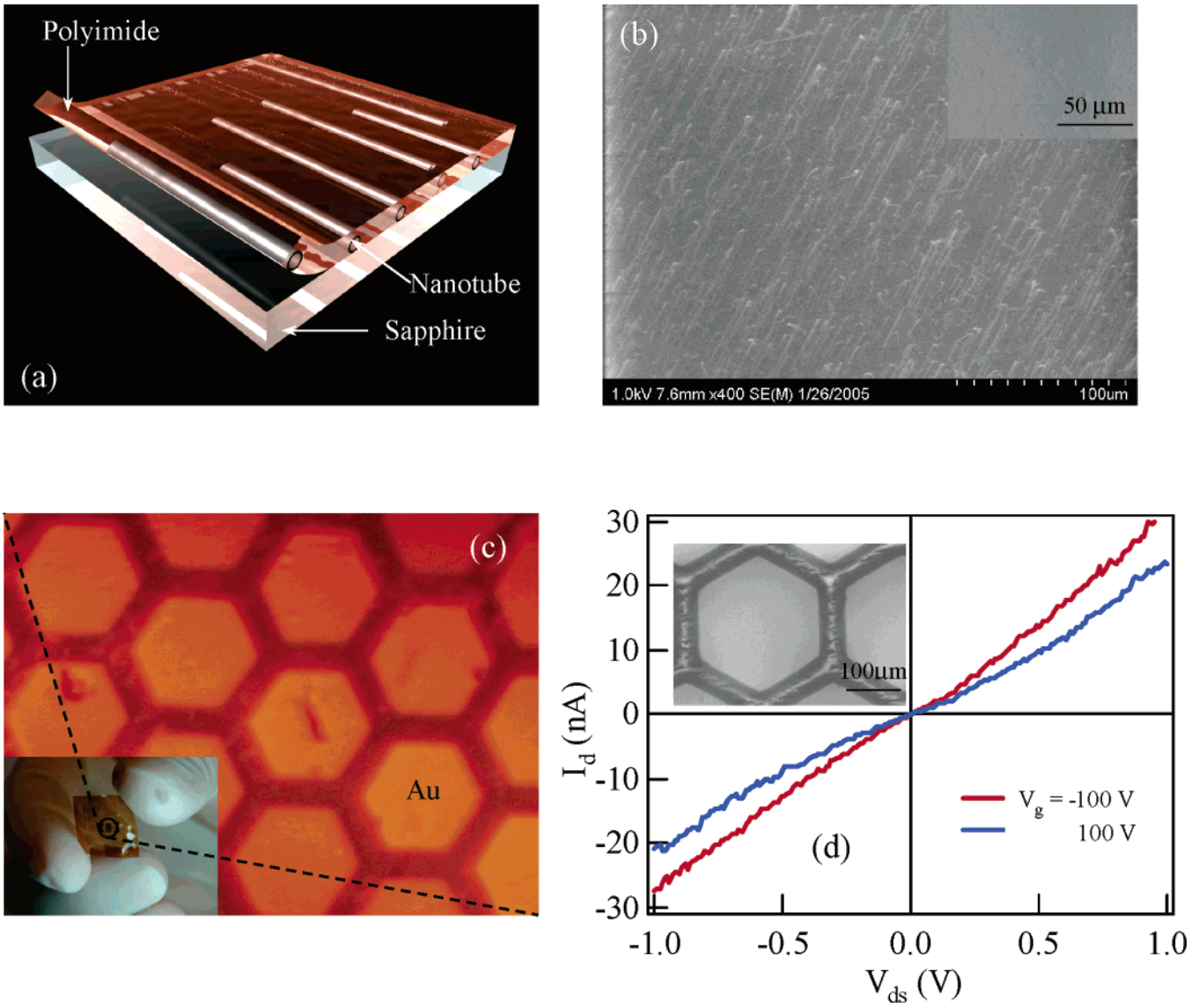

Figure 5. (a) Schematic diagram illustrating the transfer of aligned nanotubes to a flexible polymer substrate. (b) Inset: SEM images of an NOI sample before and after the transfer. (c) Photograph of the polyimide substrate with transferred nanotubes and patterned metal electrodes. Inset: a photograph showing bending of the polyimide substrate. (d) $I-V$ curves measured between two electrodes with $V_g = -100$ and 100 V. Inset: SEM image of the device.

and further optimization of the device structure should lead to even better performance.

In addition to top-gated nanotube transistors, this registration-free NOI approach can be extended easily to polymer-electrolyte-gated devices. First, we patterned the source and drain electrodes as discussed for top-gate device fabrication. A polymer electrolyte made of poly(ethylene oxide) (PEO)[14,15] was then spin coated onto the substrate, followed by baking at 90 °C for 4 h in vacuum to remove the solvent. A probe tip was subsequently put in contact with the PEO layer close to the active nanotube channel and used as a local gate electrode, as shown in Figure 4a. The electrical breakdown technique was used again to selectively remove metallic nanotubes. Most of the fabricated devices showed ambipolar characteristics. Figure 4b displays the $I-V_g$ curve of a typical device. As V_g increased from −2 to 0 V, the device exhibited suppressed conduction and became fully depleted around −0.4 V. The device remained depleted until the gate voltage reached 1 V. For V_g beyond 1 V, the current increased with increasing gate voltage, indicating n-type semiconductor characteristics. This ambipolar behavior can also be observed clearly in the current−voltage ($I_d - V_{ds}$) plots shown in Figure 4c and d, corresponding to the p regime and the n regime, respectively. We can extract the transconductance of the device shown in Figure 4b as 180 nS in the p region and 20 nS in the n region, respectively. Again, these values can be improved significantly with optimized devices.

The above-mentioned transistors based on aligned nanotube on sapphire substrates may have great potential for use for integrated nanotube circuits because of the high-yield nature of the fabrication process; however, another important area of electronics, flexible electronics, may benefit from aligned nanotubes residing atop flexible substrates.[16] We have developed an approach for transferring the aligned nanotubes from sapphire substrates onto flexible polymer substrates

successfully. We started with NOI samples with highly aligned carbon nanotubes and then deposited several drops of polyimide onto the substrate. After baking the sample on a hotplate at 90 °C for 2 h, we peeled the polyimide film (~0.5 milimeter in thickness) off of the sapphire surface, as shown in the schematic diagram in Figure 5a. Figure 5b and the inset display SEM images of an NOI sample before and after the peeling process, respectively. One can see clearly that there were abundant aligned nanotubes on the sapphire before the transfer, whereas virtually no nanotube can be found left on the sapphire after the transfer. This unambiguously confirms the success of the transfer process and indicates that the polyimide−nanotube interaction can overcome the van der Waals interaction between the sapphire substrate and the nanotubes easily. To test the electrical properties of the transferred nanotube arrays, we deposited Ti/Au electrodes onto the polyimide substrate using a TEM grid as a shadow mask. The inset of Figure 5c shows a nanotube-on-polyimide sample, which can be bent by our fingers and is apparently flexible. A photograph of the sample with deposited Ti/Au electrodes is displayed in Figure 5c, showing arrays of hexagonal Ti/Au electrodes with separations of ~30 μm. The bridging carbon nanotubes can be visualized in the SEM image displayed in the inset of Figure 5d, although the insulating polyimide substrate made it difficult to resolve individual carbon nanotubes clearly. A metal electrode was subsequently put in contact with the backside of the polyimide substrate and used as a gate electrode. Figure 5d shows two $I-V$ curves measured between two adjacent Ti/Au electrodes with the gate electrode biased at −100 and 100 V, respectively. The observed conductance serves as further evidence for the successful transfer of the aligned single-walled carbon nanotubes because our control experiment performed with bare polyimide films revealed no conduction at all. The relatively weak gate dependence shown in Figure 5d is understandable because the thick polyimide layer prohibits strong gate modulation. This problem can be solved easily by patterning top gate electrodes with a thin dielectric layer atop the nanotubes-on-polyimide sample.

By now, the potential of the NOI approach for micro- and flexible electronics has been discussed extensively. We note that the device performance can be improved significantly with further optimization of the device design. For instance, although the above-mentioned top-gated nanotube transistors had typically ~5 nanotubes bridging the source/drain electrodes, this number can be increased easily by 1 order of magnitude by using NOI samples with higher nanotube densities (up to 40 nanotubes/μm has been demonstrated). Further optimization may include reducing the channel length down to a deep submicrometer regime and using a dielectric layer of 5−10 nm in thickness. Combining the high carrier mobility for nanotubes and the minimized parasitic capacitance, the optimized NOI transistors may compare favorably with modern silicon-based transistors and bode well for power electronic and flexible electronic applications. We note, however, that the aligned nanotubes grown on sapphire consist of mixed metallic and semiconductive ones, which remains a hurdle for building integrated carbon nanotube circuits. Controlled growth of aligned and predominantly semiconductive nanotubes on sapphire substrates could lead to a new realm of nanotube research and is currently being pursued.

In summary, we have developed a novel nanotube-on-insulator (NOI) approach for producing high-yield nanotube devices based on aligned single-walled carbon nanotubes. This approach enabled a large quantity of devices to be made at desired locations and required no registration between the source/drain electrodes and the nanotubes, in addition to the advantage of providing minimized parasitic capacitance. On the basis of this approach, we have demonstrated both top-gated and polymer-electrolyte-gated nanotube transistors with yield ~98%. These transistors exhibited pronounced ambipolar transport characteristics and high on/off ratios. In addition, the aligned nanotubes on sapphire can be transferred easily to polyimide substrates by first depositing polyimide to the NOI sample and then peeling the film off. Our approach has great potential for high-density, large-scale integrated systems based on carbon nanotubes for both micro- and flexible electronics.

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