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Molecular Memory Based on Nanowire–Molecular Wire Heterostructures

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This article reviews the recent research of molecular memory based on self-assembled nanowire–molecular wire heterostructures. These devices exploit a novel concept of using redox-active molecules as charge storage flash nodes for nanowire transistors, and thus boast many advantages such as room-temperature processing and nanoscale device area. Various key elements of this technology will be reviewed, including the synthesis of the nanowires and molecular wires, and fabrication and characterization of the molecular memory devices. In particular, multilevel memory has been demonstrated using In_2O_3 nanowires with self-assembled Fe-bis(terpyridine) molecules, which serve to multiple the charge storage density without increasing the device size. Furthermore, in-depth studies on memory devices made with different molecules or with different functionalization techniques will be reviewed and analyzed. These devices represent a conceptual breakthrough in molecular memory and may work as building blocks for future beyond-CMOS nanoelectronic circuits.

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Keywords: Nanowire Transistors, Nanowires, Molecular Wires, Molecular Memory.

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1. INTRODUCTION

With the continuous increase in the density of silicon-based memories, the process scaling in semiconductor technology will soon reach physical and technical limits. New technologies for electronic memories have been widely explored in the past decade. Molecular electronics[1–32] has been considered to be one of the best solutions to circumvent the limits associated with semiconductor based devices. Electroactive molecules can store charges through discrete redox states that are readily accessible, thus providing a viable approach for programming through oxidation and reduction reactions. Molecular memory could in principle function at nanoscale with a few electrons, and therefore promises low power and ultra-dense systems. There have been recent reports of molecular memory devices, constructed with molecular monolayers sandwiched between metallic contacts.[33–38] This approach has shown interesting device properties; however, the deposition of metals onto a monolayer of molecular wires can lead to low device yield and this problem remains a major challenge.

An alternative approach to the metal/molecule/metal sandwich structures is to utilize redox active molecules to chemically gate charge sensitive nanostructures, such as nanotubes or nanowires. This way it is possible to make reliable contacts to the nanotube or nanowire and control its properties with the self-assembled molecules, without having to make direct electric contacts to the molecules themselves.[39–42] On one hand, discrete multilevels naturally exist in an ensemble of redox-active molecules,[43] or even one molecule containing multiple redox centers.[44] On the other hand, precise charge sensing at discrete levels can be carried out with a semiconducting nanowire transistor[45–49] whose conductance is ultra sensitive to

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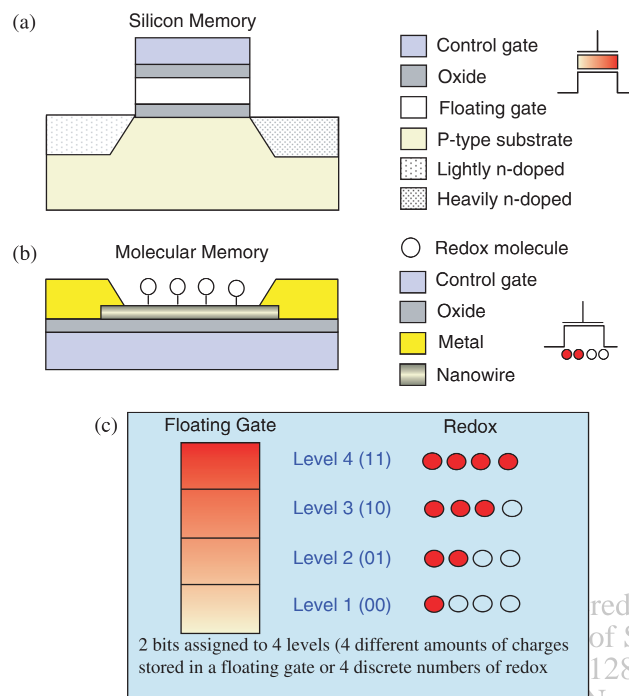

Fig. 1. Schematic diagram compares design and operation for a conventional silicon flash memory (a) and the proposed molecular memory for multilevel nonvolatile data storage (b). (c) In a 2-bit silicon memory cell, four different amounts of charges are placed in the floating gate via channel hot electron injection. In contrast, multilevels in memory cells are represented by altering the population of the reduced/oxidized molecules by applying gate voltage pulses of different amplitude. Current sensing is used in the memory cell for the read-out. Reprinted with permission from [40], C. Li et al., *Appl. Phys. Lett.* 84, 1949 (**2004**). © 2004, American Institute of Physics.

charges in the surrounding environment. The data storage can be carried out by altering the population of the reduced/oxidized molecules, while the read-out can be implemented by measuring the conduction of the nanowire. The device structure is similar to the silicon flash memory, which relies on hot electron injection from the channel into the floating gate through a tunneling oxide layer, and different memory states are represented by different amount of charges stored, as shown in Figure 1.[50] Such molecular memory device can be of great interest for future high-performance data storage. This review presents recent advances on molecular memory based on self-assembled nanowire–molecular wire heterostructures. The design, fabrication, and characterization of these devices are discussed below.

2. SYNTHESIS OF In_2O_3 NANOWIRES AND MOLECULAR WIRES

2.1. Laser Ablation Synthesis of In_2O_3 Nanowires

One-dimensional nanostructured systems have attracted much attention due to their novel properties and great potential applications in numerous areas such as nanoscale electronics, photonics, and sensors.[51–66] Nanowires of various compositions have been synthesized using a wide variety of methods including chemical vapor deposition (CVD),[51–54] laser ablation,[55–57] and electrochemical deposition.[58] These efforts have led to the successful growth of many semiconductive nanowires including Ge,[51,67,68] ZnO,[69–71] Si,[72–75] GaN,[76–80] and GaAs,[81] which were then employed to construct exciting systems such as nanowire integrated systems[82–84] and nano-lasers.[85–88]

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The laser assisted catalytic synthesis approach is the most common used method for semiconductive nanowires synthesis.[89–92] Figure 2(a) shows the schematic diagram of the typical laser-assisted chemical vapor deposition system. Taking the synthesis of In_2O_3 nanowires as an example, a source target (InAs was used for In_2O_3 nanowires) was placed at the upstream end of a quartz tube furnace and the In vapor generated during the laser ablation process was carried downstream by a stream of Ar mixed with 0.02% O_2. A Si/SiO_2 substrate decorated with Au clusters was placed at the downstream end and used to collect the final products. The pressure inside the quartz tube was kept at 100–700 Torr and the temperature was maintained at 770 °C during the whole process. The growth follows the well-known vapor–liquid–solid mechanism. This process is illustrated in Figure 2(b) for the In_2O_3 nanowires growth. Indium atoms in the vapor phase first alloyed with the gold clusters, and continued supply of indium brought the In/Au solution beyond supersaturation, followed by the outgrowth of In and reaction with oxygen at the high temperature to form single crystalline In_2O_3 nanowires. The typical reaction time used was about 35 minutes. After cooling down, the samples

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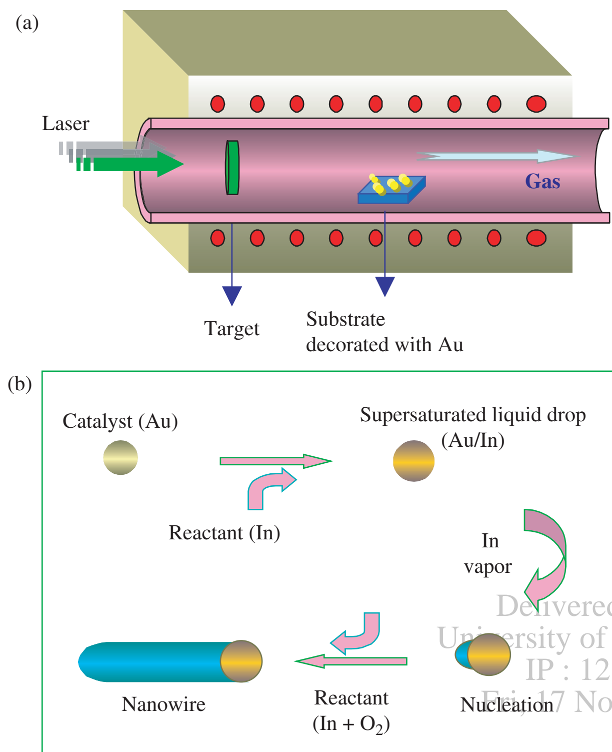

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Fig. 2. (a) Schematic diagram of our laser-assisted chemical vapor deposition setup. (b) Illustration of the vapor–liquid–solid mechanism. The diameter of the nanowires is directly controlled by the catalyst nanoparticle size.

were characterized using scanning electron microscopy (SEM), X-Ray diffraction (XRD), transmission electron microscopy (TEM), high resolution TEM (HRTEM), and selected area electron diffraction (SAED). The nanowire diameters were usually determined using TEM and the lengths were measured from SEM images.

2.2. Characterization

Figure 3(a) shows a typical SEM image of In_2O_3 nanowires grown on the Si/SiO_2 substrate with monodispersed gold clusters as catalysts. These nanowires covered the whole substrates and appeared to be straight. Detailed TEM and SEM examination showed that these nanowires had diameters about 10 nm and lengths exceeding 3 μm, indicating an aspect ratio of more than 300:1. Figure 3(b) is a detailed TEM examination of a single In_2O_3 nanowire made from 10 nm Au cluster. The Au/In alloy particle, with a diameter around 10 nm, can be clearly seen at the very tip of the nanowire. The In_2O_3 appeared rather homogeneous without any domain boundaries, indicating the single crystalline nature of the material, as expected from the vapor–liquid–solid growth mechanism. The nanowire diameter (~10 nm) is apparently consistent with the diameter of the catalytic particle. In addition, indexing the pattern demonstrates that the [110] direction is the nanowire growth direction. A high resolution

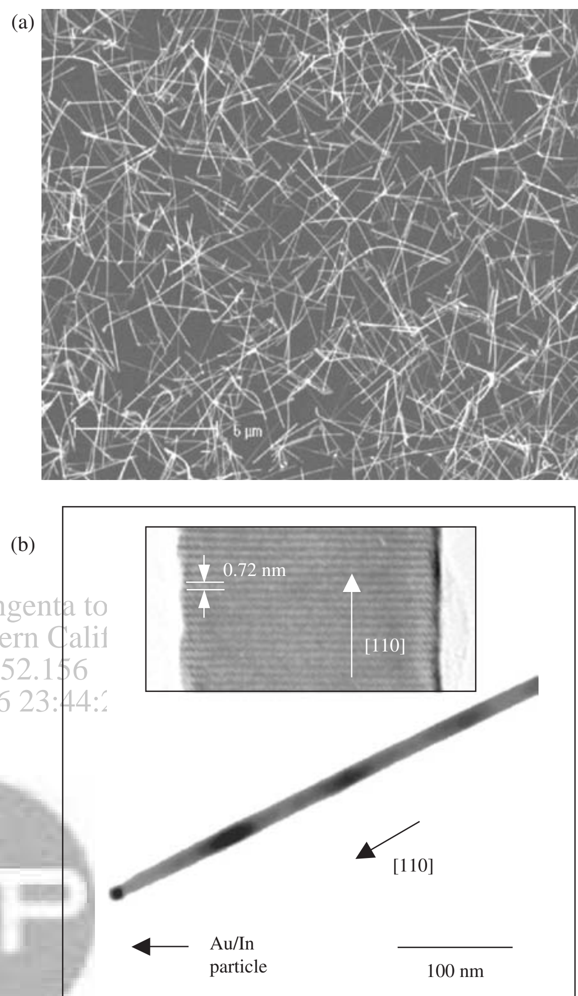

Fig. 3. (a) SEM image of In_2O_3 nanowires grown by laser ablation on a Si/SiO_2 substrate. (b) TEM image of an In_2O_3 nanowire with a catalyst particle at the very tip. Inset: HRTEM image of an In_2O_3 nanowire showing the [110] growth direction. The lattice spacing is consistent with the lattice constant (10.1 Å) for bulk In_2O_3.

TEM image is shown in the inset of Figure 3(b). The lattice spacing along the [110] growth direction (0.72 nm) is in good agreement with the lattice constant for In_2O_3 (1.01 nm).[93] Furthermore, it is apparent from the HRTEM image that there is no native oxide layer outside our nanowire, in sharp contrast to nanowires made of conventional semiconductors such as Si and InP.[94] This important discrepancy leads to significant results such as reliable electrical contacts and superior chemical sensing properties for In_2O_3 nanowires.

2.3. Synthesis of Novel Molecular Wires

A variety of molecular wires have been used for systematic studies. Some representative examples are shown in Figure 4. Molecules 1–5 are based on bis(terpyridine)-Fe(II) and molecules 7–8 are based on porphyrin structures. Molecule 6 is cobalt phthalocyanine (CoPc). For

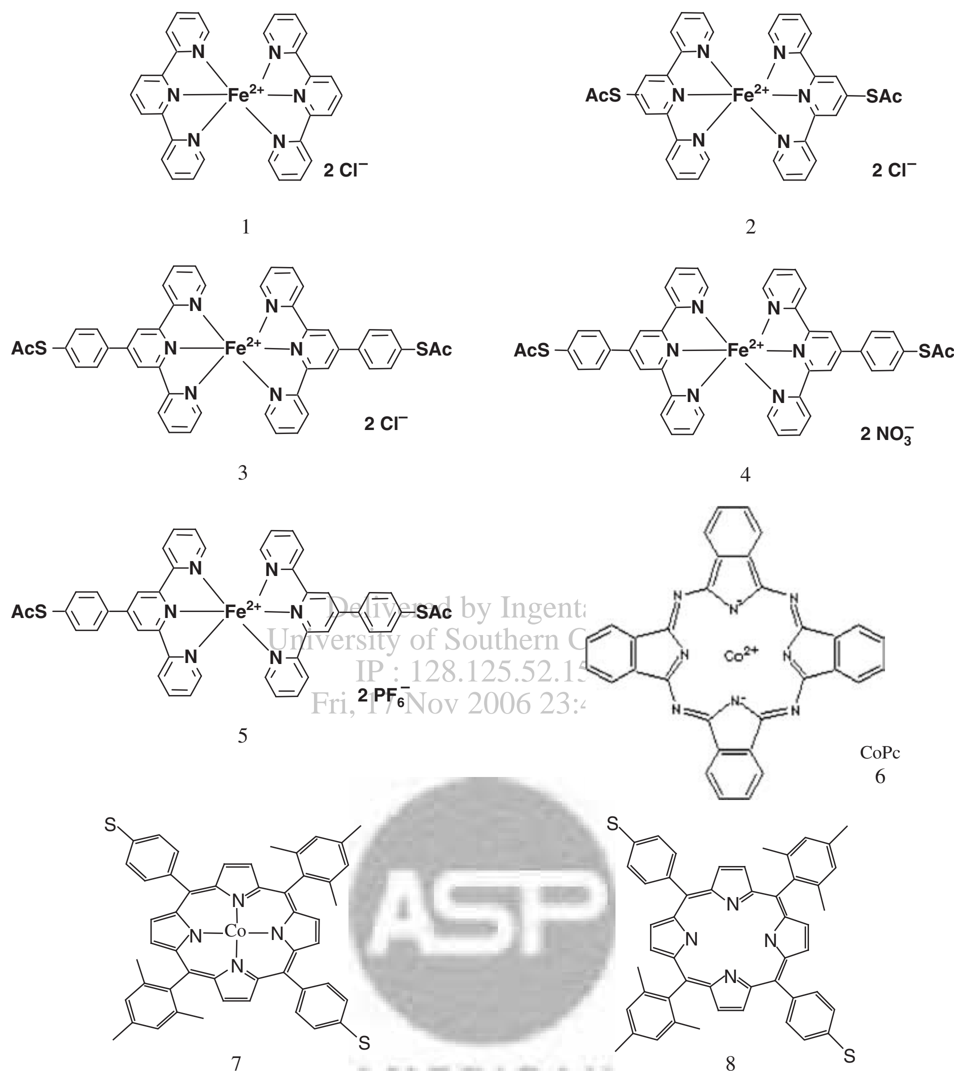

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Fig. 4. Typical molecular wires used for this study.

bis(terpyridine)-Fe(II), molecules with different ligand length (molecules 1–3) and also with different counter ions (molecules 3–5) were synthesized. Because of their octahedral configuration in coordination, bis-(terpyridine)-transition metal complexes exhibit superior chemical and electronic stability toward redox reactions.[95–97] A model for application of these molecules in molecular electronics uses the metal atom as charge storage vehicle and the terpyridine ligands as insulating barriers for charge transfer.[9] The porphyrin molecules have been synthesized with different chelations (molecules 7–8). All the molecules have thiolate groups except molecules 1 and 6. It is known that molecules with thiolate groups can chemisorb on In_2O_3 surfaces to form strong bonds while those molecules without cannot; the latter may physisorb, i.e., get trapped by weak van der Waals interaction, thus forming weaker and random contacts with the nanowire surface.[98] Among these eight compounds, molecules 1–7 are expected to exhibit facile redox properties while molecule 8 has much higher redox potentials.

The molecules shown in Figure 4 were synthesized according to literature methods[96, 97, 99, 100] and were characterized with 1H and 13C NMR, mass (ES) spectroscopy, and elemental analysis. These molecules represent an important family of molecular wires and make systematic transport studies possible.

3. FABRICATION AND CHARACTERIZATION OF NANOWIRE/MOLECULAR WIRE HYBRID MEMORY DEVICES

After the synthesis In_2O_3 nanowires were then deposited onto a silicon wafer coated with SiO_2. Source/drain electrodes contacting the nanowires were patterned using photolithography or E-beam lithography and the silicon substrate was used as the back gate electrode.[46] These devices exhibited typical *n*-type field effect transistor behavior and showed no hysteresis in electrical properties when measured in vacuum.

Functionalization of the nanowire surface was carried out by two approaches, spin-coating and chemisorption. The first method is to spin coat chlorobenzene solutions of redox active molecules such as ferrocene, zinc tetrabenzoporphine, and cobalt phthalocyanine (CoPc) onto nanowire device, which produces a uniform molecule layer on the nanowire surface (Fig. 5(a)).[39] InP nanowires were used for this approach. These spun-on films, however, may lead to molecules deposited in various orientations, ranging from standing normal to lying flat on the nanowire surface. To prepare more robust nanowire/molecular interface with better control, dithioacetate terminated molecules were prepared and the gating effect of the self-assembled monolayers (SAM) on In_2O_3 nanowire field effect transistors (FETs) were studied. The as-fabricated devices were immersed into a 0.1 mM–0.5 mM solution of the desired molecules. A small amount of aqueous NH_4OH was added to the solution to convert the thioacetate groups into free thiols, which spontaneously adsorbed onto the In_2O_3 surface and formed self-assembled monolayers,[98] as shown in Figure 5(b).

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3.1. Operation Mechanism of Memory Devices

The memory studies were based on devices consisting of individual nanowires. The writing operation of the devices was performed by applying a negative voltage pulse to the Si back gate, which led to positive charges injected into the self-assembled molecules, leaving them in the oxidized state. The readout of the memory was performed by measuring the conductance of the In_2O_3 nanowire with the gate bias fixed at 0 V or a small voltage, where the oxidized molecules should work as a chemical gate and lead to a high-conductance state for the *n*-type semiconductive In_2O_3 nanowire. Vice versa, applying a positive bias to the gate can return the molecules to its reduced form and bring the nanowire device to a low-conductance state. The retention time of the memory devices is therefore determined by the charge retention of the redox states of the self-assembled molecular coating, which can be controlled by rational engineering of the molecular structures.

For the spin coated molecular layer, the overall configuration and operating principle are almost the same. In a NW-FET functionalized with redox active molecules,

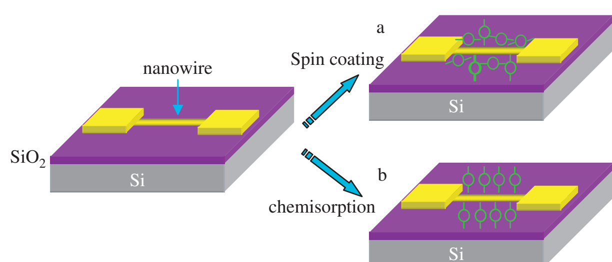

Fig. 5. Two approach to functionalize the nanowire surface: (a) Spin-coating and (b) chemisorption.

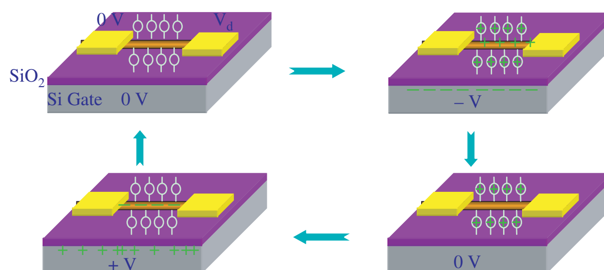

Fig. 6. Operation mechanism of the molecular memory devices.

an applied gate voltage (V_g) or source–drain voltage (V_{sd}) pulse injects net positive or negative charges on the molecular layer. However, the oxide layer on the NW surface serves as a barrier to reduce charge leakage between the molecules and NW, and thus maintain the charge state of the redox molecules.

3.2. Memory Device with Spin-Coated Molecular Layer

The *n*-type InP nanowire FET was used in this study. These devices were typically measured in high vacuum to eliminate the effect of adsorbed water molecules. Figure 7(a) showed the typical conductance ($G = I/V_{sd}$) verse V_g curve before and after modification with a CoPc layer. Both curves show *n*-type transistor behavior, as the gate voltage went up, the conductance of transistor increased. However, a large hysteresis was observed in G–V_g after addition of the CoPc layer, in sharp contrast to little or no hysteresis in G–V_g before adding CoPc molecules. From the hysteresis, two states can be defined as high conductance ON state and low conductance OFF state. These two states can be switched by a V_g pulse (e.g., 10 V for off state and −10 V for on state), and the change is as high as 10^4. The conductance of the NW-FET switch was continuously monitored at a fixed V_{sd} and V_g, while the NW-FET was switched between *on* and *off* states by a V_g pulse (Fig. 7(b)). This type of devices have been demonstrated to show reversible switching over many cycles between the *on* and *off* states without much degradation. The molecule gated NW-FETs was further demonstrated to show memories with a V_{sd} pulse, which was used to inject positive or negative charges on the redox active molecules. Similar to G–V_g curve, G versus V_{sd} measurements exhibit a significant hysteresis in CoPc-modified NW-FETs (Fig. 7(c)), while no hysteresis is observed in the unmodified NW-FETs. The two states can be reversibly switched using 2–5 V source–drain pulses (Fig. 7(d)). Further more, parallel arrays of CoPc-modified NWFETs have been assembled and characterized. Parallel arrays of NW devices were assembled using the fluidic-flow directed assembly approach (Fig. 7(e)). It has been found that the two adjacent devices can be independent addressed and switched without significant coupling (Fig. 7(f)). These results demonstrate that the

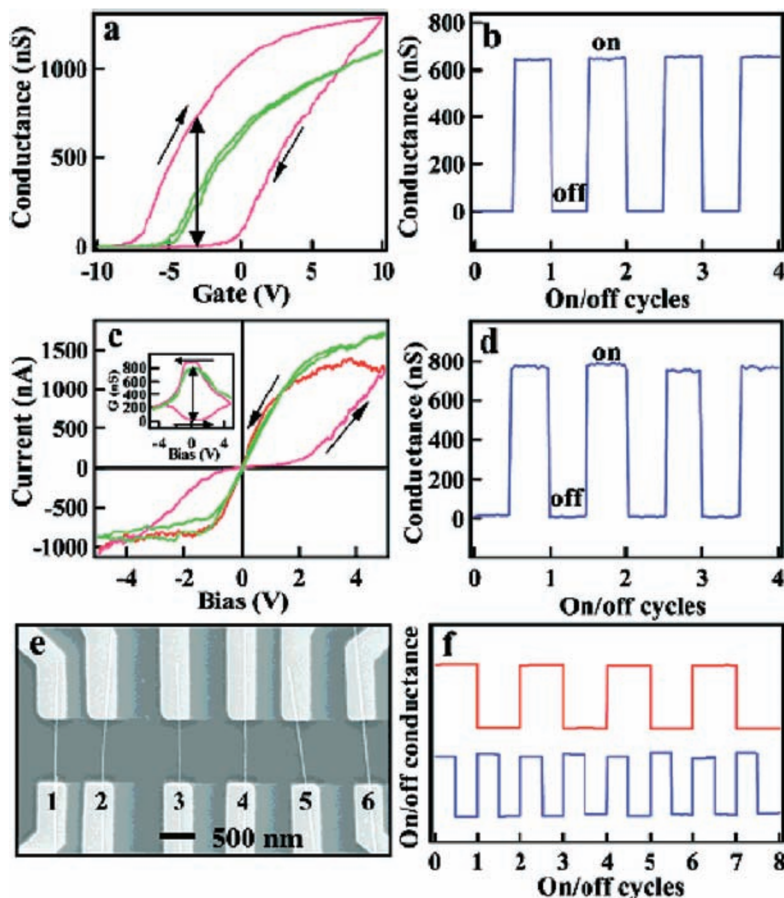

Fig. 7. (a) Conductance versus V_g for an n-InP NW-FET before (green) and after (red) surface modification with CoPc recorded with $V_{sd} = 0.1$ V. Single-headed arrows show gate sweep directions, and the double-headed arrow indicates a position of large *on/off* hysteresis. (b) Reversible *on* and *off* switching of the device in (a) using +10 and −10 V, respectively, 1 s gate pulses; *on/off* states were measured with $V_{sd} = 0.1$ V and $V_g = -3$ V. (c) I versus V_{sd} for an n-InP NW-FET before (green) and after (red) surface modification with CoPc; (inset) Conductance versus V_{sd}. (d) *On* and *off* switching of the device in (c) using +5 and −5 V, respectively, 1 s bias pulses; *on/off* states were measured with $V_{sd} = 0.1$ V. (e) SEM image of a parallel array of NW devices. (f) Independent switching of two devices in a parallel array; +5 and −5 V bias pulses were used to switch between *on* and *off* states, respectively. Reprinted with permission from [39], X. Duan et al., *Nano Lett.* 2, 487 (**2002**). © 2002, American Chemical Society.

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molecule-gated NWFET switches can be independently programmed, and thus could be utilized, for example, as nonvolatile random access memory that is integrated in parallel array structures.

3.3. Porphyrin-Based Molecular Memory Devices

Figure 8(a) shows typical memory operations of an In_2O_3 nanowire field effect transistor functionalized with a self-assembled monolayer of Co-porphyrin molecules. All the measurements were carried out at room temperature with the devices residing in a high-vacuum chamber to eliminate the effect of moisture (pressure ♡ ← 10^{-6} Torr). These devices exhibited a striking hysteresis in the current (I) versus gate bias (V_g) curve, as shown in Figure 8(a). The source–drain bias was held constant at −0.1 V, while the gate bias was swept from −5 to 5 V. A current onset was observed for $V_g \sim -3$ V; however, when V_g was swept back from 5 to −5 V, the current decreased monotonically and reached zero around 3 V. Similar experiments were also performed with devices containing protio porphyrin molecules using the same method, and typical I–V_g curves are plotted in Figure 8(b). In contrast to the large hysteresis observed with the device containing Co-porphyrin molecules, almost no hysteresis was observed for the devices functionalized with protio porphyrin. More than six devices were measured for each porphyrin, and consistent behavior was clearly observed. This directly links the observed memory effects to the redox states of the metal ion in the porphyrin coating. Cobalt porphyrins show facile oxidation, due to the readily accessible. Protio porphyrins also show oxidation states, associated with oxidation of the porphyrin π-system, but at higher potential than the Co-metallated analogue.[101–102] Thus oxidation of the Co porphyrin leads to a largely metal-centered positive charge, while the protio porphyrin has the charge delocalized over the entire porphyrin. These results indicate that sweeping the gate bias converts the Co-porphyrin

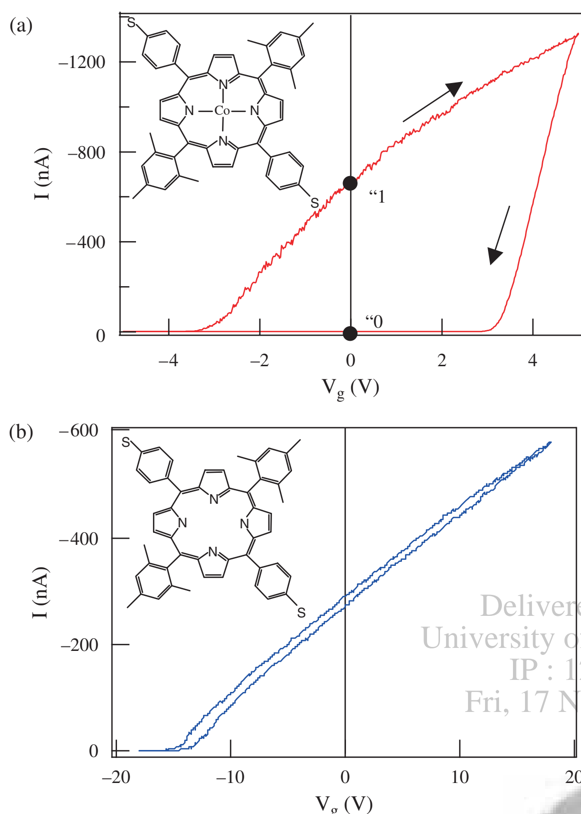

Fig. 8. I–V_g characteristics of In_2O_3 nanowire devices with self assembled Co-porphyrin (a) and protio porphyrin (b), respectively. Insets: structures of the corresponding molecules. Reprinted with permission from [42], C. Li et al., *J. Phys. Chem. B* 108, 9646 **(2004)**. © 2004, American Chemical Society.

molecules to different redox states, which subsequently led to the prominent hysteresis observed in the I–V_g sweep in Figure 8(a). The positive charge, written to the Co porphyrins, leads to a lasting change in the nanowire conductance, whereas cycling to a high enough positive bias can erase the written information and reduce the Co porphyrin. The protio porphyrin molecules, however, do not show evidence of any lasting reduced or oxidized porphyrin states on sweeping the gate bias up to tens of volts, thus clearly illustrating the importance of the molecular porphyrin coating. The working hypothesis is that trapping the charge on the metal center of the porphyrin (as in the Co case) leads to a largely trapped positive charge, relative to the case in the protio porphyrins, where the positive charge extends to edges of the porphyrin molecule and is thus readily transferred back to the nanowire on reverse cycling of the potential.

From Figure 8(a), two memory states, one denoted state "1" and the other denoted state "0," can therefore be defined at $V_g = 0$. From the I–V_g curve in Figure 9(a), a transconductance of $gm = dI/dV_g = 1.56 \times 10^{-7}$ S at a source–drain bias of $V = -0.1$ V for the sweep from −5 to 5 V, and $gm = 8.30 \times 10^{-7}$ S for the sweep from 5 to −5 V can be calculated. Normalized by the width of the nanowire $d = 10$ nm, transconductance values of 15.6 S/m and 83 S/m were thus obtained. The electron mobility can be further deduced from the transconductance of the FET.[103, 104] In the linear regime, it is given by $dI/dV_g = \mu(C/L^2)V$ where C is the capacitance and L is the length of nanowire. The capacitance of the nanowire is given by $C \approx 2\pi\epsilon\epsilon_0 L/\ln(2h/r) = 1.17 \times 10^{-16}$ F, where $\epsilon = 3.9$ is the dielectric constant, $h = 100$ nm is the thickness of the silicon oxide layer, and $r = 5$ nm and $L = 2$ μm

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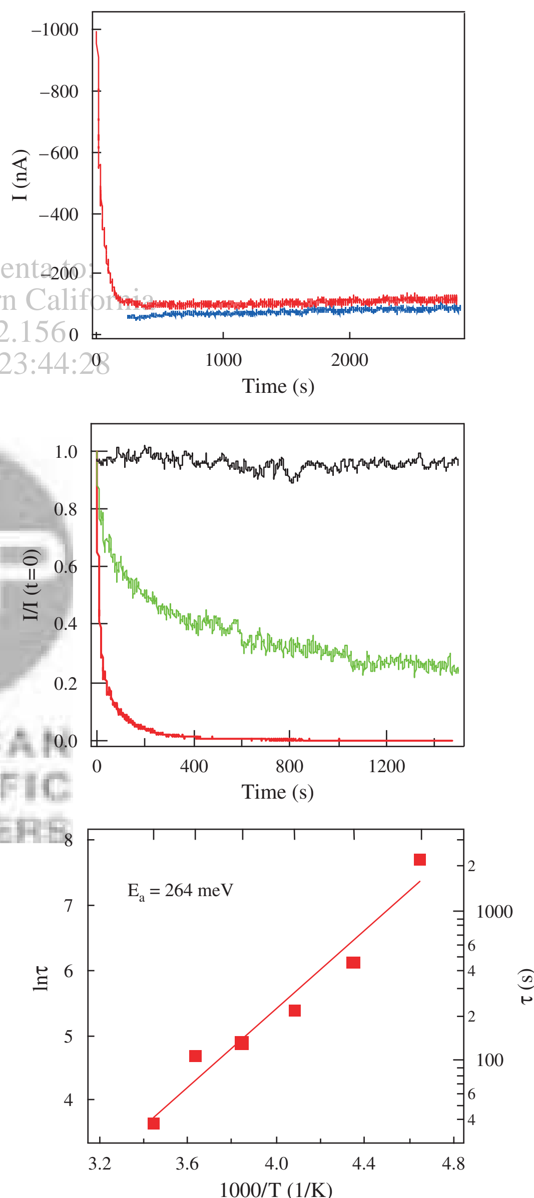

Fig. 9. Retention measurements as a function of time and temperature for In_2O_3 nanowire devices with self assembled Co-porphyrin. (a) Current versus time ($I-t$) for states "1" and "0" measured with $V = -0.2$ V. (b) Current (normalized by $I(t)0$) recorded for state "1" at three temperatures: 160, 230, and 290 K. (c) Temperature dependence of the retention time, indicating an activation energy (E_a) 264 meV. Reprinted with permission from [42], C. Li et al., *J. Phys. Chem. B* 108, 9646 **(2004)**. © 2004, American Chemical Society.

are the radius and length of the In_2O_3 nanowire, respectively. The electron mobility was thus estimated to be 533 cm^2/Vs and 2838 cm^2/Vs from the transconductance values obtained for the different gate bias sweep directions. From the change of the threshold voltage (V_t) when the gate bias was swept back and forth, the electron concentration variation can be estimated using the equation $\Delta n = C\Delta V_t/eL = 3\ \text{nm}^{-1}$, where $\Delta V_t = 6.8$ V is the shift of the threshold gate voltage. This estimation confirms that the memory devices operate with few electrons (3 e^- per nanometer length of the nanowire). We nevertheless note that the equation $C \approx 2\pi \in\in_0 L/\ln(2h/r)$ is only true for the capacitance of an infinitely long cylinder lying above a conductive plane. The nanowire length used in the memory devices is typically finite, and therefore more rigorous modeling of the electrostatics of the nanowire transistors is needed for a reliable estimate of the stored charges.

Bit retention as a function of time and temperature are shown in Figure 9. Current versus time curves (shown in Fig. 9(a)) were taken at room temperature with a fixed source–drain bias $V = -0.2$ V for both State "1" (upper curve) and State "0" (lower curve) right after the writing ($V_g = -5$ V and $+5$ V) was performed. A relatively large decrease in the current value for State "1" was observed, whereas State "0" only exhibited a relatively small increase in current. This is consistent with the fact that the as synthesized Co-porphyrin has Co^{2+} ions (reduced state) as the default state. The retention curve for State "1" can be fitted with an expression $Ae^{t/\tau}$ and a retention time constant of 41 s was obtained. This device was then cooled down with the bit retention measured at various temperatures. Three typical curves are shown in Figure 9(b), corresponding to temperatures of 160 K, 230 K, and 290 K, where the y-axis represents the current normalized by the starting value $I(t = 0)$. One can clearly see that the retention time increased as the temperature decreased. For temperatures lower than 200 K, the device can retain the stored information for several hours without any degradation, as illustrated by the top curve in Figure 9(b). Measurements of the retention time at different temperatures yielded an exponential dependence with $1000/T$, as shown in Figure 9(c). This indicates a thermal activation behavior as $\tau = \tau_0 \exp(E_a/kT)$. The activation energy E_a for this molecule over this bias regime was found to be approximately 264 meV.

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3.4. Pyridine-Based Multilevel Molecular Memory

As mentioned above, the In_2O_3 nanowire devices functionalized with Co-porphyrin molecules showed nice hysteresis curves; however, the retention time is not good enough to work as nonvolatile memory components. Following the same fabrication and self-assembling approach, In_2O_3 nanowires functionalized with a variety of redox-active molecules have been studied. Multilevel data storage has been achieved from Fe-terpyridine molecules by varying the population of reduced or oxidized molecules.

Figures 10 and 11 illustrate characteristic multilevel data storage for a device containing Fe-terpyridine redox molecules. The SiO_2 thickness used for these devices was 500 nm. Figure 10(a) shows a family of I–V_g hysteresis loops taken with different lower-bound and higher-bound values for the V_g sweep. One can clearly see that different negative gate biases can bring the device to different conduction levels at $V_g = 0$ V. Programming of the memory device can therefore be achieved by sweeping V_g from 0 to different negative values, or by applying negative V_g pulses of different amplitude. On the other hand, erasing of the memory device can be easily achieved by sweeping V_g from 0 to a large positive value (e.g., 25 V), or by applying a V_g pulse of 25 V, which leaves the device in a highly resistive state. This is also evident in Figure 10(b), where a family of I–V curves were taken at $V_g = 0$ V after the device was written into various memory levels (denoted state "0" to "8") using V_g pulses of different amplitude. These curves represent distinctively different conduction levels, thus confirming the effectiveness of the memory programming and reading. The different states of the memory devices are attributed to different populations of the oxidized molecular wires, as a higher negative gate bias is expected to bring more negative charges to the Si/SiO_2 interface and correspondingly more positive charges to the nanowire/molecules, thus leaving more molecules in the oxidized state.

The retention of the memory devices was characterized for nonvolatile applications. Figure 10(c) shows the retention time measurements taken with fixed source–drain bias $V = -0.1$ V for memory states "0" to "8" right after the writing was performed. All the states showed little degradation over time and remain clearly separated from each other even after 1500 seconds. The on/off ratio between state "0" and state "8" is estimated to be 10^4 through out this duration. Extended stability test was carried out up to retention of 600 hours. The readout current at each of the eight levels remained within 80% variation for first 120 hours (5 days). Figure 10(d) shows extended retention test results for state "0" and state "6" measured with a source–drain bias $V = -10$ mV. Both states were very stable and exhibited slow decays over a period of many days. They eventually reached steady states, featured by current values of 63 nA from initial 100 nA for state "6" and 48 nA from initial 10^{-2} nA for state "0". These levels are still distinguishable since the white noise is on the order of ~1 nA. Such stability in both the on and the off states is remarkable, as other molecular memories typically hold retention times ranging from hundreds of seconds to a few hours.[33–35] Four different redox molecules that vary either in metal ion (Fe^{2+} or Co^{2+}) or counter ion (Cl^- or PF_6^-), and found that retention time can vary from minutes to hundreds of hours and follows a general trend

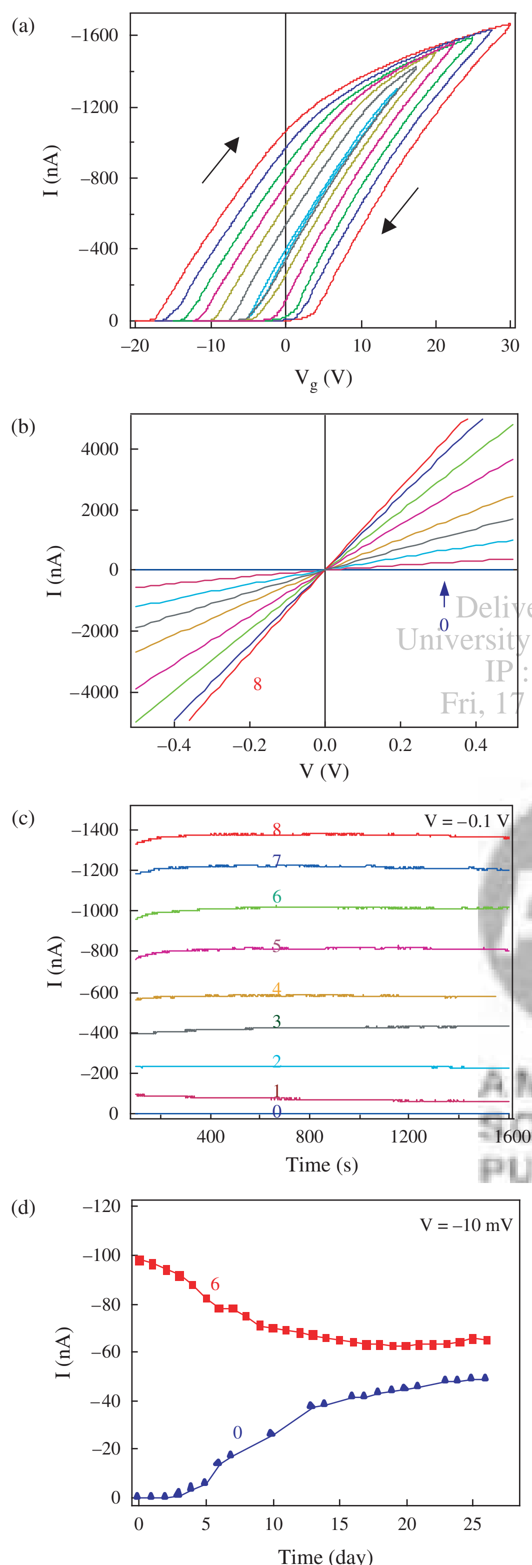

Fig. 10. Characteristic programming and erasing, reading and retention obtained from the devices functionalized with Fe^{2+}-terpyridine molecules. (a) I–V_g hysteresis loops obtained by sweeping gate voltage from $-n*2.5$ V to $10+n*2.5$ V and then back to the starting value. n is the index of levels from "2" (the innermost curve) to "8" (the outermost curve) (b) I–V characteristics recorded after the device was written using V_g pulses of +25 V, −2.5 V, −5 V, −7.5 V, −10 V, −12.5 V, −15 V, −17.5 V, −20 V, respectively, from the least conductive curve to the most conductive one. Inset is the molecule structure. (c) Current recorded over time after the device was written into states "0" (the bottom curve) to "8" (the top curve), $V_{ds} = -0.1$ V. (d) Extended retention measurements performed for state "0" and "6" with $V_{ds} = -10$ mV. Reprinted with permission from [40], C. Li et al., *Appl. Phys. Lett.* 84, 1949 (**2004**). © 2004, American Institute of Physics.

of $Fe^{2+} > Co^{2+}$ and $Cl^- > PF_6^-$. The molecular memory promises greatly enhanced retention or charge storage stability through appropriate molecular design, thus offers an attractive solution to problems resulting from poor charge storage in down-scaling of current silicon flash memory.

Writing/reading/erasing operations in real time domain have been further carried out for storage of 1, 2, and 3 bits in the same cell, respectively, at 2, 4, and 8 levels, as shown in Figure 11. For one-bit (two-level) memory, the device was repeatedly written into state "0" and "1" by applying alternating V_g pulses of 25 V and −12.5 V. The memory state after each writing operation was read out at $V_g = 0$ V with a source–drain voltage of −0.1 V, and the data are plotted in Figure 11(a). For two-bit operation, the memory cell was written into state "0," "1," "2," and "3" using V_g pulses of 25 V, −5 V, −10 V, and −15 V, respectively, as shown in Figure 11(b). V_g pulses of 25 V were also used to erase the previous memory state for the ensued writing. Three-bit memory operation were similarly carried out using V_g pulses of +25 V, −2.5 V, −5 V, −7.5 V, −10 V, −12.5 V, −15 V, −17.5 V, and −20 V, and the data are shown in Figure 11(c). Tens of cycles for endurance test for each memory operation have been tested and all levels were found distinguishable in the tested cycles.

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3.5. Molecular Structure Dependence

To ascertain the role of molecular structure in charge storage, In_2O_3 nanowire devices self-assembled with a family of terpyridine molecules have been systematically studied (Fig. 12(a)). First the I–V_g curves of the NW-FETs assembled with the terpyridine ligand (lower right inset of Fig. 12(b)) and with molecules 1–3 were obtained. As shown in Figure 12(b) and Figures 13(a–c), the device with just the ligand showed very little hysteresis while devices with molecules 1–3 showed large hysteresis loops. A significant hysteresis indicates an electronic bistable system where the two states defined at $V_g = 0$ V can be used for data storage applications. These results confirm that the redox active Fe(II) center is responsible for the memory effect. Furthermore, the hysteresis becomes more pronounced within the series of molecules 1, 2, and 3, as is evident by the increasing gate voltage shift (ΔV_{th}) of 4.8 V, 10.0 V, and 28.0 V, showing a strong dependence of ΔV_{th} on molecular structure. We stress that the observed hysteresis is highly reproducible. For each molecule we have

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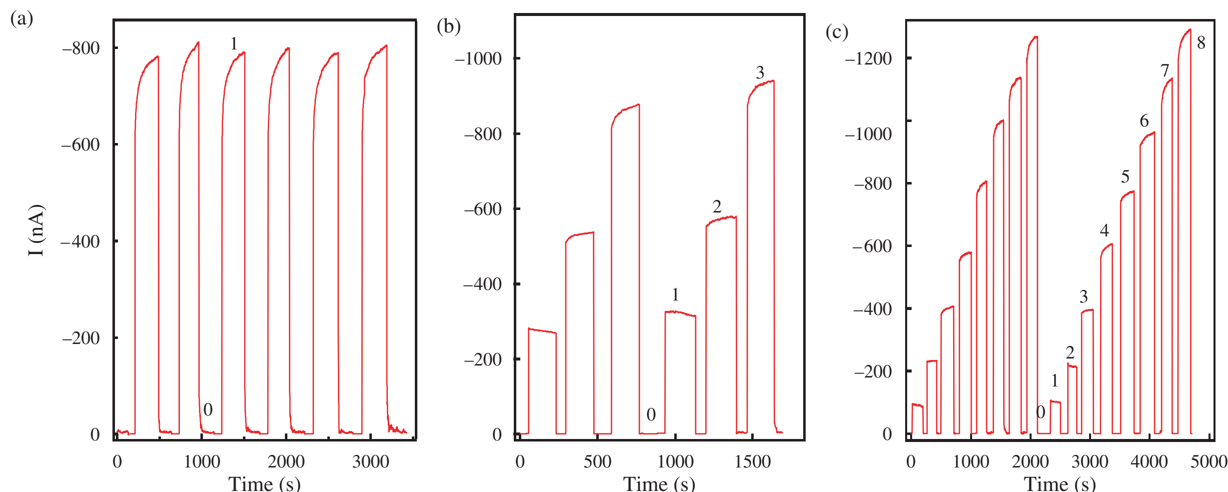

Fig. 11. Endurance test characterized by cycling of write-erase-read operations for 1, 2, and 3 bits data storage at 2 (a), 4 (b), and 8 (c) levels, respectively. Reprinted with permission from [40], C. Li et al., *Appl. Phys. Lett.* 84, 1949 **(2004)**. © 2004, American Institute of Physics.

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measured more than three devices, and consistent results were observed.

Charge retention was obtained by first writing (or erasing) the devices into "*on*" (or "*off*" state) using gate voltage pulses and then recording the source–drain conduction over time with fixed V_{ds} of −0.1 V. Figures 13(d–f) show the dependence of drain current on time for devices

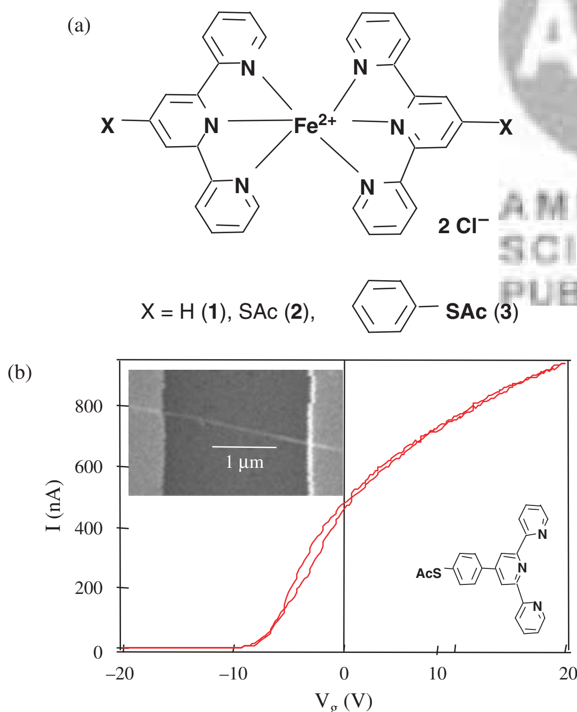

Fig. 12. (a) A family of the bis(terpyridine)-Fe(II) molecules with different ligand length. (b) I–V_g curve of the device modified with the ligand of molecule 3 at $V_{ds} = 0.1$ V. Inset: SEM image of the nanowire device. Right: the structure of the ligand. Reprinted with permission from [41], C. Li et al., *J. Am. Chem. Soc.* 126, 7750 **(2004)**. © 2004, American Chemical Society.

with molecules 1–3 at both "*on*" (red curve) and "*off*" (blue curve) states. From these curves, retention time τ was estimated as τ_1 = 200 seconds, τ_2 = 12 hours, and τ_3 = 287 hours. (Here the retention time was defined as the time when the current difference $\Delta I = I_{on} - I_{off}$, where I_{on} and I_{off} are current for "on" and "off" state, respectively, falls to 40% of the original current difference.) The ratio τ_1:τ_2:τ_3 of 1:216:5166 indicates a strong dependence of charge retention on molecular structure. For electron transfer reactions involving a single electron tunneling step, the exponential dependence of electron transfer constant on distance has been described by the super exchange model[106, 107] and also observed in experiments.[107, 108] Compared with molecule 2, the extra phenyl ring between the thiolate headgroup and the Fe(II) center in molecule 3 increases the charge tunneling distance by 5–6 Å, thus could be responsible for the larger τ measured for molecules 3 ($\tau_3 = 24\tau_2$). It is less straightforward to comprehend the even greater difference in retention between molecules 1 and 2 ($\tau_2 = 216\tau_1$), since the two molecules only differ in a thiolate headgroup. However, it is known that molecules with thiolate groups can chemisorb on In_2O_3 surface to form strong contact while those molecules without can not; the latter may physisorb, i.e., trapped by weak van der Waals interaction, thus forming weaker and random contacts with the In_2O_3 surface. These weak and random contacts could result poorly defined charge tunneling paths with low barriers, as is strongly indicated by the sharp current drop in a time scale of 100 s (Fig. 13) for molecule 1. On the contrary, current for devices with molecules 2 and 3 were nearly constant over a much longer time scale (Figs. 13(e–f)). This extremely slow leakage of charge indicates a uniform tunneling path with a high barrier, a possible result of the strong contact formed between the thiolate and In_2O_3 nanowire.

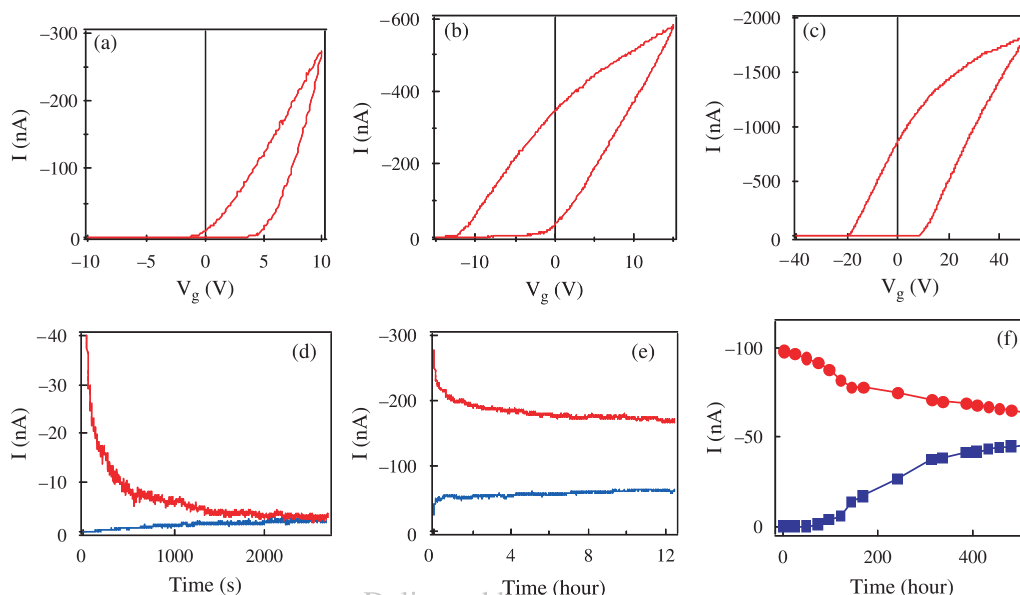

Fig. 13. I–V_g curves of devices with (a) molecule 1, (b) molecule 2, (c) molecule 3 in Figure 12 and retention time measurements of devices with (d) molecule 1, (e) molecule 2, (f) molecule 3 ($V_{ds} = -0.1$ V). Reprinted with permission from [41], C. Li et al., *J. Am. Chem. Soc.* 126, 7750 **(2004)**. © 2004, American Chemical Society.

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4. CONCLUSION

Nanoscale memory devices based on nanowire field effect transistors functionalized with redox active molecules were demonstrated. This technique creates a seamless integration of nanowires and molecular wires and yielded devices with on/off ratios exceeding 10^4. Multilevel nanoscale memory devices based on pyridine molecules were further demonstrated. The multilevel data storage represents a conceptual breakthrough in molecular memory and yielded devices with retention times ~600 hours. This approach may further lend itself for investigation of many intriguing scientific issues such as electron transfer between nanowires and molecular wires, and redox properties of molecules in solid-state devices. Furthermore, both retention time and threshold voltage shift were found to strongly depend on the structure of the bis-(terpyridine)-Fe(II) molecule. These results suggests that the presence of the thiolate headgroup and/or longer ligand length increases charge retention with a wider and more stable memory window, possibly due to the increasing tunneling barrier. The approach of using molecular components, i.e., ligand, to replace the inorganic oxide as insulating layer in memory devices, affords simple fabrication, ultra-small device size, and molecular level control.

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