

Wafer-Scale Growth and Transfer of Aligned Single-Walled Carbon Nanotubes

Nishant Patil, *Member, IEEE*, Albert Lin, *Student Member, IEEE*, Edward R. Myers, Kounghmin Ryu, Alexander Badmaev, Chongwu Zhou, H.-S. Philip Wong, *Fellow, IEEE*, and Subhasish Mitra, *Senior Member, IEEE*

Abstract—Experimental demonstration of wafer-scale growth of well-aligned, dense, single-walled carbon nanotubes on 4" ST-cut quartz wafers is presented. We developed a new carbon nanotube (CNT) wafer-scale growth process. This process allows quartz wafers to be heated to the CNT growth temperature of 865 °C through the alpha-beta phase transformation temperature of quartz (573 °C) without wafer fracture. We also demonstrate wafer-scale CNT transfer to transfer these aligned CNTs from quartz wafers to silicon wafers. The CNT transfer process preserves CNT density and alignment. Carbon nanotube FETs fabricated using these transferred CNTs exhibit high yield. Wafer-scale growth and wafer-scale transfer of aligned CNTs enable carbon nanotube very large-scale integration circuits and their large-scale integration with silicon CMOS.

Index Terms—Carbon nanotube FETs, wafer-scale carbon nanotube growth, wafer-scale carbon nanotube transfer.

I. INTRODUCTION

CARBON nanotube FETs fabricated from horizontally aligned single-walled carbon nanotubes (SWNTs¹) grown on single-crystal quartz substrates have promising applications as extensions to silicon transistors in high-performance digital and analog circuits [1], [2]. At the 32 nm technology node, CNFETs circuits show 13× energy delay product improvement [2]–[4] over 32 nm silicon CMOS due to near-ballistic CNT transport [5]–[7].

Major progress has been made in demonstrating digital circuits using CNTs, e.g., ring oscillator using a single CNT [1]. However, for very large-scale integration (VLSI) CNFET circuits, multiple CNTs are needed per CNFET to provide the current density necessary for high-performance digital circuits [2]–[4]. Significant research is needed for design and integration of multiple-CNT CNFET circuits. For practical VLSI CNFET circuits, CNFETs must be fabricated on a wafer scale. We

present two techniques that enable wafer-scale fabrication of CNFETs. We present wafer-scale growth of aligned CNTs on single-crystal quartz wafers and also demonstrate wafer-scale CNT transfer of aligned CNTs grown on quartz wafers to silicon wafers for VLSI integration with silicon. This low-temperature CNT transfer technique preserves CNT alignment and density. We present distributions of wafer-scale electrical characteristics of CNFETs fabricated from the aligned CNTs. CNFETs fabricated using these transferred aligned CNTs have very high yield (~99%) since they are made from multiple parallel CNTs. For VLSI CNFET integration, it is necessary to quantify CNFET variation [2]. We present statistical data from electrical and physical measurements to quantify the variations of the CNTs and CNFETs across the wafers.

We reported preliminary results of wafer-scale CNT growth and transfer techniques in [8]. In this paper, we provide a detailed description and analysis of the techniques. This paper also presents improved CNT growth and transfer processes that are compatible with patterned CNT growth for significantly enhanced CNT alignment with ~99.5% of all CNTs being aligned. Design techniques described in [9] can be used to fabricate VLSI CNFET circuits that function correctly in the presence of the small fraction of misaligned and mispositioned CNTs.

The paper is organized as follows. Section II describes the wafer-scale-aligned CNT growth process, followed by Section III that describes the wafer-scale CNT transfer technique. Section IV details the characterization of CNTs using atomic force microscopy (AFM) and wafer-scale electrical measurements to quantify CNFET variations.

II. WAFER-SCALE-ALIGNED CNT GROWTH

CNTs grown on substrates such as sapphire or single-crystal quartz grow aligned to a particular orientation of the crystal lattice [10], [11]. Pioneering work has been done in demonstrating aligned CNTs with remarkable CNT alignment on single-crystal quartz substrates. Patterning CNT catalyst in lithographically defined regions dramatically improves CNT alignment as it reduces the probability that a CNT encounters a catalyst particle during growth and becomes misaligned [11], [12].

For VLSI integration of CNFETs, we must scale this aligned CNT growth to the wafer scale. Published processes for aligned growth on quartz only allow growth on small quartz pieces. This is because single-crystal quartz undergoes a phase transformation from alpha quartz to beta quartz at 573 °C. This phase transformation at 573 °C results in a high probability of fracture of single-crystal wafers that are heated through this temperature [13], [14]. Aligned CNT growth requires

Manuscript received May 30, 2008. First published March 10, 2009; current version published July 9, 2009. This work was supported in part by the Focus Center Research Program (GSRC, C2S2, FENA) and in part by the National Science Foundation (NSF). The work of N. Patil was supported by an Art and Mary Fong Stanford Graduate Fellowship. The review of this paper was arranged by Associate Editor D. Litvinov.

N. Patil, A. Lin, E. R. Myers, H.-S. P. Wong, and S. Mitra are with Stanford University, CA 94305, USA (e-mail: nppatil@stanford.edu; mrlin@stanford.edu; edmyers@stanford.edu; hspwong@stanford.edu; subh@stanford.edu).

K. Ryu, A. Badmaev, and C. Zhou are with the University of Southern California, CA 90089 USA (e-mail: kounghryu@usc.edu; badmaev@usc.edu; chongwuz@usc.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TNANO.2009.2016562

¹In this paper, all CNTs are SWNTs.

temperatures higher than 573 °C, and it has also been shown that high temperature (900 °C) annealing of quartz improves CNT alignment [11]. The probability of fracture increases with the size of the quartz substrate. Four-inch quartz wafers shatter when previously published CNT growth processes are used.

We have developed a new CNT growth process that enables full-wafer-scale growth on 4" ST-cut quartz wafers. The key elements necessary for full-wafer-aligned CNT growth on quartz are

- 1) Uniform thermal gradient across the quartz wafer: This is achieved by using a three-zone chemical vapor deposition furnace. The thermal uniformity is further improved by using low pressure² while heating the wafers through the critical phase transformation temperature.
- 2) Slow thermal ramp rate through the alpha–beta phase transformation of single-crystal quartz: This reduces the probability of wafer fracture. This is consistent with prior work done, which determined that the fracture probability of bulk single-crystal quartz is inversely related to the thermal ramp rate as it is heated through the alpha–beta phase transformation temperature [14].

ST-cut quartz wafers (Hoffman Inc.) were first annealed in a three-zone, six-inch oxidation furnace. To avoid wafer fracture, the wafers were heated up slowly to 900 °C. The reduced thermal ramp rate is critical for the quartz wafers to remain intact through the alpha–beta phase transformation. The wafers were annealed in oxygen at 900 °C for 8 h. The presence of oxygen was critical for CNT alignment.³ The wafers were brought back to room temperature after annealing using a similar slow ramp-down through the alpha–beta phase transformation of the quartz. After the annealing step, catalyst was deposited on the wafer. We used either unpatterned ferritin (Sigma Aldrich) solution (diluted 1:150 solution in DI water) or patterned iron catalyst deposited using electron beam evaporation.

After annealing, CNTs were grown in a low-pressure furnace.⁴ Fig. 1 illustrates the detailed process for wafer-scale-aligned CNT growth. The wafer was calcined in air at 550 °C for 10 min to yield catalyst nanoparticles for CNT growth. Note that the calcination temperature is less than the phase transformation temperature; hence a reduced thermal ramp rate to this calcination temperature is not required. After the calcination step, the quartz wafer, with the calcined catalyst, was heated to the CNT growth temperature of 865 °C. For the critical ramp through the phase transition temperature of quartz, the pressure was maintained at 3 Torr with 100 sccm of oxygen flow. The low pressure improves the thermal uniformity of the CNT growth furnace and reduces the thermal gradient across the wafer. The temperature ramp rate from 550 °C to 620 °C was kept at 0.8 °C/min. This ramp rate is consistent with prior studies done on the thermal fracture of bulk single-crystal quartz [14]. A faster ramp rate may be used if thermal uniformity across the wafers is within 1 °C. Beyond this critical temperature range,

²Low pressure reduces convective heat loss, improving thermal uniformity of the furnace.

³Annealing in nitrogen for the same duration gave significantly degraded CNT alignment.

⁴Base pressure of furnace was 10 mTorr.

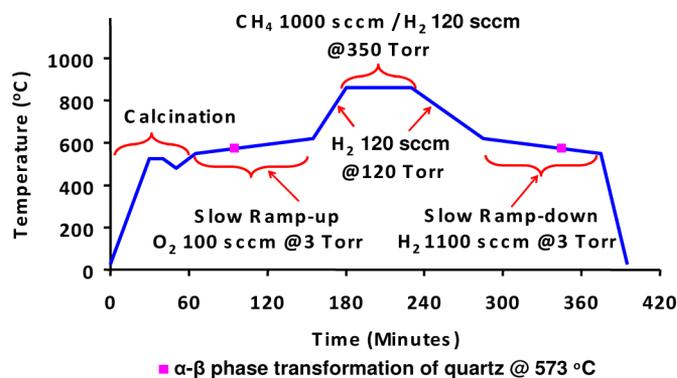


Fig. 1. Wafer-scale-aligned CNT growth process.

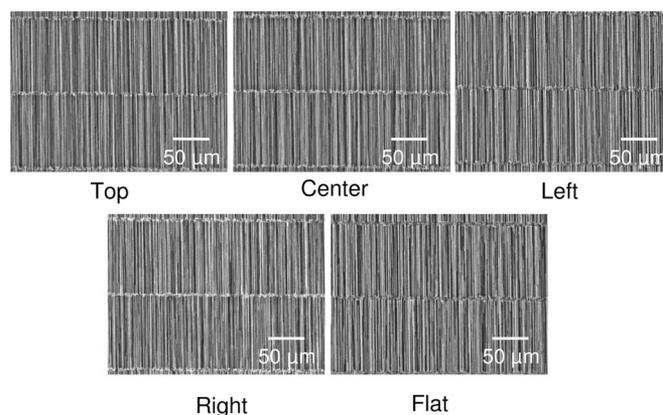


Fig. 2. Wafer-scale-aligned CNT growth using stripped Fe catalyst.

the wafer was heated in hydrogen at 120 Torr to the CNT growth temperature of 865 °C at a thermal ramp rate of ~ 10 °C/min. CNT growth was carried out at 865 °C by coflowing methane and hydrogen (1000 sccm CH_4 /120 sccm H_2) at a pressure of 350 Torr. After growth, the wafer was cooled to room temperature using a similar process employing a slow thermal ramp during the critical phase transformation of the single-crystal quartz wafers. The reproducibility of this wafer-scale growth technique is confirmed by multiple full-wafer-scale-aligned CNT growth runs for the various experiments presented in this paper.

CNT alignment and density can be significantly improved with patterned catalyst with $\sim 99.5\%$ of CNTs being aligned. As mentioned in Section I, design principles described in [9] can be used to fabricate VLSI CNFET circuits that function correctly in the presence of the small fraction of misaligned CNTs. We show that full-wafer-aligned CNT growth on quartz is possible with patterned catalyst (Fig. 2). CNT growth was carried out using the process illustrated in Fig. 1. We used 0.2 nm of evaporated Iron (Fe) catalyst in photolithographically defined stripes. It is desirable to maximize the ratio of aligned CNT area to the catalyst area so that a large fraction of devices have aligned CNTs. We used different catalyst stripe widths (W) ranging from 0.5 to 10 μm and catalyst stripe spacing (S) between 50 and 1200 μm (Fig. 3). The CNTs have an average length of ~ 400 μm and an average density of 5–10 CNTs/ μm . The longest CNTs are approximately 675 μm in length [Fig. 3(a)]. The maximum

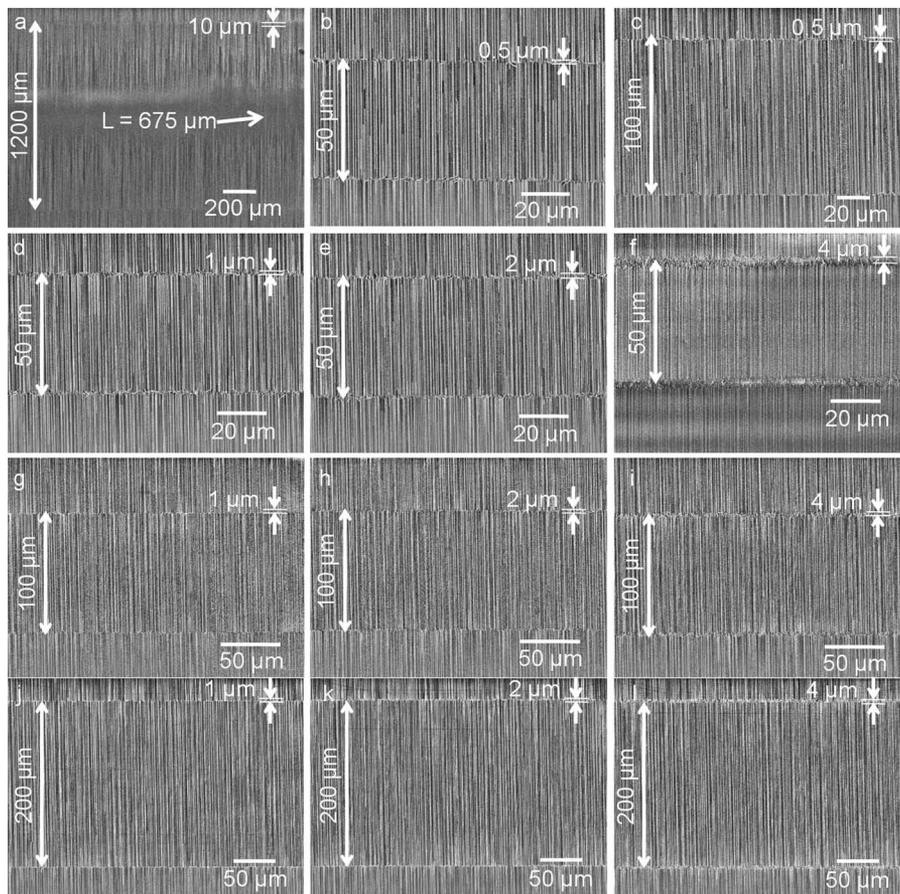


Fig. 3. Effect of catalyst width (W) and spacing (S) on CNT density and CNT coverage. (a) $W = 10 \mu\text{m}$, $S = 1200 \mu\text{m}$. (Length of longest CNT in image = $675 \mu\text{m}$). (b) $W = 0.5 \mu\text{m}$, $S = 50 \mu\text{m}$. (c) $W = 0.5 \mu\text{m}$, $S = 100 \mu\text{m}$. (d) $W = 1 \mu\text{m}$, $S = 50 \mu\text{m}$. (e) $W = 2 \mu\text{m}$, $S = 50 \mu\text{m}$. (f) $W = 4 \mu\text{m}$, $S = 50 \mu\text{m}$. (g) $W = 1 \mu\text{m}$, $S = 100 \mu\text{m}$. (h) $W = 2 \mu\text{m}$, $S = 100 \mu\text{m}$. (i) $W = 4 \mu\text{m}$, $S = 100 \mu\text{m}$. (j) $W = 1 \mu\text{m}$, $S = 200 \mu\text{m}$. (k) $W = 2 \mu\text{m}$, $S = 200 \mu\text{m}$. (l) $W = 4 \mu\text{m}$, $S = 200 \mu\text{m}$.

catalyst spacing, for which CNT density is uniform between stripes, is approximately equal to the CNT length ($\sim 400 \mu\text{m}$). Experimental results show that the catalyst strip can be as narrow as $0.5 \mu\text{m}$. It may be possible to further reduce the width of the catalyst strip, while retaining high CNT density between the stripes.

III. WAFER-SCALE CNT TRANSFER

For VLSI integration of CNFETs on silicon, aligned CNTs need to be transferred from quartz to silicon on a wafer scale. Transfer of aligned CNTs grown on quartz wafer pieces to silicon substrates using gold and polyimide was first demonstrated in [11]. Here, we demonstrate a new CNT transfer technique that can be used to transfer CNTs from quartz to silicon on a wafer scale. This low temperature (90°C – 120°C) transfer procedure uses thermal release adhesive tape (Nitto Denko, Part Number: #3198MS) and preserves CNT density and alignment (Fig. 4). Unlike aligned CNT growth that requires high temperatures, CNT transfer is a low temperature process and enables the integration of CNTs on already fabricated silicon CMOS wafers, dies, and flexible substrates.

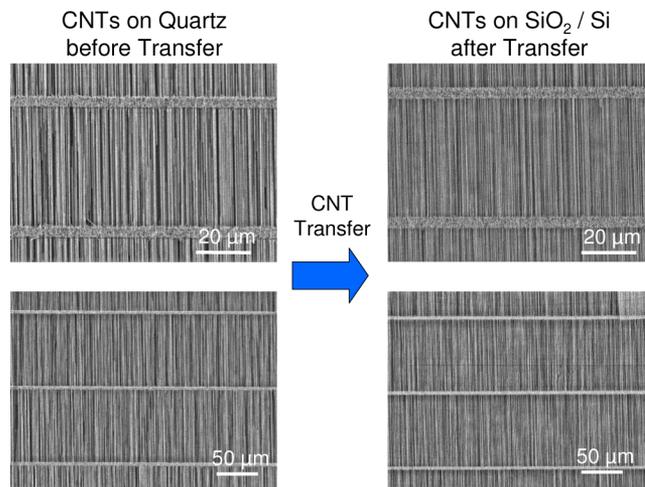


Fig. 4. SEM images of transferred CNTs.

Fig. 5 illustrates the CNT transfer technique. Aligned CNTs are grown on a quartz wafer [Fig. 5(a)]. A gold film (100 nm) is evaporated on the quartz wafer using e-beam evaporation [Fig. 5(b)]. Thermal release tape is applied to the gold film and the tape/gold bilayer is peeled off from the quartz substrate

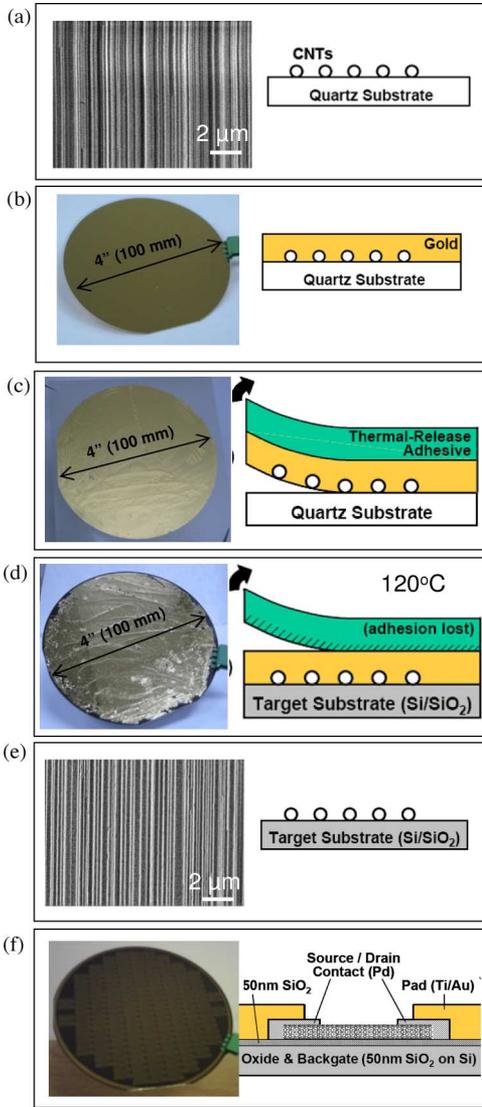


Fig. 5. CNT transfer technique.

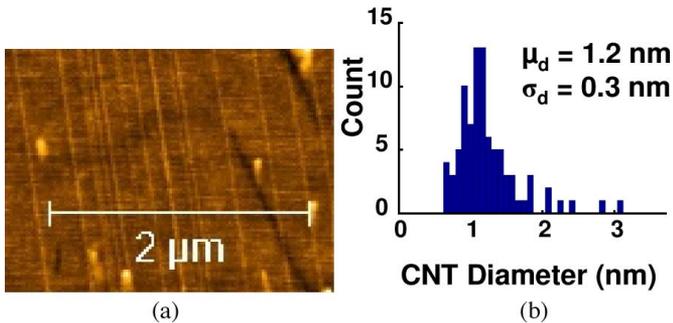


Fig. 6. (a) AFM image of aligned CNTs on quartz. (b) CNT diameter distribution.

[Fig. 5(c)]. The CNTs remain embedded in the gold layer. This tape/gold bilayer is then applied to the target wafer. The target wafer is then heated to the release temperature of the tape (90 °C or 120 °C, depending upon the type of thermal release tape). At this temperature, the tape loses adhesion and peels off, while the gold, along with the embedded CNTs, sticks to the

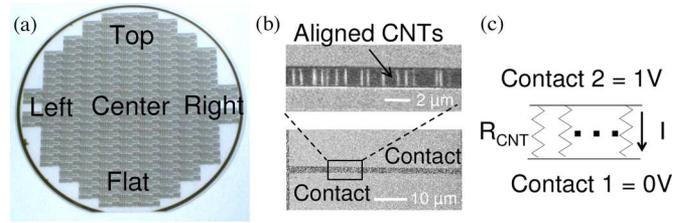


Fig. 7. (a) Optical micrograph of 4" ST-cut quartz wafer after aligned CNT growth and subsequent patterning of contacts. (b) SEM image of aligned CNTs bridging two contacts. (c) Two terminal measurement parameters.

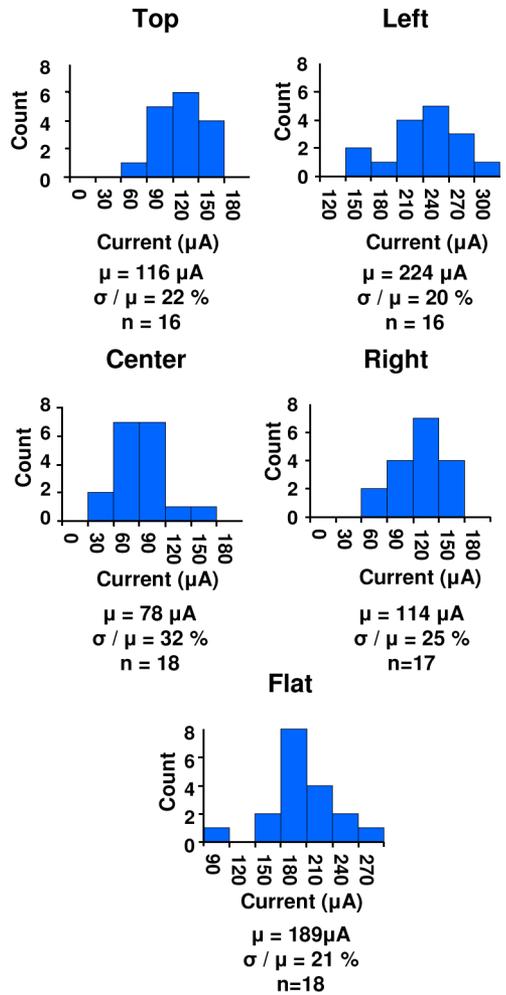


Fig. 8. Two terminal current distributions at 1V bias for n functional devices (out of 18) (Width = 50 μm , Length = 1 μm) in 5 arbitrary dies (out of 197 dies on the wafer) over 5 regions of the quartz wafer.

target substrate (Fig. 5(d)). Oxygen plasma descum (55 W, 25 mTorr, 20 sccm O_2) for 3 min is then used to remove organic residues from the gold surface after transfer. The gold is then removed using gold etchant (Transcene Corp. KI/I₂), which leaves the CNTs on the target wafer. Fig. 5(e) shows an SEM image of the transferred CNTs on a silicon wafer. CNT density and alignment is preserved as can be seen from Figs. 4 and 5(e).

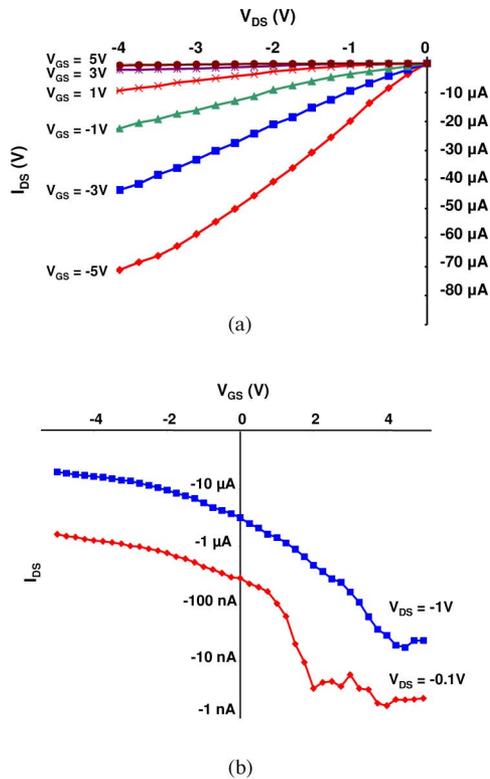


Fig. 9. CNFET current-voltage characteristics (width = 50 μm , length = 1 μm , t_{SiO_2} = 50 nm) after metallic-CNT breakdown. (a) I_{ds} vs. V_{ds} . (b) I_{ds} vs. V_{gs} .

IV. CHARACTERIZATION OF CNTs

Using wafer-scale-aligned CNT growth described in Section II and wafer-scale-aligned CNT transfer described in Section III, we can now characterize CNT and CNFET variations. The CNTs have a mean diameter (μ_d) of 1.2 nm with a standard deviation (σ_d) of 0.3 nm [Fig. 6(b)] as measured from AFM images [Fig. 6(a)]. Fig. 7(a) shows an optical micrograph of a quartz wafer after CNT growth. The wafer was patterned with contacts [Ti (5 nm)/Au (40 nm)] using photolithography and e-beam evaporation of metals. We conducted two-terminal measurements of 18 devices with width = 50 μm /length = 1 μm [Fig. 7(b)] in a randomly selected die in each region (top, left, center, right, and flat) of the wafer. The measured current is due to the CNTs bridging the contacts and provides a measure of the electrical uniformity of the CNTs across the wafer. Fig. 8 shows the mean current and the standard deviation of these two terminal measurements at a bias of 1V. The standard deviation of CNT current equals to $\sim 25\%$ of the mean current in all regions. The variation in CNFET current is likely due to variation in the CNT density and CNT contact resistance.

We also fabricated back-gated CNFETs on silicon wafers using transferred CNTs. Fabricated CNFETs had a low $I_{\text{ON}}/I_{\text{OFF}}$ ratio due to the presence of metallic CNTs. Metallic CNTs can be removed by using electrical breakdown [15] or selective etching [16]. CNFETs retain well-behaved I - V characteristics after electrical burning. Fig. 9 shows the current-voltage (I_{ds} vs. V_{ds} and I_{ds} vs. V_{gs}) measurements of a CNFET with Ti (1 nm)/Au

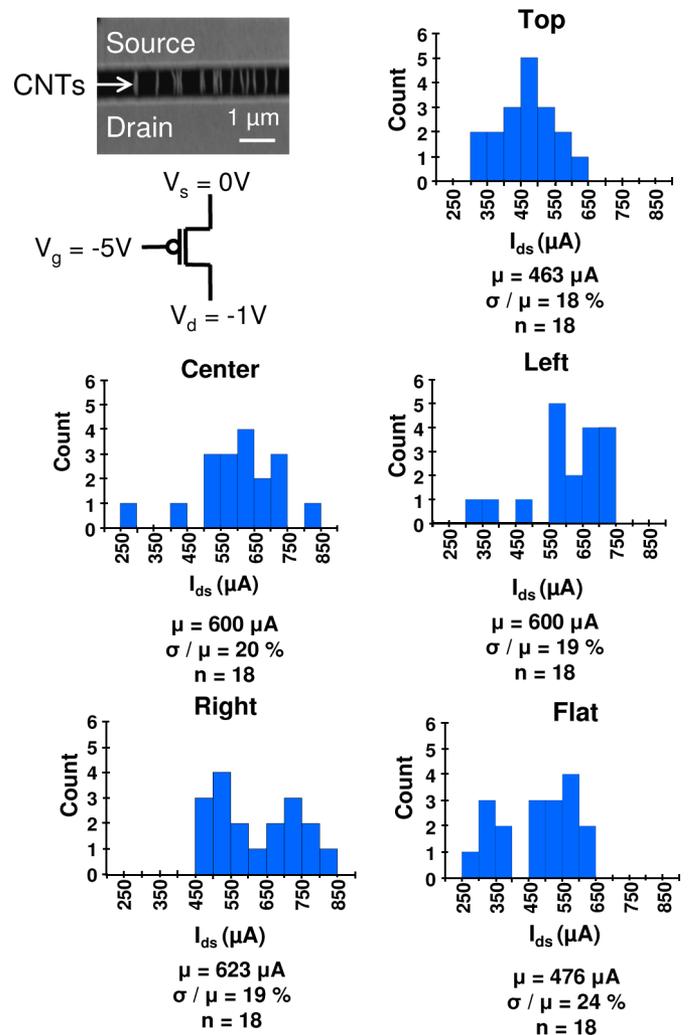


Fig. 10. CNFET current distributions ($V_{\text{ds}} = 1$ V $V_{\text{gs}} = -5$ V) of 18 back-gated CNFETs ($W = 50$ μm , $L = 1$ μm , $t_{\text{SiO}_2} = 50$ nm, Ti(5 nm)/Au(50 nm) contacts) in five regions of the silicon wafer.

(40 nm) source and drain contacts. We used electrical breakdown of metallic CNTs to achieve a high $I_{\text{ON}}/I_{\text{OFF}}$ ratio [15], [16].

To assess the electrical uniformity of the transferred CNTs across the wafer, we measured the I_{ON} ($V_{\text{gs}} = -5$ V, $V_{\text{ds}} = -1$ V) distributions of CNFETs (prior to electrical breakdown). For this electrical characterization, we measured 18 identically sized (width = 50 μm , length = 1 μm) randomly chosen CNFETs in each of the five regions (top center, left, right, and flat) of the wafer (out of a total of ~ 100 000 CNFETs fabricated) (Fig. 10).

SEM images indicate an average CNT density of approximately 4 CNTs/ μm . For the 50 μm wide CNFETs, there are, on average, 200 CNTs per CNFET. The average CNFET ON-current across the wafer is 552 μA corresponding to CNFET average current density of 11 $\mu\text{A}/\mu\text{m}$. For the performance gains over CMOS projected in [2], CNT density must be improved to 250 CNTs/ μm . One potential technique to attain high CNT density is to perform wafer-scale CNT transfer (Fig. 5) multiple times from multiple quartz wafers to the same target silicon wafer.

V. CONCLUSION

We have presented wafer-scale-aligned growth on single-crystal quartz and wafer-scale CNT transfer from quartz wafers to silicon wafers. Full-wafer-scale CNT growth on quartz and full-wafer-scale CNT transfer from quartz to silicon enable wafer-scale characterization of CNFETs and fabrication of VLSI circuits. The low-temperature CNT transfer technique potentially enables integration of aligned CNTs with already fabricated silicon CMOS dies, wafers, and flexible substrates, while preserving CNT density and alignment. Compatibility of wafer-scale aligned growth and transfer techniques with scalable metallic-CNT removal techniques, such as selective etching of metallic CNTs [17], and metallic CNT tolerant circuit design [18] must be investigated.

ACKNOWLEDGMENT

The authors would like to thank D. Akinwande, Prof. H. Dai, Dr. J. N. Kurtin, Dr. J. McVittie, Prof. Y. Nishi, and J. Zhang for fruitful collaborations. Part of this study was done in the Stanford Nanofabrication Facility (SNF) of the National Nanotechnology Infrastructure Network (NNIN) funded by the National Science Foundation.

REFERENCES

- [1] Z. Chen, J. Appenzeller, Y. Lin, J. Sippel-Oakley, A. G. Rinzler, J. Tang, S. J. Wind, P. M. Solomon, and P. Avouris, "An integrated logic circuit assembled on a single carbon nanotube," *Science*, vol. 311, p. 1735, 2006.
- [2] J. Deng, N. Patil, K. Ryu, A. Badmaev, C. Zhou, S. Mitra, and H.-S. P. Wong, "Carbon nanotube transistor circuits: Circuit-level performance benchmarking and design options for living with imperfections," in *Proc. Int. Solid State Circuits Conf.*, 2007, pp. 70–588.
- [3] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application—Part I: Model of the intrinsic channel region," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3186–3194, Dec. 2007.
- [4] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application—Part II: Full device model and circuit performance benchmarking," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.
- [5] H.-S. P. Wong, J. Appenzeller, V. Derycke, R. Martel, S. Wind, and P. Avouris, "Carbon nanotube field effect transistors—Fabrication, device physics, and circuit implications," in *Proc. Int. Solid State Circuits Conf.*, 2003, pp. 370–371.
- [6] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," in *Proc. Int. Electron Devices Meeting*, Dec. 2004, pp. 703–706.
- [7] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, "Carbon nanotube field-effect transistors with integrated ohmic contacts and high-K gate dielectrics," *Nano Lett.*, vol. 4, pp. 447–450, 2004.
- [8] N. Patil, A. Lin, E. Myers, H.-S. P. Wong, and S. Mitra, "Integrated wafer-scale growth and transfer of directional carbon nanotubes and misaligned-carbon-nanotube-immune logic structures," in *Proc. '08 Symp. VLSI Technol.*, pp. 205–206.
- [9] N. Patil, J. Deng, H.-S. P. Wong, and S. Mitra, "Automated design of misaligned-carbon-nanotube-immune circuits," in *Proc. Design Autom. Conf.*, 2007, pp. 958–961.
- [10] S. Han, X. Liu, and C. Zhou, "Template-free directional growth of single-walled carbon nanotubes on a- and r-plane sapphire," *J. Am. Chem. Soc.*, vol. 127, pp. 5294–5295, 2005.
- [11] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nature Nanotechnol.*, vol. 2, pp. 230–236, 2007.
- [12] C. Kocabas, M. Shim, and J. A. Rogers, "Spatially selective guided growth of high-coverage arrays and random networks of single-walled carbon nanotubes and their integration into electronic devices," *J. Am. Chem. Soc.*, vol. 128, pp. 4540–4541, 2006.
- [13] S. Byers, "Thermal fracture of quartz," thesis, Case Western Reserve University, Cleveland, Ohio, 1974.
- [14] A. R. Cooper, "Fracture probability of quartz crystals cooled through the alpha-beta phase transformation," Case Western Reserve University, Tech. Rep., 1975.
- [15] P. G. Collins, M. S. Arnold, and P. Avouris, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown," *Science*, vol. 292, pp. 706–709, 2001.
- [16] A. Lin, N. Patil, K. Ryu, A. Badmaev, L. G. D. Arco, C. Zhou, S. Mitra, and H.-S. P. Wong, "Threshold voltage and on-off ratio tuning for multiple-tube carbon nanotube FETs," *IEEE Trans. Nanotechnol.*, vol. 8, no. 1, pp. 4–9, Jan. 2009.
- [17] G. Zhang, P. Qi, X. Wang, Y. Lu, X. Li, R. Tu, S. Bangsaruntip, D. Mann, L. Zhang, and H. Dai, "Selective etching of metallic carbon nanotubes by gas-phase reaction," *Science*, vol. 314, pp. 974–977, 2006.
- [18] J. Zhang, N. Patil, and S. Mitra, "Design guidelines for metallic-carbon-nanotube-tolerant digital logic circuits," in *Proc. Design Autom. Test Eur.*, 2008, pp. 1009–1014.



Nishant Patil (M'03) received the B.S. (Hons.) degree in electrical and computer engineering, with a minor in physics, from Carnegie Mellon University, Pittsburgh, PA, in 2004, and the M.S. degree in electrical engineering, in 2006, from Stanford University, Stanford, CA, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include design and fabrication of carbon nanotube FETs and circuits.

Mr. Patil is a recipient of the Stanford School of Engineering Fellowship Award and the Art and Mary Fong Stanford Graduate Fellowship Award.



Albert Lin (S'07) received the B.S. degree in electrical engineering and computer science and the M.Eng. degree in electrical engineering and computer science, with a minor in biomedical engineering, from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 2004 and 2006, respectively. He is currently working toward the Ph.D. degree in electrical engineering at Stanford University, Stanford, CA.

He is interested in exploring how nanotechnology can emerge to become the future of large-scale ICs.

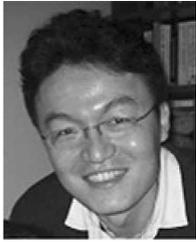
His current research interests in carbon nanotubes include material synthesis, novel transistor device structures, VLSI fabrication and processing, and circuit design.

Mr. Lin is a recipient of the Siebel Scholar Fellowship Award and the Stanford Fellowship Award for Graduate Study.



Edward R. Myers received the B.S. degree in metallurgy and mining from the University of Illinois, Urbana-Champaign and the M.S. and Ph.D. degrees in material science from North Carolina State University, Raleigh. He is a Research Engineer at the Stanford Nanofabrication Facility, Stanford, CA. He is a Material Scientist having over 20 years of experience in electronics and fabrication research in semiconductors, ferroelectric nonvolatile memories, field emission flat-panel displays, and large-area solid-state p-i-n X-ray sensors for digital medical imaging applications and electronic detection of DNA. He has over 20 technical publications.

He developed, co-chaired, and edited the successful sequence of MRS symposiums on "Ferroelectric Thin Films." He has given invited presentations at the Northern California's IEEE and TMS Annual Electronic Materials Symposium, was a Distinguished Lecturer at Northern Telecom Limited, Ottawa, ON and Gennum Corporation, Burlington, ON. Currently, he is a Core2 co-PI at the Stanford University Center for Cancer Nanotechnology Excellence Focused on Therapy Response, funded by the National Institutes of Health, Bethesda, MD.



Kounghmin Ryu received the B.S. degree in metallurgy and the M.S. degree in materials science and engineering from Hanyang University, Seoul, Korea, in 1998 and 2000, respectively. Since 2004, he has been working toward the Ph.D. degree at the University of Southern California (USC), Los Angeles, CA.

He was a Chemical Vapor Deposition (CVD) Process Engineer at Samsung Electronics for four years. He is the author or coauthor of three journal papers related to carbon nanotubes synthesis and organic LED (OLED) fabrication. His current research interests include carbon nanotube synthesis and applications such as nanotube circuits using aligned carbon nanotubes, chemical sensing, and OLED fabricated by carbon nanotube conductive films.



Alexander Badmaev received the B.S. and M.S. degrees in applied physics and mathematics from Moscow Institute of Technology, Moscow, Russia, in 2003 and 2005, respectively. He is currently working toward the Ph.D. degree at the University of Southern California (USC), Los Angeles, CA.

His current research interests include carbon nanotube nanoelectronics such as integrated logic and RF devices.



Chongwu Zhou received the Ph.D. degree in electrical engineering from Yale University, New Haven, CT, in 1999.

From 1999 to 2000, he was a Postdoctoral Researcher at Stanford University, Stanford, CA. In 2000, he joined the University of Southern California (USC), Los Angeles, CA, as an Assistant Professor. He has authored or coauthored more than 70 journal publications. His work has been reported by Science, Scientific American, Physics Today, Materials Research Society (MRS) Bulletin, Materials Today, National Cancer Institute, and Royal Society of Chemistry. His current research interests include semiconductive oxide nanowires, transition metal-oxide nanowires, carbon nanotubes, and chemical and biosensing.

Dr. Zhou is an Associate Editor for the IEEE TRANSACTIONS ON NANOTECHNOLOGY. He is the recipient of a number of awards, including the National Science Foundation (NSF) CAREER Award, the National Aeronautics and Space Administration (NASA) Turning Goals into Reality (TGIR) Award, the USC Junior Faculty Research Award, and the IEEE Nanotechnology Early Career Award.



H.-S. Philip Wong (S'81-M'82-SM'95-F'01) was at IBM Research, T. J. Watson Research Center, New York, for 16 years, where he worked on charged-couple device (CCD) and complementary metal-oxide-semiconductor (CMOS) image sensors, double-gate/multigate MOSFET, device simulations for advanced/novel MOSFET, strained silicon, wafer bonding, ultrathin body silicon on insulator (SOI), extremely short gate FETs, germanium MOSFET, carbon nanotube FET, and phase change memory. He held various positions from Research Staff Member to Manager and Senior Manager. While he was Senior Manager, he had

the responsibility of shaping and executing IBM's strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology. In September 2004, he joined Stanford University, Stanford, CA. His current research interests include nanoscale science and technology, semiconductor technology, solid-state devices, electronic imaging, exploring new materials, novel fabrication techniques, and novel device concepts for future nanoelectronic systems.

Prof. Wong is a member of the Emerging Research Devices Working Group of the International Technology Roadmap for Semiconductors (ITRS). From 2001 to 2006, he served on the IEEE Electron Devices Society (EDS) as elected AdCom member. From 1998 to 2007, he served on the International Electron Devices Meeting (IEDM) Committee, and was the Technical Program Chair in 2006 and General Chair in 2007. From 1998 to 2004, he served on the International Solid State Circuits Conference (ISSCC) Program Committee, and was the Chair of the Image Sensors, Displays, and Microelectromechanical Systems (MEMS) subcommittee from 2003 to 2004. Currently, he serves on the Executive Committee of the Symposia of very large-scale integration (VLSI) Technology and Circuits. From 2005 to 2006, he was the Editor-in-Chief of the IEEE TRANSACTIONS ON NANOTECHNOLOGY. He is also a Distinguished Lecturer of the IEEE Electron Devices Society and also a Distinguished Lecturer of the IEEE Solid State Circuits Society. He has taught several short courses at the IEDM, ISSCC, Symposium VLSI Technology, SOI Conference, and the International Society for Optical Engineering (SPIE) conferences.



Subhasish Mitra (SM'06) received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA.

He was a Principal Engineer at Intel Corporation. He is currently an Assistant Professor in the Departments of Electrical Engineering and Computer Science, Stanford University, where he leads the Stanford Robust Systems Group. He has authored or coauthored more than 100 technical papers, and has invented design and test techniques that have seen widespread proliferation in the chip design industry.

His X-compact technique for test compression is used by more than 50 Intel products, and is supported by major computer-aided design (CAD) tools. His recent work on imperfection-immune circuit design using carbon nanotubes has been highlighted in the Massachusetts Institute of Technology (MIT) Technology Review, EE Times, and several other publications. His current research interests include robust system design, VLSI design, CAD and test, and design for emerging nanotechnologies.

Prof. Mitra is the recipient of the National Science Foundation CAREER Award, Terman Fellowship Award, IEEE Circuits and Systems Society Donald O. Pederson Award for the best paper published in the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, Association for Computing Machinery (ACM) Special Interest Group on Design Automation (SIGDA) Outstanding New Faculty Award, Best Paper Award at the IEEE/ACM Design Automation Conference, a Divisional Recognition Award from Intel "for a Breakthrough Soft Error Protection Technology," a Best Paper Award at the Intel Design and Test Technology Conference for his work on Built-In Soft Error Resilience, and the Intel Achievement Award, Intel's highest corporate honor, "for the development and deployment of a breakthrough test compression technology." He has held several consulting positions, and served on committees of several IEEE and ACM conferences and workshops as Cofounder, General and Program Chair, and organizing and program committee member.