Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications

Chuan Wang,[†] Jialu Zhang,[†] Koungmin Ryu, Alexander Badmaev, Lewis Gomez De Arco, and Chongwu Zhou*

Department of Electrical Engineering, University of Southern California, Los Angeles, CA 90089

ABSTRACT

Preseparated, semiconductive enriched carbon nanotubes hold great potential for thin-film transistors and display applications due to their high mobility, high percentage of semiconductive nanotubes, and room-temperature processing compatibility. Here in this paper, we report our progress on wafer-scale processing of separated nanotube thin-film transistors (SN-TFTs) for display applications, including key technology components such as wafer-scale assembly of high-density, uniform separated nanotube networks, high-yield fabrication of devices with superior performance, and demonstration of organic light-emitting diode (OLED) switching controlled by a SN-TFT. On the basis of separated nanotubes with 95% semiconductive nanotubes, we have achieved solution-based assembly of separated nanotube thin films on complete 3 in. Si/SiO$_2$ wafers, and further carried out wafer-scale fabrication to produce transistors with high yield (>98%), small sheet resistance ($\sim$25 kΩ/sq), high current density ($\sim$10 μA/μm), and superior mobility ($\sim$52 cm^2 V^{-1} s^{-1}). Moreover, on/off ratios of >10^4 are achieved in devices with channel length L > 20 μm. In addition, OLED control circuit has been demonstrated with the SN-TFT, and the modulation in the output light intensity exceeds 10^4. Our approach can be easily scaled to large areas and could serve as critical foundation for future nanotube-based display electronics.

As the most widely used channel material for thin-film transistors (TFTs), amorphous silicon suffers from drawbacks that it requires high-temperature processing and the mobility is relatively low.[1-6] Organic TFTs as a replacement for amorphous silicon based TFTs receives lots of attention, while on the other hand they also suffer from poor device mobility.[7,8] Single-walled carbon nanotubes (SWNTs) offers high intrinsic carrier mobility and current-carrying capacity and have already been used to demonstrate ballistic and high mobility transistors,[9-11] and integrated logic circuits such as inverters and ring-oscillators.[12-16] Thin-films of SWNTs that possess extraordinary conductivity, transparency, and flexibility have been achieved using either solution-based filtration or chemical vapor deposition (CVD) growth, and TFTs based on SWNTs have also been demonstrated and offer outstanding electrical properties as expected.[17-23] However, all of the work mentioned above shares the same drawback, which is the coexistence of both metallic and semiconductive nanotubes with approximate 33% nanotubes being metallic. Recently, significant advance has been made on CVD grown nanotube networks for flexible devices and circuits by using stripe-patterning to remove heterogeneous percolative trans-

port through metallic nanotube networks and increase the average device on/off ratio to 10^4. This technique nevertheless requires additional fabrication steps of stripe patterning and large device dimensions.[24]

Alternatively, the problem of the coexistence of metallic and semiconductive nanotubes can be solved by using preseparated semiconductive enriched nanotubes produced by density gradient ultracentrifugation.[25,26] On the basis of the separated nanotubes, TFTs have been demonstrated by the IBM research group. Ninety-nine percent semiconductive nanotubes were deposited using a sophisticated evaporation self-assembly method and the devices exhibited on/off ratios of more than 10^3 with channel length L = 4 μm, sheet resistance of $\sim$200 kΩ/sq, and mobility of $\sim$10 cm^2 V^{-1} s^{-1}.[27] Despite the significant progress, many interesting issues remain to be studied. For example, can one use a simple and reliable method to assemble nanotubes besides the evaporation self-assembly method? What are the key factors affecting the TFT performance? Can one achieve even better TFT performance with separated nanotubes of less demanding purities (<99%)?

To answer the above-mentioned questions, we report our recent advance on wafer-scale processing of SN-TFTs and their potential application in display electronics. Surprisingly,

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* To whom correspondence should be addressed. E-mail: chongwuz@usc.edu.
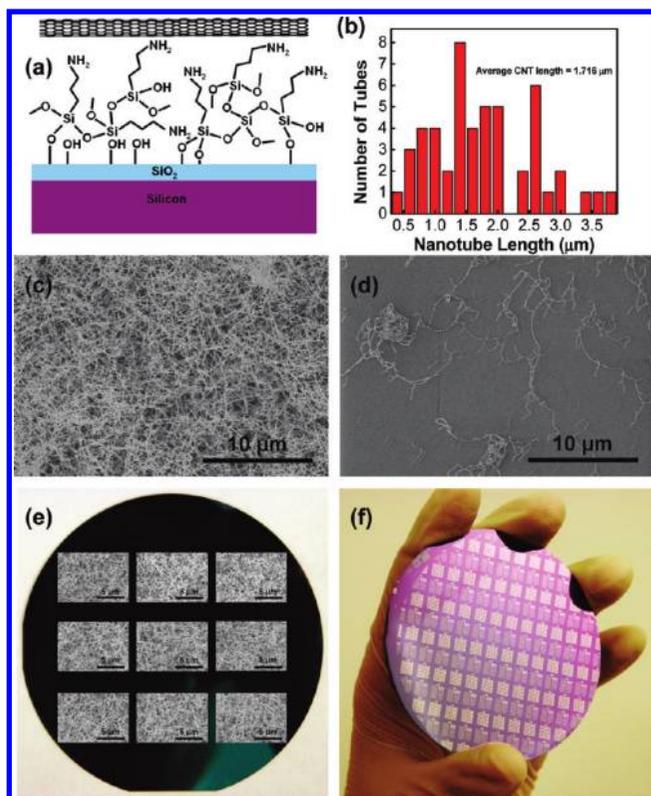† These authors contributed equally to this work.

Figure 1. Wafer-scale deposition of separated carbon nanotubes and fabrication of SN-TFTs. (a) Schematic diagram of APTES assisted nanotube deposition on Si/SiO$_2$ substrate. (b) Length distribution of the separated nanotubes used in this study; the average nanotube length is 1.716 μm. (c, d) FE-SEM images of separated nanotubes deposited on Si/SiO$_2$ substrates with (c) and without (d) APTES functionalization, respectively. (e) Photograph of 3 in. Si/SiO$_2$ wafer after APTES assisted nanotubes deposition. Inset: FE-SEM images showing nanotubes deposited at different locations on the wafer, the locations of the SEM images on the wafer correspond to the approximate locations on the wafer where the images were taken. All the scale bars are 5 μm. (f) Photograph of the same wafer after electrode patterning. The wafer consists of SN-TFTs used in this study and other types of electronic devices. Such SN-TFTs are made with channel width (*W*) of 10, 20, 50, 100, and 200 μm, and channel length (*L*) of 4, 10, 20, 50, and 100 μm.

we have produced TFTs using only 95% enriched semiconductive nanotubes with overall better performance than previous work[27] using 99% enriched nanotubes. Our work includes the following essential components. (1) Uniform and high density separated nanotube thin-films were deposited onto 3 in. Si/SiO$_2$ wafers using a facile solution-based assembly method. (2) Wafer-scale device fabrication was performed on 3 in. Si/SiO$_2$ wafers to yield SN-TFTs with high yield (>98%), small sheet resistance ($\sim$ 25kΩ/sq), high current density ($\sim$10 μA/μm), high mobility ($\sim$52 cm^2 V^{-1} s^{-1}), and good on/off ratio (>10^4). (3) OLED control circuit has been demonstrated using the SN-TFT with output light intensity modulation over 10^4. Our wafer-scale processing of SN-TFTs shows significant advantage over conventional platforms with respect to scalability, reproducibility, and device performance and suggests a practical and realistic approach for nanotube-based integrated circuit applications.

Figure 1 illustrates our wafer-scale processing of SN-TFTs including aminosilane assisted nanotube deposition and

device fabrication. In order to improve the density and uniformity of the solution-based nanotube assembly, aminosilane is introduced due to its well-known affinity to the carbon nanotubes.[28,29] In this work, aminopropyltriethoxy silane (APTES) is used to functionalize the Si/SiO$_2$ surface to form amine-terminated monolayer and the schematic of the APTES-assisted deposition is shown in Figure 1a. The detailed procedure of wafer-scale separated nanotube assembly begins with using corona discharge generator to generate UV ozone to clean the surface of the Si/SiO$_2$ wafer making it hydrophilic. Next, the cleaned wafer is immersed into diluted APTES solution (3 drops of APTES in 20 mL of isopropanol alcohol (IPA)) for 10 min, then rinsed with IPA, and blown dry thoroughly. After APTES functionalization, the wafer is immersed into 0.01 mg/mL separated nanotube solution with 95% semiconducting nanotube prepared using density gradient ultracentrifugation[25,26] for 20 min. The enrichment of semiconducting nanotubes in the separated nanotube solution is confirmed by UV−vis-NIR absorption spectroscopy and the result is shown in Supporting Information (S1). The length distribution of the semiconductive nanotubes is measured by field-emission scanning electron microscope (FE-SEM) and the results are shown in Figure 1b. The average length is measured to be 1.7 μm, which is longer than 1 μm for 99% semiconducting nanotubes as reported in the literature.[27] As a final step, IPA and deionized water rinsing are used to remove the sodium dodecyl sulfate (SDS) residuals on the nanotubes, and the wafer is blown dry with N$_2$.

FE-SEM was used to inspect the surface after nanotube assembly. Figure 1 panels c and d are the SEM images of the separated nanotubes deposited on Si/SiO$_2$ substrates with and without APTES functionalization, respectively. From the image, one can find that the sample with APTES functionalization gives much higher nanotube density (24−32 tubes/μm^2) than the sample without APTES (<0.5 tubes/μm^2). Besides high density, APTES functionalization also helps to give uniform deposition throughout the wafer. Figure 1e shows the photograph of a 3 in. Si/SiO$_2$ wafer after APTES assisted nanotube deposition. There is no abnormal color or junk left on the wafer after the deposition and cleaning process. In order to determine the deposition uniformity, SEM images were taken at nine different locations on the wafer. In Figure 1e, the locations of the SEM images on the wafer correspond to the approximate locations on the wafer where the images were taken and all the scale bars correspond to 5 μm. The SEM images indicate that high density, uniform deposition is achieved throughout the 3 in. wafer.

Following the nanotube deposition is the device fabrication process. SiO$_2$ (50 nm) is used to act as the back-gate dielectric. The source and drain electrodes are patterned by photolithography, and 5 Å Ti and 70 nm Pd are deposited followed by the lift-off process to form the source and drain metal contacts. Finally, since the separated nanotube thin film cover the entire wafer, to achieve accurate channel length and width and to remove the possible leakage in the devices, one more step of photolithography plus O$_2$ plasma is used to remove the unwanted nanotubes outside the device
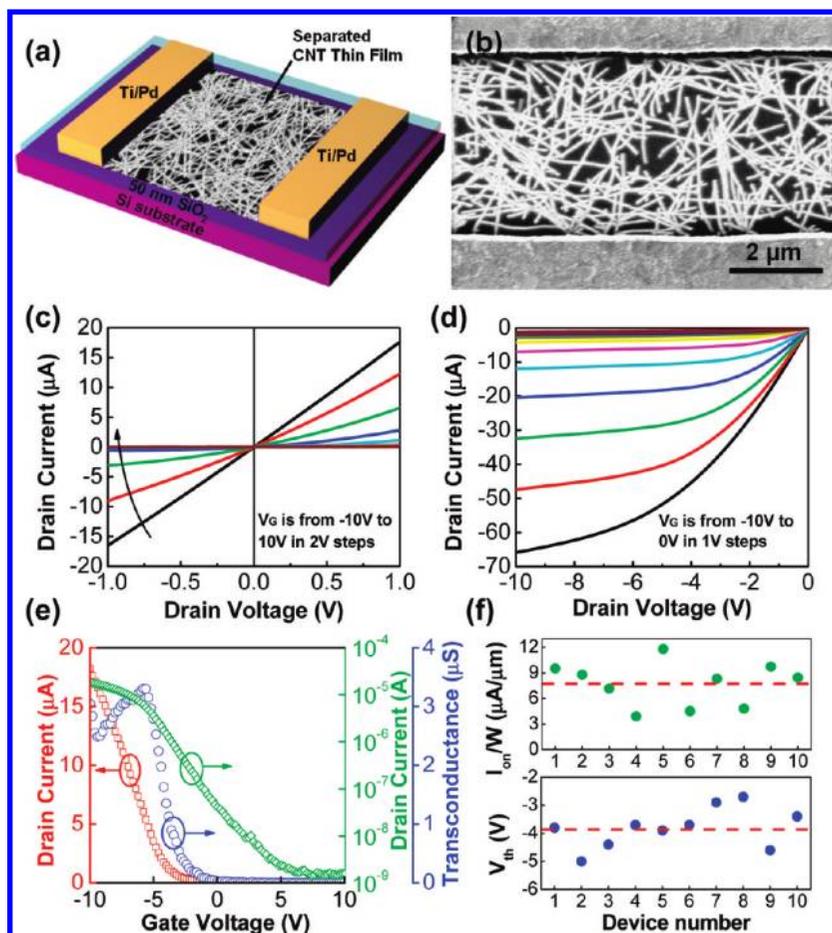
Figure 2. Electronic properties of back-gated SN-TFTs. (a) Schematic diagram of a back-gated transistor built on separated nanotube thin-film with Ti/Pd (5 Å/70 nm) contacts and SiO_2 (50 nm) gate dielectric. (b) FE-SEM image of a typical SN-TFT with 4 μm channel length. (c,d) Output (I_D-V_D) characteristics of a typical SN-TFT ($L = 20$ μm and $W = 100$ μm) in triode region (c) and saturation region (d), respectively. (e) Transfer (I_D-V_G) characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of the same device with $V_D = 1$ V. (f) Current density (I_{on}/W) measured at $V_D = 1$ V and threshold voltage (V_{th}) of 10 representative SN-TFTs showing the uniformity of devices. The red line represents the average value.

channel region. Figure 1f is a photograph of the wafer after electrode patterning. The wafer consists of SN-TFTs used in this study and other types of electronic devices. Such SN-TFTs are made with channel width (W) of 10, 20, 50, 100, and 200 μm, and channel length (L) of 4, 10, 20, 50, and 100 μm.

We carried out a systematic study of the electrical performance of the SN-TFTs as basic components for macroelectronic integrated circuits and display electronics. Figure 2a shows the schematic diagram of a back-gated SN-TFT built on separated nanotube thin-film with Ti/Pd (5 Å/70 nm) contacts and SiO_2 (50 nm) gate dielectric. The SEM image of the channel of a typical SN-TFT with 4 μm channel length is shown in Figure 2b. Figure 2c,d is the output (I_D-V_D) characteristics of a typical SN-TFT ($L = 20$ μm, and $W = 100$ μm) measured in triode region and saturation region, respectively. The I_D-V_D curves appear to be very linear for V_D between -1 and 1 V, indicating that ohmic contacts are formed between the electrodes and the nanotubes. Under more negative V_D, these devices typically exhibit saturation behavior, as shown in Figure 2d. Figure 2e shows the transfer (I_D-V_G) characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of

the same representative device with $V_D = 1$ V. The on-current at $V_D = 1$ V is measured to be 18.5 μA, corresponding to a current density of 0.185 μA/μm. The on/off ratio exceeds 10^4 and the transconductance is 3.3 μS. Furthermore, due to the high density and uniform nature of the separated nanotube thin-film deposited on Si/SiO_2 substrates with APTES functionalization, the SN-TFTs are also expected to behave uniformly. The uniformity of the devices is illustrated in Figure 2f, which shows the current density (I_{on}/W) measured at $V_D = 1$ V and threshold voltage (V_{th}) of 10 representative SN-TFTs with $L = 4$ μm. The red lines represent the average values and one can find that those device parameters have much smaller distribution compared with single nanotube devices.

CVD grown nanotube thin-films with mixed nanotubes have also been used to demonstrate TFTs and significant advance has been made toward flexible devices and integrated circuits.[19,22,24] However, the major problem of using CVD grown nanotube networks is the coexistence of metallic and semiconductive nanotubes with approximate 33% nanotubes being metallic. Stripe-patterning of CVD nanotube network has been proposed to remove heterogeneous percolative transport through metallic nanotube networks and
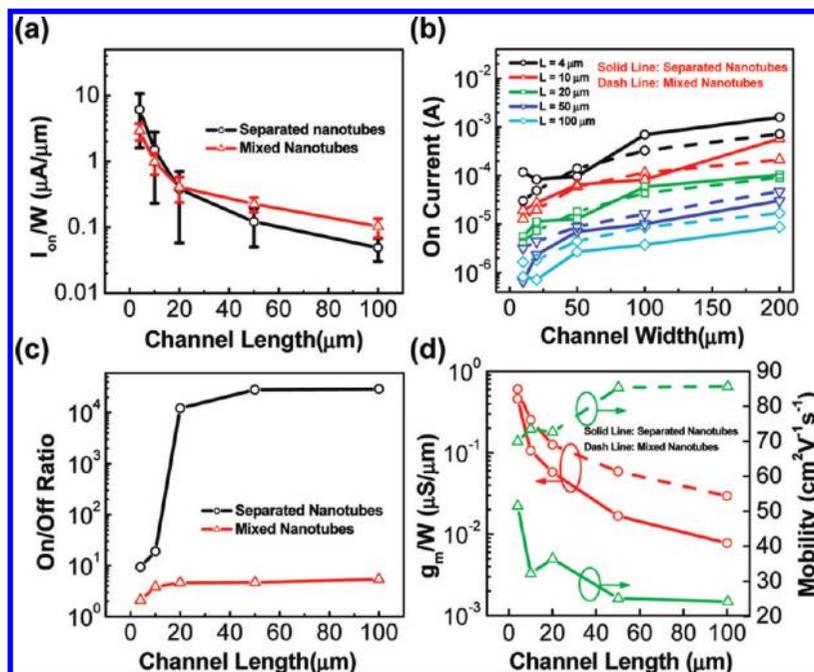
Figure 3. Statistical study of 200 nanotube TFTs based on separated nanotubes and mixed nanotubes. (a) Plot of current density (I_{on}/W) versus channel length for TFTs fabricated on separated nanotubes and mixed nanotubes. (b) Plot of average on current (I_{on}) versus channel width for TFTs fabricated on separated nanotubes and mixed nanotubes with various channel lengths (4, 10, 20, 50, 100 μm). (c) Plot of average on/off ratio (I_{on}/I_{off}) versus channel length for TFTs fabricated on separated nanotubes and mixed nanotubes. (d) Plot of average transconductance per unit width (g_m/W) and average device mobility (μ_{device}) versus channel length for TFTs fabricated on separated nanotubes and mixed nanotubes.

increase the average device on/off ratio to 10^4. Nevertheless, this technique requires additional fabrication steps and large device dimensions.

To get a more comprehensive understanding, we compare the performance of SN-TFTs based on separated nanotubes (5% metallic) with TFTs based on CVD grown mixed nanotubes (33% metallic). The CVD recipe was fine-tuned to produce TFTs with a current drive (I_{on}/W) similar to SN-TFTs. More information about TFTs based on CVD grown nanotubes can be found in Supporting Information (S2). Figure 3 summarizes the results after the measurement of 200 nanotube TFTs with various channel lengths and channel widths. Half of these devices are based on separated nanotubes and the other half based on mixed nanotubes. The device yield is more than 98%, and the few unconductive devices are due to the peel-off of metal contact during fabrication process.

Figure 3a exhibits the average normalized on-current densities (I_{on}/W) of the transistors with various channel lengths measured at $V_D = 1$ V and $V_G = -10$ V, showing that the on-current density is approximately reversely proportional to the channel length. The highest on-current density is measured to be 10 μA/μm and is achieved in devices with $L = 4$ μm. This value is comparable to the devices based on parallel aligned nanotubes with a typical nanotube density of 5 tubes/μm.[31,32] Figure 3b shows that the average on-current of the TFTs with various channel lengths is approximately proportional to the channel width. The highest average on-current 1.59 mA is achieved in devices with $L = 4$ μm and $W = 200$ μm. On the basis of the information in Figure 3b, we can further extract the best

sheet resistance of the separated nanotube thin-film to be $\sim$25 kΩ/sq, which is 8 times better than 200 kΩ/sq reported in the previous publication.[27]

For TFTs fabricated with separated nanotubes and mixed nanotubes, the major difference is expected to be the on/off ratio, and the difference is explained in Figure 3c. First of all, as the channel length increases, the average on/off ratio of both SN-TFTs and mixed nanotube TFTs increases. This can be explained by the decrease in the probability of percolative transport through metallic nanotube networks as the device channel length increases. On the other hand, SN-TFTs have much higher on/off ratio compared with mixed nanotube TFTs due to the small percentage of metallic nanotubes. For the mixed nanotube TFT with 33% metallic nanotubes, the on/off ratio stays in the range of 2−10 as the channel length increases from 4 to 100 μm. In contrast, for SN-TFT with only 5% metallic nanotubes the on/off ratio improves significantly from 10 to above 10^4 as the channel length increases from 4 to 100 μm. The turning point happens between 10 and 20 μm. When $L > 20$ μm, more than 90% of the devices exhibit on/off ratio higher than 10^3. This amount of on/off ratio is large enough for most kinds of integrated circuit applications. Similar results have also been reported in previous work done by the IBM research group.[27] For their work, the turning point happens between 2 and 4 μm. The reason that their turning point happens at smaller channel length is that they used 99% semiconductive nanotubes. By using higher purity semiconductive enriched nanotubes, on the one hand it can help to achieve sufficient on/off ratio with smaller channel length, thus smaller device area; on the other hand, since higher purity requires more
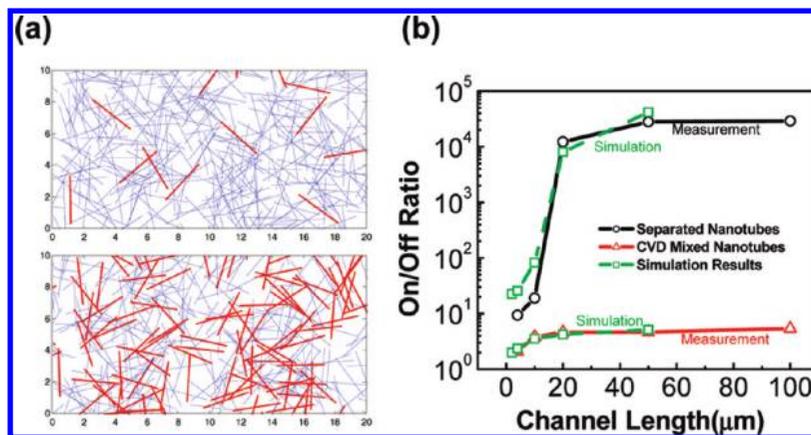
Figure 4. Simulation of nanotube thin-film percolation network. (a) Randomly generated nanotube percolation networks of separated nanotubes (top) and mixed nanotubes (bottom) for devices with $L = 10 \, \mu$m and $W = 20 \, \mu$m. The red and blue lines represent metallic and semiconductive nanotubes, respectively. (b) Comparison between the simulation data derived from the percolation network and measurement data.

ultracentrifugation, which will give rise to shorter nanotube length, it can cause more nanotube percolation and hurt the mobility of the devices as discussed below.

Besides the on current density and on/off ratio, there are two more important figures of merit for SN-TFTs, which are device transconductance (g_m) and mobility (μ_{device}). The normalized device transconductance (g_m/W) and mobility of devices with various channel lengths are characterized and are plotted in Figure 3d. g_m is extracted from the maximum slope of the transfer characteristics measured at $V_D = 1$ V and is normalized to device channel width. From the figure, one can find that as channel length increases, g_m/W decreases, this is because g_m/W is also inversely proportional to channel length.

On the basis of the normalized transconductance, we can further extract the mobility of the nanotube thin-film. We note that the SN-TFTs exhibit hysteresis as shown in the Supporting Information (S3). For consistency, we used g_m derived from the forward sweep for all the mobility calculations. Under $V_D = 1$ V, devices operate in triode region, so the device mobility can be calculated from the following equation

$$\mu_{device} = \frac{L}{V_d C_{ox} W} \cdot \frac{dI_d}{dV_g} = \frac{L}{V_D C_{ox}} \cdot \frac{g_m}{W}$$

where L and W are the device channel length and width, $V_D = 1$ V, and C_{ox} is the gate capacitance per unit area. The capacitance is calculated by considering the electrostatic coupling between nanotubes[33] and more details about the calculation can be found in Supporting Information (S4). For the device mobility, one interesting finding is that for the SN-TFTs, the device mobility decreases as channel length increases, while for the mixed nanotube TFTs, the device mobility increases as channel length increases. The highest mobility of SN-TFTs is 52 cm^2 V^{-1} s^{-1} and is achieved in devices with $L = 4 \, \mu$m, while the highest mobility of mixed nanotube TFTs is 86 cm^2 V^{-1} s^{-1} and is achieved in devices with $L = 100 \, \mu$m. The reason for the difference is believed to be related to nanotube length. For the separated nanotubes, the average length is small and is measured to be 1.7 μm, so the device mobility is limited by the percolative transport through nanotube network. As the device channel length

increases from a value comparable to the nanotube length to a much larger value, there are significantly more tube-to-tube junctions introduced into the conduction path, causing the device mobility to decrease. In contrast, for the mixed nanotubes the average length is much larger (>20 μm), so the device mobility is likely to be limited by the metal/nanotube contacts, similar to the case for aligned nanotube transistors.[30−32] As the channel length increases, the effect of metal/nanotube contacts become less significant and the mobility increases. Our SN-TFTs exhibit mobility up to 52 cm^2 V^{-1} s^{-1} which is more than five times higher than the previously reported work (10 cm^2 V^{-1} s^{-1}).[27] Our improvement in the device performance can be attributed to longer nanotube length as described before. For instance, the average nanotube length in our SN-TFTs is approximately 1.7 μm, while the nanotube length is about 1 μm for previous work. For transistors of similar channel length, using longer nanotubes would lead to less nanotube−nanotube junctions and consequently higher mobility.

To further assess the effect of the carbon nanotube percolation network on the performance of nanotube TFTs,[34−36] a numerical simulation of nanotube TFTs with various channel lengths was performed to extract their on/off ratios. The simulation consists of the following steps. First, we generate random nanotube networks that are defined by the following parameters: density of nanotubes, nanotube length, percentage of metallic nanotubes, and channel length and width. The representative networks for separated nanotubes and mixed nanotubes are shown in Figure 4a. Then we calculate the resistance of a nanotube network in the on- and off-states, where we assume that the resistance per unit length of a semiconducting nanotube in the on-state to be equal to the resistance per unit length of a metallic nanotube, and 10^4 times larger in the off-state. We also assume fixed contact resistances between metallic/metallic, metallic/semiconductive, semiconductive/semiconductive nanotubes, and nanotubes/metal contacts. On the basis of the resistance in the on- and off-states calculated from the randomly generated carbon nanotube network, one can derive the on/off ratios of the devices. The simulation results are compared with the measurement results and are plotted in Figure 4b. On the basis of the figure, the simulation results fit the measurement
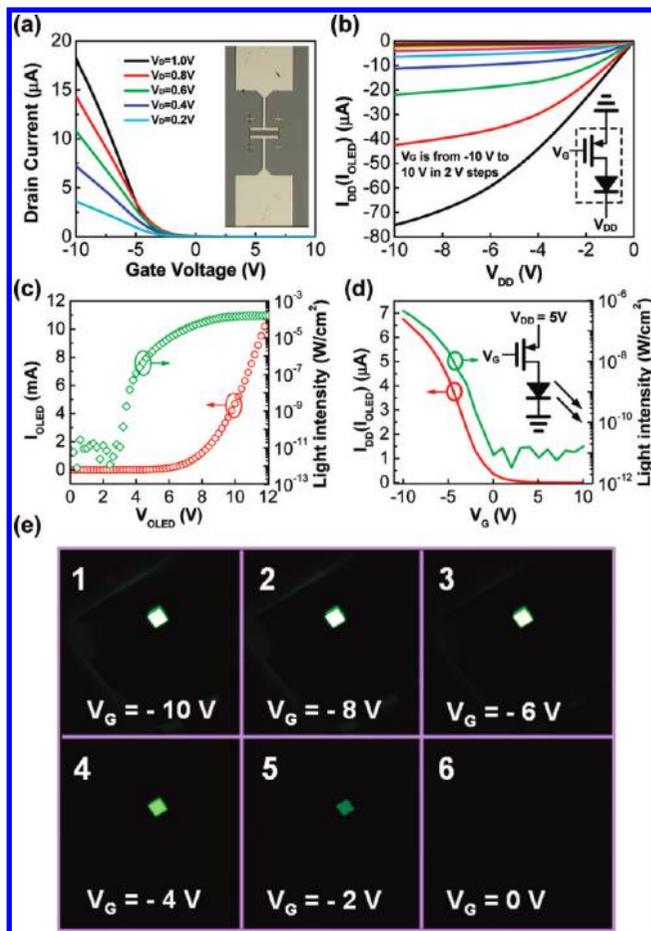
Figure 5. OLED control circuit by SN-TFT. (a) Transfer (I_D-V_G) characteristics under different drain voltages for the device used to control the OLED ($L = 20 \mu m$, and $W = 100 \mu m$), Inset: optical microscope image of the device. (b) Characteristics of the OLED control circuit where the current flow through the OLED (I_{OLED}) is measured by sweeping the V_{DD} and Input voltage V_G. Various curves correspond to various values of V_G from -10 to 10 V in 2 V steps. (c) Two terminal measurement of the OLED showing the current through the OLED (I_{OLED}) (red line) and OLED light intensity (green line) versus the voltage applied across the OLED (V_{OLED}). (d) Plot of the current through the OLED (I_{OLED}) (red line) and OLED light intensity (green line) versus V_G with $V_{DD} = 5$ V. Inset: The circuit diagram of an OLED driven by a SN-TFT. (e) Photographs of the OLED driven by SN-TFT under different inputs showing the turn on and turn off of the OLED.

results well, which indicate that the nanotube percolation indeed plays a critical role in determining the on/off ratios of nanotube TFTs.

Our ability to fabricate high performance, uniform, high on/off ratio SN-TFTs enable us to further explore their applications in display electronics. For the proof of concept purpose, an OLED was connected to and controlled by a typical SN-TFT device whose transfer characteristics are shown in Figure 5a. The OLED employed in this study is a standard NPD/Alq3 OLED with multilayered configuration given as ITO/4−4′-bis[N-(1-naphthyl)-N-phenyl-amino]bi-phenyl (NPD) [40 nm]/tris(8-hydroxyquinoline) aluminum (Alq3) [40 nm]/LiF [1 nm]/aluminum (Al) [100 nm]. The channel length of the SN-TFT is selected to be 20 μm so that the on/off reaches 10^4 and can meet the requirement for controlling the OLED to switch on and off. The schematic

of the OLED control circuit is shown in the inset of Figure 5b, where one SN-TFT is connected to an external OLED and V_{DD} (<0 V) is applied to the cathode of the OLED. The OLED control circuit is characterized by sweeping the V_{DD} and input voltage V_G and measuring the current flow through the OLED (I_{OLED}). It shows field effect transistor-like behavior with various curves corresponding to various values of input voltage. The figure illustrates that by controlling V_{DD} and V_G that worked as the input for the circuit, we can control the current flow through the OLED. To fully understand the behavior of the OLED, it is further character-ized and the current and output light intensity versus applied voltage behaviors are plotted in Figure 5c. From the figure, we can see that the OLED gives nice diode $I-V$ characteristic and in terms of the light intensity, the turn on voltage is about 3 V.

On the basis of the data in Figure 5b,c, we demonstrate the switching of the OLED by applying $V_{DD} = 5$ V to the source of the transistor and sweeping the input voltage V_G from -10 to 10 V. Figure 5d shows the current (red curve) flowing through the OLED, which is successfully modulated by V_G by a factor of 1140, and this modulation leads to the control of the OLED light intensity as shown in the green curve. When $V_G = -10$ V, the OLED is on, and on the basis of the measured light intensity, the brightness is calculated to be 16.5 Cd/m^2. When $V_G = 10$ V, the OLED is off and the brightness is calculated to be <0.001 Cd/m^2. The modulation in the OLED brightness is greater than 10^4 and the significant change in the light intensity can be visually seen as shown in Figure 5e. The optical photographs represent the OLED under various input voltages with 1, 2, 3, 4, 5, and 6 corresponding to the inputs of -10, -8, -6, -4, -2, and 0 V, respectively.

In summary, we have reported significant progress on wafer-scale processing of SN-TFTs for display applications, including progress on wafer-scale assembly of high density, uniform separated nanotube networks, high-yield fabrication of devices with good performance, and proof of concept demonstration of OLED switching controlled by a SN-TFT. The APTES-assisted solution-based assembly of separated nanotube thin-film has been achieved on complete 3 in. Si/SiO$_2$ wafers, followed by the fabrication to yield transistors with high yield (>98%), small sheet resistance ($\sim$25 kΩ/sq), high current density ($\sim$10 μA/μm), high mobility ($\sim$52 cm^2 V^{-1} s^{-1}) and good on/off ratio (>10^4). In addition, OLED control circuit has been demonstrated with the SN-TFT, and the modulation in the output light intensity exceeds 10^4. This demonstration can provide a guide to future research on SN-TFT-based display electronics such as active matrix organic light-emitting diode (AMOLED). Our work represents significant advance toward the challenging task of large scale separated nanotube thin-film assembly and solves the prob-lem of coexistence of both metallic and semiconductive nanotubes in the state-of-the-art nanotube transistor fabrica-tion techniques.

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