Rigid/Flexible Transparent Electronics Based on Separated Carbon Nanotube Thin-Film Transistors and Their Application in Display Electronics

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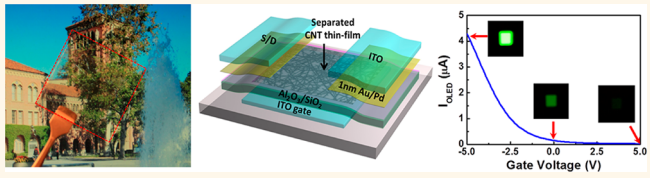
ABSTRACT



Transparent electronics has attracted numerous research efforts in recent years because of its promising commercial impact in a wide variety of areas such as transparent displays. High optical transparency as well as good electrical performance is required for transparent electronics. Preseparated, semiconducting enriched carbon nanotubes are excellent candidates for this purpose due to their excellent mobility, high percentage of semiconducting nanotubes, and room-temperature processing compatibility. Here we report fully transparent transistors based on separated carbon nanotube networks. Using a very thin metal layer together with indium tin oxide as source and drain contacts, excellent electrical performance as well as high transparency (~82%) has been achieved (350−800 nm). Also, devices on flexible substrates are fabricated, and only a very small variation in electric characteristics is observed during a flexibility test. Furthermore, an organic light-emitting diode control circuit with significant output light intensity modulation has been demonstrated with transparent, separated nanotube thin-film transistors. Our results suggest the promising future of separated carbon nanotube based transparent electronics, which can serve as the critical foundation for next-generation transparent display applications.

KEYWORDS: flexible and transparent transistors · carbon nanotubes · nanotube separation · thin-film transistors · transparent display

Since first proposed in 1997,[1] transparent electronics has attracted extensive attention due to its great potential in wide variety of areas including solar cells,[2] photodetectors,[3] and charge-coupled devices (CCDs).[4] Among all of those applications, transparent display is one of the most attractive and promising ones.[5−7] The major challenge for the realization of transparent displays is the development of high-performance transparent thin-film transistors with decent mobility, high current on/off ratio, low operation voltage, and low-temperature-compatible fabrication processing. Amorphous silicon,[8,9] polysilicon,[10,11] and organic materials[12,13] are possible candidates for transparent transistor channel materials, but they either suffer from low mobility and low transparency or require high-temperature processing.

Compared with the above channel materials, single-walled carbon nanotubes (SWNTs)[14−17] have advantages in terms of mobility, transparency, flexibility, and low-temperature processing. Transparent devices have already been reported previously by using both aligned carbon nanotube arrays and random nanotube networks.[18−20] However, those transistors share a common drawback, which is the coexistence of both metallic and semiconducting nanotubes, and therefore require addition steps such as electrical breakdown or stripe-patterning processing to improve the device's current on/off ratio, which would hurt the uniformity and mobility of the transistors. Recently, significant progress has been made by us and several other groups in the carbon nanotube thin-film transistor (TFT) direction. High-performance TFTs[21−25] have been demonstrated using preseparated semiconducting nanotubes produced by a density-gradient ultracentrifuge separation method.[26,27] In those previous reports, due to the use of high-purity semiconducting nanotubes, the transistors exhibit highly uniform electrical performance, high on/off ratio (>10^5), and excellent mobility (up to 67 $cm^2\ V^{-1}\ s^{-1}$), which make separated nanotube thin-film transistors (SN-TFTs) very attractive for transparent electronic applications.

In this paper, we report our recent advance on fully transparent, separated

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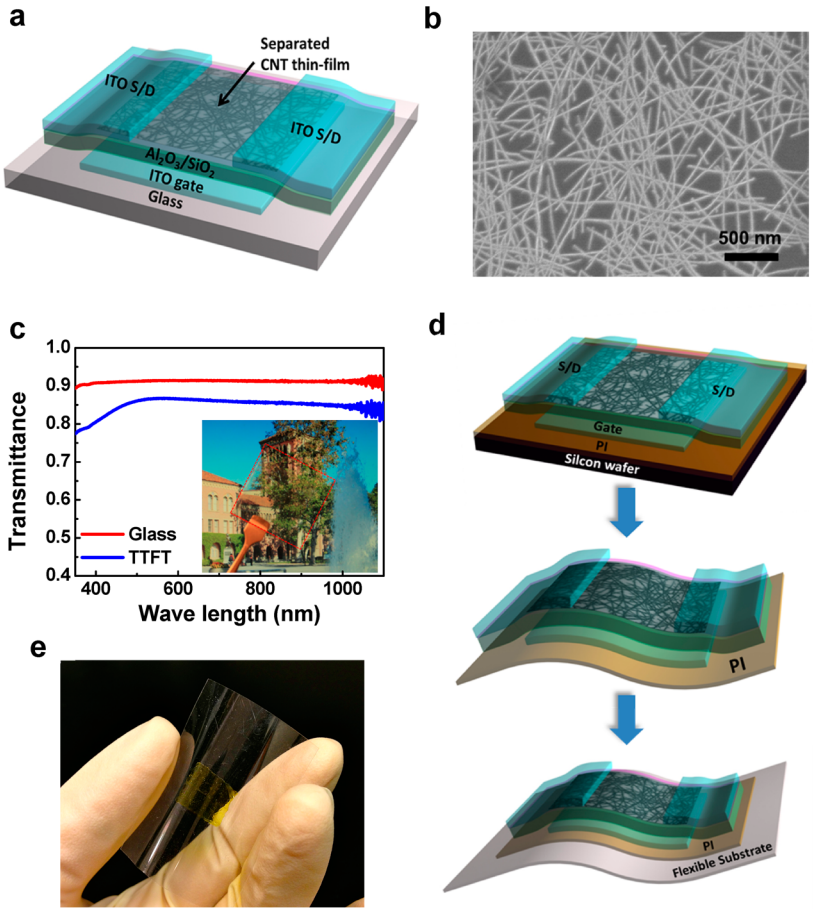

Figure 1. Fully transparent, separated carbon nanotube devices. (a) Schematic diagram of a transparent SN-TFT with ITO (100 nm) as back gate, Al_2O_3/SiO_2 (40 nm/5 nm) as gate dielectric, and ITO (100 nm) as source and drain contacts. (b) FE-SEM image of the separated carbon nanotube thin film inside the transistor channel region. (c) Optical transmittance of the bare glass substrate (red curve) and glass with arrays of transparent SN-TFTs with ITO contacts (blue curve). Inset: Optical image of the fully transparent SN-TFTs on a 2 in. square glass substrate with the substrate area marked with a red frame for clarity. (d) Schematic diagram showing the fabrication steps for transparent SN-TFTs on flexible substrates. (e) Optical image of transparent SN-TFTs on a PET substrate.

carbon nanotube thin-film transistors on both rigid and flexible substrates and their application in display electronics. Transparent SN-TFTs with uniformly assembled separated nanotube networks as channel material and indium tin oxide (ITO) as electrodes were fabricated on a glass substrate through a low-temperature process. In addition, we have investigated the contacts between ITO and naonotubes and introduced a thin metal layer (Au and Pd used) in between to improve the device performance. About 3-time device enhancement in terms of on-current and device mobility was achieved by adding the thin metal layers. Furthermore, transparent SN-TFTs were also fabricated on flexible substrates, and excellent flexibility was observed. Finally, as a demonstration, an OLED control circuit has been fabricated using the transparent SN-TFT with output light intensity modulation over 10^3. Our transparent SN-TFT platform shows significant advantages over conventional platforms with respect to low temperature processing compatibility, scalability, reproducibility, and device performance and suggests a practical and realistic approach for carbon-nanotube-based transparent devices, circuits, and display applications.

RESULTS AND DISCUSSION

Figure 1a illustrates our fully transparent SN-TFT device structure. The 98% semiconducting nanotubes obtained from NanoIntegris, Inc. (IsoNanotubes-S) were uniformly deposited onto the glass substrate with a prepatterned ITO back gate (100 nm) and Al_2O_3/SiO_2 (40 nm/5 nm) dielectric layer. We carried out separated nanotube deposition by using aminopropyltriethoxysilane (APTES) to functionalize the SiO_2 surface and then immersing the substrate in the nanotube solution as reported in our previous publications.[22,23] Following that, source and drain electrodes made of 100 nm ITO were sputter-coated and defined on top of the nanotube thin film by photolithography and lift-off techniques as described in the Methods section. Field-emission scanning electron microscopy (FE-SEM) was used to inspect the

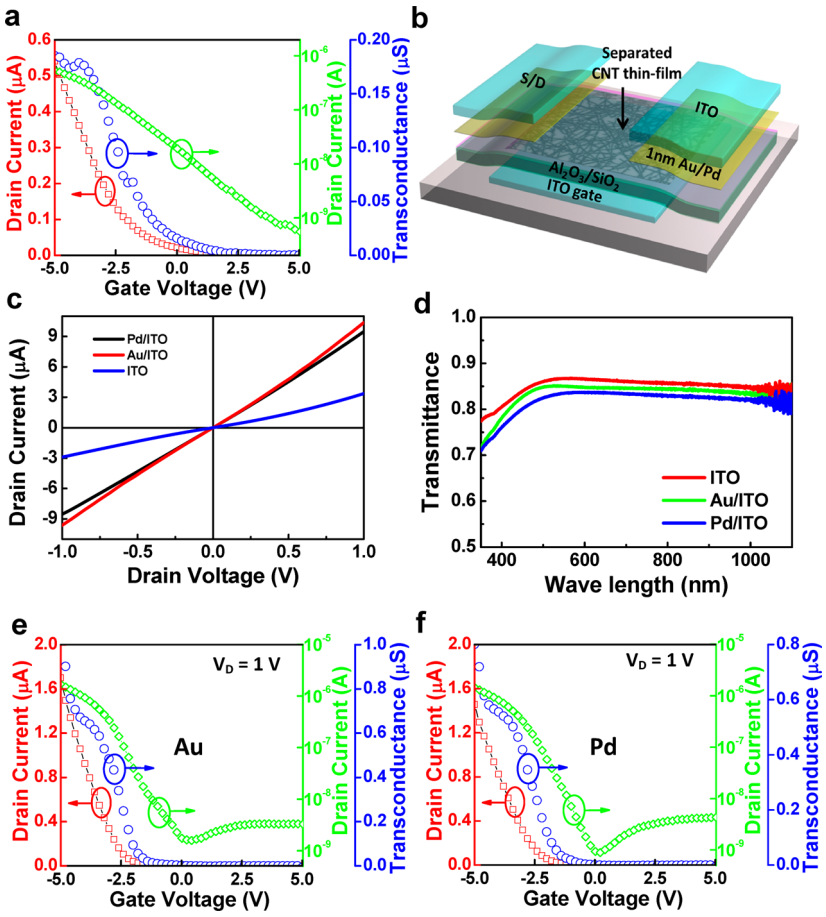

Figure 2. Transparent transistors with improved contacts. (a) Transfer (I_D-V_G) characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of a typical SN-TFT ($L = 100\ \mu$m, $W = 100\ \mu$m) with $V_D = 1$ V. (b) Schematic diagram of the improved transparent SN-TFT structure with Au/Pd + ITO as the source and drain contacts. (b) Transfer (I_D-V_G) characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of the same SN-TFT with $V_D = 1$ V. (c) Typical I_D-V_D plots for devices with the same channel geometry ($L = 20\ \mu$m, $W = 100\ \mu$m) but with Au/ITO (red), Pd/ITO (black), and ITO (blue) contacts under $V_G = -5$ V, respectively. (d) Optical transmittance of glass substrates with arrays of transparent SN-TFTs with Au/ITO (green curve), Pd/ITO (blue curve), and ITO (red curve) contacts. (e, f) Transfer (I_D-V_G) characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of the typical SN-TFTs ($L = 100\ \mu$m, $W = 100\ \mu$m) with Au/ITO (e) and Pd/ITO (f) contacts measured at $V_D = 1$ V, respectively.

surface after nanotube assembly. Figure 1b is a representative SEM image of the deposited separated nanotube thin film inside the transistor channel region on the glass substrate. From this image, one can find that high-density, monolayer nanotube networks are uniformly deposited on top of the Al_2O_3/SiO_2 dielectric layer. Nanotubes show very clean and smooth surfaces due to the cleaning process using DI water and isopropanol alcohol rinsing after deposition. The deposited nanotube density is around 30 tubes/μm^2, which is a desired density for transistor applications considering the trade-off between the device on-current and current on/off ratio studied in our previous work.[24]

Due to the excellent transparency of the CNT film and ITO electrodes, SN-TFT arrays on glass substrates have excellent transparency, as exhibited in Figure 1c, where the background can be easily seen through these devices fabricated on a 2 in. glass substrate (marked with red dash lines) in the inset photograph. The optical transmittance measurement in this plot shows that the sample with fabricated transparent SN-TFTs with ITO electrodes had a transmittance ~85% over the visible light regime (380−780 nm). In contrast, a similar glass substrate without any devices on top had a transmittance of ~90%, so the transparent SN-TFTs only decreased the transmittance from 90% to 85%.

Benefiting from the low-temperature fabrication process, transparent SN-TFTs can also be fabricated on flexible substrates. Flexible electronics is extremely attractive owing to its wearable and portable properties as well as compatibility with roll-to-roll fabrication.[7,12,13] Figure 1d illustrates the fabrication steps for transparent SN-TFTs on flexible substrates. To minimize the fabrication difficulty, devices are first patterned on thin polyimide (PI) films on silicon handling wafers.[28,29] After the fabrication, the transistors together with the polyimide films can be peeled off from the silicon wafer and transferred to any target flexible substrate. As an example, Figure 1e shows an

optical image of transparent SN-TFTs on a polyethylene terephthalate (PET) substrate. Electrical performance of the flexible transparent SN-TFTs will be discussed later in this article.

The electrical performance of fully transparent transistors on a glass substrate is studied and shown in Figure 2. Figure 2a exhibits the transfer characteristics of a typical transparent SN-TFT with a channel length of 100 μm and channel width of 100 μm including the drain current−gate voltage (I_D-V_G) characteristics in both linear and logarithm scales and transconductance−gate voltage (g_m-V_G) characteristics measured at a drain voltage of 1 V. From this plot, one can find that the on-current (I_{on}) at V_D = 1 V and V_G = −5 is 0.55 μA. Also, from the transfer curve in logarithm scale, one can derive the current on/off ratio and subthreshold slope ($S = dV_G/[d(\log_{10} I_D)]$) to be 10^3 and 1.2 V/dec, respectively. In addition, the peak transconductance of this transistor is 0.16 μS, and device mobility is extracted to be 1 $cm^2\ V^{-1}\ s^{-1}$. It is worth noting that the parallel plate model is used to estimate the gate capacitance when calculating the device mobility, which is essentially the effective device mobility for a TFT of channel length L and channel width W. The real gate capacitance would be smaller than the parallel plate model predicts if we take the electrostatic coupling between nanotubes into consideration, and therefore the real nanotube network mobility can be larger than the value listed above.[30,31] While previously many groups, including us, reported mobility by calculating the gate capacitance with electrostatic coupling between nanotubes taken into consideration,[22,32,33] we would like to point out that the effective device mobility is as important, because it provides direct comparison with film-based TFTs and correlates directly to transconductance and normalized on-current, both of which are important parameters for TFT applications. In addition, family transfer and output characteristics of this device can be found in the Supporting Information (S1).

Judging from the parameters derived above, the transparent devices with ITO contacts exhibit rather moderate performance compared with previous reported SN-TFTs with Ti/Pd source and drain contacts. This results from the work function difference between the ITO (3.9−4.4 eV)[34] electrodes and the nanotube thin films (4.7−5.1 eV),[35,36] which introduces large barriers at the source and drain contacts. As nanotubes are usually p-type doped in air, large work function metals, such as Au (5.1−5.47 eV) and Pd (5.22−5.6 eV), are preferred to achieve ohmic contacts for holes. However, continuous Au and Pd are not transparent over the visible light regime, which means SN-TFTs will lose their transparency if a thick layer of metals is deposited directly as the electrodes. Therefore, in order to improve the device performance while maintaining a reasonable transmittance, we added a thin layer (1 nm) of metal between the nanotube and ITO to lower the contact barrier. Figure 2b shows the improved device structure, where 1 nm Au or Pd was evaporated on top of the deposited nanotube film before ITO sputtering. As only a very small amount of metal was evaporated, instead of forming a continuous film, metal "islands" were deposited on the substrate, which makes the metal layer semitransparent. Optical transmittance measurement of the thin metal films shown in the Supporting Information (S2) proves this point.

The electrical performance of the transparent SN-TFTs improves significantly after the thin metal films are applied, which is shown in Figure 2c. Typical I_D-V_D plots for devices with the same channel geometry (L = 20 μm, W = 100 μm) but with different source and drain contacts under V_G = −5 V reveal that ohmic contacts were achieved for devices with Au/ITO and Pd/ITO electrodes, and the on-current for these two kinds of devices increased about 3 times compared with the one from devices with ITO-only source and drain electrodes. While the electrical performance has been improved, the transparency of the devices did not change too much. Figure 2d plots the transmittance of glass substrates with arrays of transparent SN-TFTs with Pd/ITO, Au/ITO, and ITO contacts. From this figure, one can find that the transmittance of the devices decreases only about 3% (with Au/ITO) and 5% (with Pd/ITO) compared with the ITO-only electrodes, which is acceptable considering the significant electrical performance improvement.

In addition to the on-current and optical transmittance, a more detailed analysis of the improved transparent SN-TFTs is shown in Figure 2e and f, which includes the transfer characteristics in both linear and logarithm scale and g_m-V_G characteristics of a typical device with channel dimensions of L = 100 μm and W = 100 μm. On the basis of this plot, one can find that devices with Au/ITO and Pd/ITO exhibit similar behavior in terms of on-current (1.8 μA for the device with Au/ITO contacts and 1.5 μA for the device with Pd/ITO contacts; same sequence for parameters listed below), current on/off ratio (1.07×10^3 and 1.6×10^3), subthreshold slope (0.8 and 0.85 V/dec), and peak transconductance (0.7 and 0.6 μS). Also, based on the peak transconductance, the derived device mobilities for these two kinds of device are 4.47 $cm^2\ V^{-1}\ s^{-1}$ for a transistor with Au/ITO contacts and 3.72 $cm^2\ V^{-1}\ s^{-1}$ for that with Pd/ITO contacts. Compared with the devices that have the same channel geometry but with ITO-only source−drain electrodes, all the parameters listed above show 2−3 times improvement owing to the added large work function metal contact film. In addition, although Pd has a slightly higher work function compared with Au, devices with thin layers of Au and Pd provide similar electrical performance. This may be due to the fact that the deposited Au/Pd was too thin to form a continuous film, so the contact resistances between nanotube and source/drain electrodes not only are affected by the work function of the

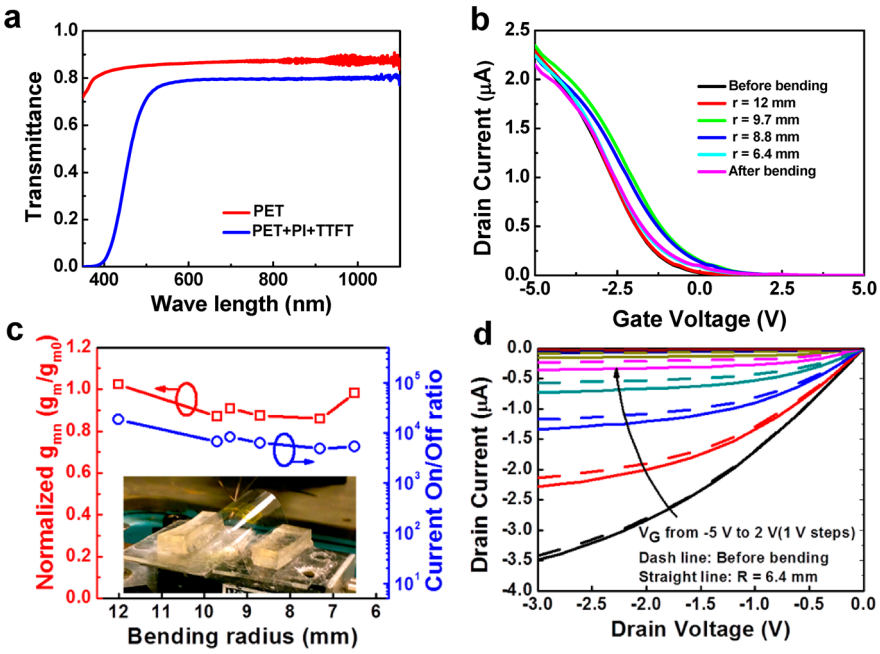

Figure 3. Fully transparent and flexible SN-TFTs. (a) Optical transmittance of a PET substrate with transparent SN-TFTs with Au/ITO contacts. (b) Transfer (I_D-V_G) characteristics of a representative device (L = 100 μm, W = 100 μm) under different bending radii in linear and logarithm scales. (c) Normalized transconductance (red) and on/off ratio (blue) extracted from the data in Figure 4b *versus* bending radius. Inset shows an optical micrograph of the experimental setup to measure I_D-V_G under different bending radii. (d) Output (I_D-V_D) characteristics of the same device under different gate voltages with bending radius of 6.4 mm. V_g was swept from −5 V (black curve) to 2 V with 1 V steps.

thin metal layers but also depend on some other factors, such as the resistance of the thin metal layers or the contact resistances between Au/Pd and the ITO layers. While devices with a Au film have higher transmittances, Au/ITO contacts could be a better choice for transparent electronic applications.

Besides transistors on glass substrates, the performance of transparent SN-TFTs on flexible substrates is also investigated. Flexible transparent SN-TFTs with Au/ITO contacts and 50 nm Al_2O_3 and 5 nm SiO_2 gate dielectrics were fabricated on thin polyimide films on silicon handling wafers and then transferred to PET substrates for flexibility measurements. Figure 3a is the optical transmittance of the transparent and flexible devices on PET. The optical transmittance is ∼80% in the 500−1100 nm wavelength range, which is similar to those fabricated on glass substrates. The sudden drop of transmittance below 500 nm is due to the existence of the PI film, which shows a light yellow color. To evaluate the flexibility of our devices, I_D-V_G measurements were performed under various bending radii (r) using the setup illustrated in the inset of Figure 3c, and the plots are shown in Figure 3b. The I_D-V_G curves correspond to a device before bending (black), under weak (r = 12 mm, red), moderate (r = 9.7 mm, green; r = 8.8 mm, blue), and strong bending (r = 6.4 mm, cyan) and after bending (magenta), respectively. From these curves, normalized transconductance g_{mn} (take the one before bending as g_{m0}) and on/off ratio of this device at each bending condition were extracted and plotted in Figure 3c. One can see that due to the excellent mechanical properties of SWNT,[37] the device continued to perform as a transistor for different bending radii, only a very small variation is observed from the on-current, transconductance, and on/off ratio, which is also proved by the output (I_D-V_D) characteristics of the same device before bending and with 6.4 mm radius bending, as exhibited in Figure 3d.

Our ability to fabricate high-performance transparent SN-TFTs on both rigid and flexible substrates enables us to further explore their application in transparent display electronics. For proof of concept purposes, an organic light-emitting diode (OLED) was connected to and controlled by a typical SN-TFT device on a glass substrate whose transfer and output characteristics are shown in Figure 4a and b, respectively. In order to control the OLED, device on-current as well as on/off ratio are crucial. Here the device channel length and channel width are both selected to be 100 μm so that the transistor can provide enough current while the on/off reaches 1.3 × 10^3 and therefore can meet the requirement for controlling the OLED to switch on and off. A standard NPD/Alq_3 OLED (2 × 2 mm^2) with multilayered configuration is employed in this study, given as ITO/4,4′-bis[*N*-(1-naphthyl)-*N*-phenylamino]-biphenyl (NPD) [40 nm]/tris(8-hydroxyquinoline)-aluminum (Alq_3) [40 nm]/LiF [1 nm]/aluminum (Al) [100 nm], whose transfer characteristics are shown in the Supporting Information S3. The schematic of the OLED control circuit is shown in the inset of Figure 4c, where the drain of the driving transistor

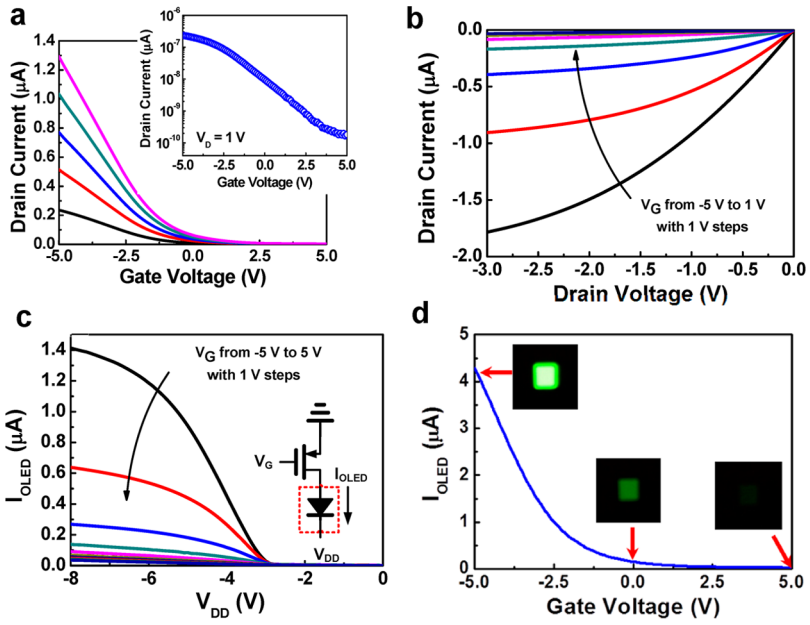

Figure 4. OLED control circuit by transparent SN-TFT. (a) Transfer (I_D-V_G) characteristics under different drain voltages (from 0.2 to 1 V with 0.2 V steps) for the device used to control the OLED (L = 100 μm, W = 100 μm), Inset: I_D-V_G plot of the same device in logarithm scale with V_D = 1 V. (b) Output (I_D-V_D) characteristics of the same device with different gate voltages. (c) $I_{OLED}-V_{DD}$ characteristics of the OLED control circuit. Various curves correspond to various values of V_G from −5 to 5 V in 1 V steps. Inset: Schematic diagram of the OLED control circuit. (d) Plot of the current through the OLED (I_{OLED}) *versus* V_G with V_{DD} = −8 V. The inset optical images show the OLED intensity at certain gate voltages.

was connected to an external OLED and a negative voltage ($-V_{DD}$) was applied to the cathode of the OLED. Current flow through the OLED (I_{OLED}) was measured by sweeping the V_{DD} while also changing the input voltage V_G as plotted in Figure 4c. The figure illustrates that the tested OLED has a threshold voltage of about 3 V, and it will be turned on when the controlling transistor is in the "ON" state and the supply voltage is higher than the OLED threshold voltage. Furthermore, the current flow through the OLED can be modified by varying the voltage applied to V_G, as directly revealed in Figure 4d, where current *versus* V_G characteristics are plotted with a fixed V_{DD} of −8 V. From this figure and the inset optical photographs taken at certain gate voltages, one can find that the light intensity of the OLED is modulated by the gate voltage, and it can be fully turned on and turned off when V_G is biased at −5 and 5 V, respectively.

CONCLUSION

In summary, we have reported significant progress on fabrication of transparent SN-TFTs for display electronics. These separated carbon nanotube based thin-film transistors exhibit excellent transparency (~85%) and good electrical performance. In addition, to further improve the device performance, a thin layer of large work function metal is applied between the carbon nanotube and ITO electrodes. While still maintaining the attractive transparency (~82%) and current on/off ratio (>10^3), devices with Au/ITO electrodes show improved performance in terms of device mobility (4.47 $cm^2V^{-1}s^{-1}$) and subthreshold slope (0.8 V/dec). Furthermore, flexible and transparent SN-TFTs have been fabricated and tested, only a very small variation of on-current, transconductance, and current on/off ratio is observed down to 6.5 mm bending radius. Finally, an OLED control circuit has been demonstrated with transparent SN-TFTs, and large range output light intensity modulation has been observed. Our results suggest that transparent SN-TFTs have great potential to serve as building blocks for future transparent electronics, and this demonstration can provide guidance to future research on SN-TFT-based transparent display electronics.

METHODS

Separated Nanotube Deposition. A glass substrate with a SiO_2 surface was immersed into diluted APTES solution (10% APTES in isopropanol alcohol (IPA)) for 10 min to form an amine-terminated monolayer. The sample was then rinsed with IPA and immersed into commercially available a 0.01 mg/mL, 98% semiconducting nanotubes nanotube solution (NanoIntegris Inc.) for 30 min. After rinsing with DI water and IPA, uniform nanotube networks were formed on top of the substrates.

Transparent, Separated Nanotube Thin-Film Transistor Fabrication on Rigid Substrates. First, glass substrates were prepared with a common ITO (100 nm) as back-gate electrode made by photolithography, ITO sputtering, and a lift-off process. After that, 40 nm Al_2O_3 high-κ dielectric and 5 nm SiO_2 were deposited on top of the ITO back gate by atomic layer deposition and e-beam

evaporation, respectively. Separated carbon nanotubes were then deposited on the bilayer dielectric using the method discussed above. Following the CNT deposition, photolithography was used to open gate channels and define openings for source and drain electrodes. For some of the devices, 1 nm Au or Pd was evaporated using an e-beam evaporator. ITO was then deposited on all the devices by sputtering as source and drain electrodes. Finally, since the separated nanotube thin film covers the entire wafer, in order to achieve accurate channel length and width and to prevent possible leakage in the devices, one more step of photolithography plus O_2 plasma is used to remove the unwanted nanotubes outside the device channel region.

Transparent, Separated Nanotube Thin-Film Transistor Fabrication on Flexible Substrates. First, an approximately 10 μm thick polyimide layer (PI-2525, HD MicroSystems) is spin-coated on a Si/SiO_2 wafer. After that, transparent devices were fabricated following the same method as described above. To minimize any possible leakage current during bending, 50 nm Al_2O_3 and 5 nm SiO_2 were applied by ALD and an e-beam evaporator as the gate dielectric, respectively. Finally, the fabricated transistors were pealed off from the handling wafer together with PI and were transferred onto a PET substrate for flexibility measurement.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: This material is available free of charge *via* the Internet at http://pubs.acs.org.

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