CHAPTER I

Carbon Nanotubes: Synthesis, Devices, and Integrated Systems

Xiaolei Liu, Chenglung Lee, Song Han, Chao Li, and Chongwu Zhou

Department of Electrical Engineering, University of Southern California, Los Angeles, California, USA

CONTENTS

1. INTRODUCTION

Carbon nanotubes rank among the most exciting new developments in modern science and engineering. Since carbon nanotubes [1, 2] were first discovered by Iijima [3], the past 10 years witnessed significant progress in both carbon nanotube synthesis and investigations on their electrical, mechanical, and chemical properties. This has been largely driven by the exciting science involved and numerous proposed applications of carbon nanotubes due to their unique electronic properties and nanometer sizes. Single-walled carbon nanotubes are ideally suited for studies on low-dimensional physics including electron-electron interactions, electron-lattice interactions, electron localizaton, and band structures. Nanotubes have great potential to be used as nanoscale electronic devices such as field effect transistors [4–6], single-electron transistors [7, 8], and nanoscale *p-n* junctions [9]. In addition, carbon nanotubes are becoming promising candidates in many important applications such as atomic force microscope tips [10–12], field emitters [13, 14], and chemical sensors [15].

Carbon nanotubes can be viewed as sheets of graphite rolled into seamless cylinders with nanometer scale diameters and micron scale lengths [1], as shown in Figure 1. The vector $\boldsymbol{AA'}$ can completely define the rolling of a single-walled carbon nanotube (SWNT). We can express $\boldsymbol{AA'}$ as a linear combination of lattice vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$ as $\boldsymbol{AA'} = m\boldsymbol{a}_1 + n\boldsymbol{a}_2$. Thus, the notation (m, n) defines the diameter and the chirality of a SWNT. "Zigzag"

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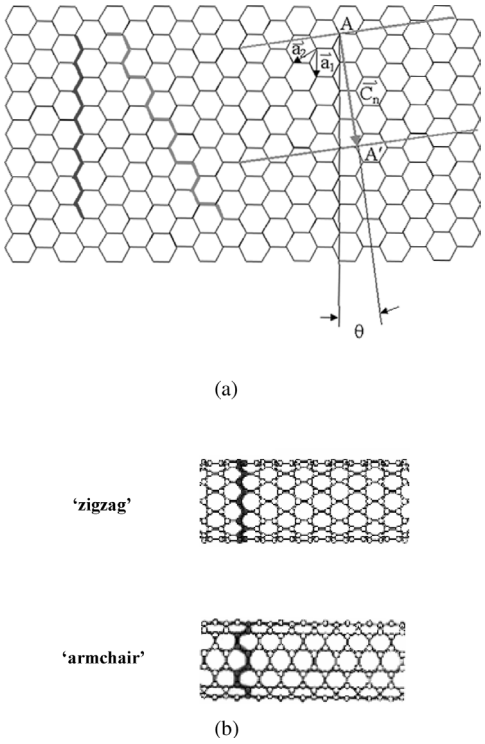

Figure 1. Virtually roll up a graphite layer to form a single-walled carbon nanotube. (a) The graphite layer can be rolled up along the near-vertical axles. Then, the vector $\boldsymbol{AA}'$ can totally define the rolling of a SWNT. We can express $\boldsymbol{AA}'$ as a linear combination of lattice vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$ as $\boldsymbol{AA}' = m\boldsymbol{a}_1 + n\boldsymbol{a}_2$. Thus, the notation (m, n) defines the diameter and the chirality of a SWNT. (b) "Zigzag" and "armchair" are the two typical carbon nanotubes. For a zigzag, $m = 0$ or $n = 0$, while for an armchair, $m = n$.

and "armchair" are two typical types of carbon nanotubes. For a zigzag nanotube, $m = 0$ or $n = 0$, while for an armchair, $m = n$. Such one-dimensional systems exhibit fascinating electronic and mechanical properties. Depending on their chiralities, nanotubes can be metallic, semimetallic, or semiconducting [1]. Nanotubes also possess remarkably high Young's modulus and tensile strength [1]. Such unique electronic and mechanical properties have captured the attention of researchers worldwide, and extensive effort has been taken to understand these properties and explore their potential applications. In recent years, progress in addressing these issues has generated significant excitement in the area of nanoscale science and technology.

This chapter summarizes the progress made in recent years in carbon nanotube synthesis and electronic studies. We will focus on a chemical vapor deposition (CVD) method utilized to grow individual single-walled carbon nanotubes at desired sites and investigations of the electronic properties of various carbon nanotubes. Part of the reviewed work (CVD synthesis, field effect transistors, and *p-n* junctions) was carried out by one of the authors (C. Zhou) and his co-workers in Prof. H. Dai's group while at Stanford. The complementary-nanotube-inverter work was carried out by Prof. Zhou's group at the University of Southern California (USC).

2. SYNTHESIS OF CARBON NANOTUBES

Iijima first discovered the multiwall carbon nanotubes in 1991, when he worked on C_{60} and observed carbon soot on the negative graphite electrode produced in arc discharge [3], shown in Figure 2. This method involves the condensation of carbon atoms and radicals from evaporation of solid carbon sources in arc discharge, and the temperature involved can be as high as 3000–4000 °C. In 1992, Ebbesen and Ajayan achieved growth and purification of multiwalled carbon nanotubes at the gram level using the arc-discharge method [16]. These nanotubes typically have diameters around 5–30 nm and lengths around 10 μm. In 1993, Iijima's group [17], as well as Bethune and his colleagues [18] found that the use of transition-metal catalysts in the arc-discharge process leads to nanotubes with only a single shell. However, the yield of carbon nanotubes was low, and there were large amounts of metal carbide clusters and amorphous carbon attached to the nanotubes. This was a significant disadvantage of the arc-discharge method for further investigations on nanotubes, until 1997, when Journet and his co-workers found that the mixture 1 at.% Y and 4.2 at.% Ni as catalysts in graphite powder gave a high yield of 70–90% in their setup [19].

Another milestone in the synthesis of single-walled carbon nanotubes is the effort made by Smalley's group in 1996 [20]. He and his co-workers at Rice University developed a laser ablation technique that could grow single-walled carbon nanotubes with a relatively high yield of more than 70%, which paved the way for the

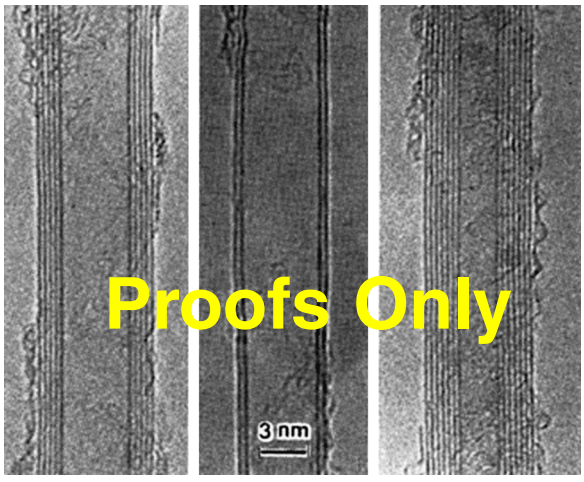

Figure 2. The transmission electron microscope (TEM) image of first discovered carbon nanotubes by Iijima: the multiwalled carbon nanotubes he found in the soot of an arc-discharge setup. Reprinted with permission from [3], S. Iijima, *Nature* 354, 56 (1991). © 1991, Macmillan Publishers Ltd.

take-off of investigations on the physical properties of SWNTs. They used the laser ablation on graphite rods doped with a mixture of cobalt and nickel powder in the inertial gas environment followed by heat treatment in vacuum to sublime out C_{60} and other small fullerenes. The nanotubes they got had highly uniform diameters and bundled together as "ropes" by van der Waals interaction. Figure 3 shows the experiment setup and the bundled ropes synthesized by laser ablation [20]. A purification process involving refluxing the as-grown nanotubes in a nitric acid for an extended period of time was also developed by Smalley and his co-workers [21]. This method has been widely applied to remove amorphous carbon and residual catalytic metal particles commonly found mixed with nanotubes in the final product.

In spite of the success of the arc-discharge and laser ablation methods in producing carbon nanotubes with a high yield, the final products are usually bundled nanotubes decorated with catalyst particles and amorphous carbon. Previous studies using such products have been severely hampered by the lack of control over the nanotube growth and the difficulty in wiring up individual nanotube devices, making practical applications almost impossible. It would be desirable to have a high-yield synthesis route to produce SWNTs with controlled length, positions, and orientations for both scientific and technological studies. It is equally desirable to develop a method to make robust, low-resistance electrical contacts between nanotubes and metallic electrodes. These goals pose great challenges to nanotube synthesis, processing, and assembly strategies. Significant progress in addressing these challenges has been made by Dai and his co-workers: a novel CVD method was developed to grow high-quality individual single-walled carbon nanotubes off patterned catalyst islands directly on substrates [22–25]. This technique readily yields large numbers of SWNTs at specific locations, and opens up new possibilities for integrated nanotube systems. Figure 4 shows a typical CVD setup, which involves flowing a hydrocarbon gas through a furnace tube, which hosts substrates decorated with catalyst particles. Hydrocarbon works as the feedstock, and catalyst particles, usually made of Fe, Ni, or Co, work as the seed for nanotube growth. Details of the controlled growth of SWNTs are shown in Figure 5. First, standard e-beam lithography is employed to pattern the Si/SiO_2 substrate, followed by the deposition of the catalyst material to form an

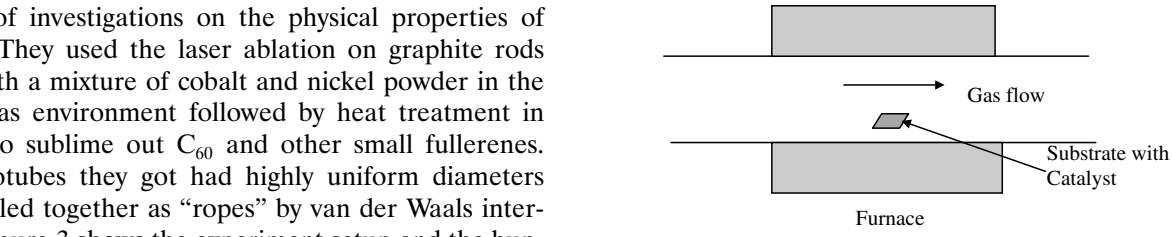

Figure 4. Schematic of a typical experimental setup for growing carbon nanotubes. In the setup a mixture of gases containing carbon stock flows through the tube which is set inside a furnace with a high temperature.

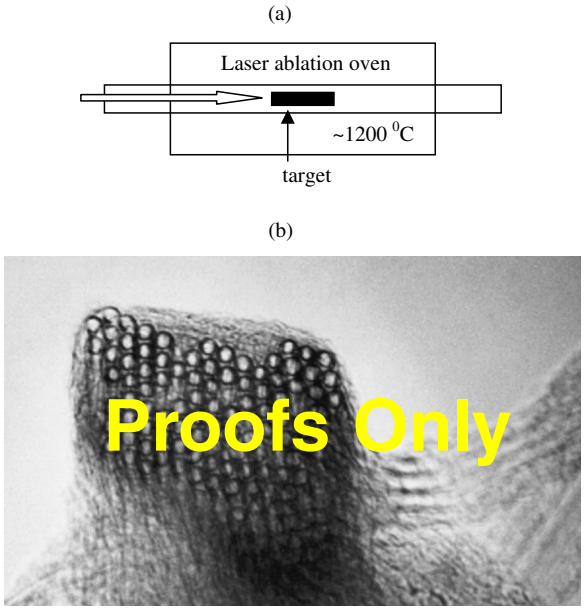

Figure 3. (a) The experimental setup of laser ablation method to synthesize the SWNT. The laser beam is focused on the carbon rod doped with catalysts when flowing inertial gas. The soot as the product is collected at the copper collector. (b) TEM image of the bundled SWNTs as "rope." Reprinted with permission from [20], A. Thess et al., *Science* 273, 483 (1996). © 1996, American Association for the Advancement of Sciences.

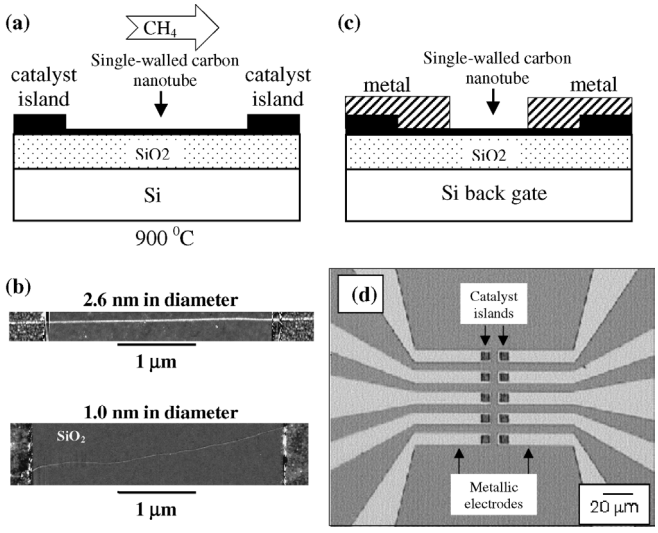

Figure 5. Schematic diagram of the CVD growth and fabrication of nanotube devices. (a) CH_4 flows through a tube furnace heated to 900 °C. SWNTs are grown bridging adjacent catalyst islands on substrates. (b) AFM images of two as-grown carbon nanotubes. (c) Schematic diagram of a nanotube device after e-beam patterning and metal evaporation to form the source and drain electrodes. The silicon substrate is used as the gate electrode. (d) Photograph of a nanotube chip showing five nanotube devices where black squares are patterned catalyst islands.

array of catalyst islands on the substrate, displayed as pairs of black squares in Figure 5d. The catalyst material consists of alumina nanoparticles coated with iron and molybdenum. CVD synthesis is carried out for 10 minutes at 900 °C in a quartz tube furnace with methane as the feeding gas. Under these conditions, nanotubes grown from the catalyst islands are predominantly individual SWNTs with negligible structural defects. The synthesized nanotubes grow from the catalyst islands and are often found to bridge adjacent catalyst islands, as manifested in Figure 5b. The diameter of these nanotubes falls in the range 0.7–5 nm with most tubes at 1.5 nm, and the length is usually found to be several microns.

After the CVD synthesis of a single-walled carbon nanotube chip, e-beam lithography and metallization are employed to define electrodes to contact both ends of the carbon nanotubes, shown in Figure 5c. These electrodes, typically consisting of 20 nm Ti followed by 60 nm Au, cover both the catalyst islands and part of the carbon nanotubes, and serve as the source and drain electrodes. Figure 5d depicts a photograph of an as-made nanotube chip, where five pairs of catalyst islands and Ti/Au electrodes are clearly visible. This CVD/fabrication method produces mechanically strong and stable metal/nanotube contacts and renders abundant nanotube devices for further studies.

Significant progress has also been made by several other groups toward CVD growth of high-quality SWNTs. Liu and his co-workers have developed a way to produce Fe/Mo catalyst supported on alumina aerogel [26]. This catalyst possesses a high surface area and large mesopore volume, and has led to a nanotube-catalyst ratio as high as 2 : 1 in the CVD product using methane as the feedstock. Smalley and his co-workers have developed a gas-phase CVD process to grow bulk quantities of single-walled carbon nanotubes [27], where carbon monoxide is used as the feedstock and catalytic nanoparticles are generated *in situ* by thermal decomposition of an iron-containing compound. Bulk production of SWNTs has also been successfully achieved by other groups using CVD techniques [28, 29].

In addition to the CVD synthesis of SWNTs, by using different hydrocarbon gases, catalysts, flowing conditions, and temperatures, multiwall carbon nanotubes (MWNTs) can also be synthesized. In contrast to the arc-discharge or laser ablation techniques, CVD growth of MWNTs can give us aligned and ordered nanotube structures. The typical methods of growing aligned multiwalled nanotube structures have been developed by several groups independently. For example, Xie and his co-workers used iron oxide particles created in the porous silica as the catalyst and 9% acetylene in nitrogen as the carbon feedstock [30, 31], while Ren and his co-workers developed a method to grow oriented MWNTs on glass substrates by a plasma-assisted CVD method with nickel as the catalyst and acetylene as the carbon source [32]. Figure 6a shows a typical setup developed by the Dai group to grow towers of multiwalled carbon nanotubes [33], where iron nanoparticles are used as the catalyst and acetylene is used as the feedstock. Towers of aligned multiwalled nanotubes can be grown following the shape of a micromotor by employing photolithography to pattern the iron catalyst layer [34], shown in Figure 6b.

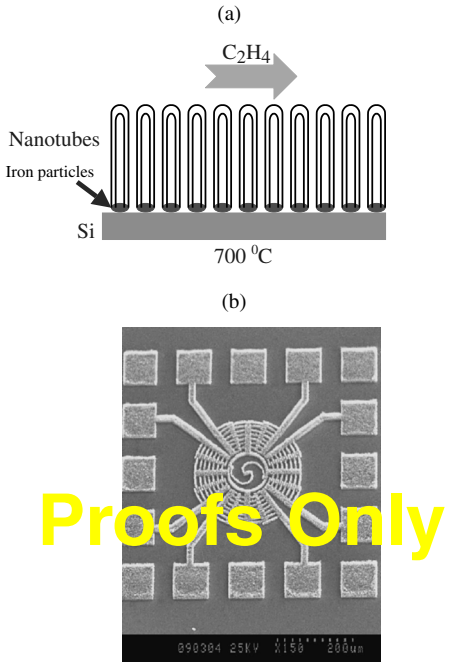

Figure 6. (a) Schematic diagram of a CVD process for multiwalled carbon nanotubes. Iron nanoparticles are used as the catalyst and C_2H_2 is used as the feedstock. (b) SEM top-view of multiwalled nanotube towers grown on a silicon substrate. The micromotor pattern is achieved by photolithographic patterning of the catalyst.

In addition to the well-developed CVD method, several novel synthesis techniques have been demonstrated. In 1998, Tang et al. found that pyrolysis of tripropylamine can form mono-sized SWNTs [35]. The diameter of the SWNT grown this way can be as small as 4 Å, close to the theoretical limit. They have also successfully observed superconductivity with their SWNT samples with a transition temperature of 15 K [36]. Schlittler and his co-workers developed a technique to control the chirality of the SWNT [37]. They deposited Ni and C_{60} layers alternately in a sandwich manner on a Mo substrate, and then heated the sample to high temperature in vacuum while applying a magnetic field oriented parallel to the surface normal. Their procedure produces carbon nanotubes with identical chiralities.

3. ELECTRONIC PROPERTIES OF CARBON NANOTUBES

Research on the electronic transport through single-walled carbon nanotubes witnessed phenomenal progress in the past few years. This has been largely driven by

the fascinating science and numerous potential applications associated with carbon nanotubes. SWNTs are usually atomically uniform and well-defined, making them ideal systems as one-dimensional conductors. However, unlike nanowires based on conventional semiconductors, carbon nanotubes display rich electronic properties, the most important of which is that a carbon nanotube can be metallic, semimetallic, or semiconducting, depending on its chirality and diameter [1, 38–42]. Band structure calculations have predicted that armchair SWNTs with (n, n) indices are truly metallic with finite density of states at the Fermi level, whereas SWNTs with (m, n) indices are semiconducting when $m - n \neq 3 \times integer$, and have primary energy gaps $E_g \propto 1/d$, where d is the nanotube diameter. SWNTs with (m, n) indices and $m - n = 3 \times integer$ are semimetallic with zero bandgap within tight-binding calculations based on p_π-orbitals alone. For this type of SWNT, Hamada et al. [39] and White et al. [40] have pointed out that the curvature of nanotubes leads to nonparallel p_π-orbitals interacting with σ-orbitals, which causes the opening of a small bandgap to result in a semiconductor from a semimetal. Louie and co-workers have carried out first-principles *ab initio* calculations and found that the curvatures of small-diameter SWNTs can lead to rehybridization of π^*- and σ^*-orbitals and thus altered electronic structures of SWNTs from those of flat graphene stripes [41]. Kane and Mele categorized SWNTs into three types, truly metallic arm-chair SWNTs, semiconducting SWNTs (S-SWNTs), and curvature-induced small-gap semiconducting SWNTs (SGS-SWNTs) [42]. For SGS-SWNTs, the bandgaps depend on specific (m, n) indices and are in the range of 2–50 meV for d = 3–0.7 nm. For SGS-SWNTs with the same m/n ratio, the gap should scale as $1/d^2$ [42]. The diameter-dependent bandgap is shown in Figure 7 for all three categories [42]. The following sections will review electronic transport studies on metallic, semimetallic, and also semiconducting nanotubes, with our focus on results obtained from nanotube devices fabricated via the CVD growth method.

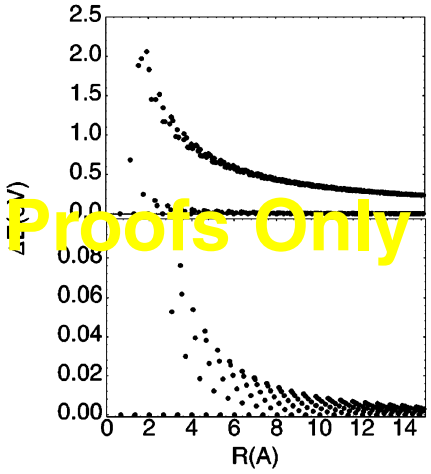

Figure 7. Bandgaps calculated for carbon nanotubes of various diameters. The tubes fall into three families: semiconducting nanotubes with primary gaps which scale as $1/R$ (top panel, top curve), semimetallic nanotubes with zero primary gap but nonzero curvature-induced gaps which scale as $1/R^2$ (top panel, lower curve, and shown in the expanded scale in the lower panel), and armchair tubes with zero primary gap and zero curvature-induced gap. Reprinted with permission from [42], C. L. Kane and E. J. Mele, *Phys. Rev. Lett.* 78, 1932 (1997). © 1997, American Physical Society.

3.1. Fabrication and Overview of Nanotube Devices

Making electrical contacts to individual carbon nanotubes lies at the heart of nanotube device fabrication. A popular spin-on method was developed by McEuen and his co-workers [8], and Dekker and his co-workers [7]. A small amount of carbon nanotube material, usually produced by laser ablation or arc discharge, is first dispersed into an organic solvent to form a suspension, and then spun onto a Si/SiO_2 substrate with predefined metal electrodes. Alternatively, atomic force microscopy (AFM) is used to locate the nanotubes first and e-beam lithography is then carried out to define electrical contacts to the carbon nanotubes. This method is simple and easy to use; however, it has no control over the nanotube location and orientation and the yield for good devices is usually low.

In contrast, the controlled CVD method can directly grow individual carbon nanotubes at desired sites on Si/SiO_2 substrates [22–25], as described in Section 2, and therefore is superior in producing nanotube devices and integrated systems. AFM is usually employed to ensure each device consists of a single nanotube bridging the metal electrodes. The length of the nanotubes between the electrodes is controlled by the e-beam lithography step and can vary from 0.5 μm to 5 μm. The electronic measurements are usually performed in the temperature range from 300 K down to 1.5 K and the heavily doped silicon substrate is used to supply the gate bias. Most of the carbon nanotube devices fall into three categories according to their resistance and gate dependence. The first category corresponds to nanotube devices with low resistance and weak or no gate dependence, generally regarded as the signature of metallic carbon nanotubes. The second category corresponds to devices with relatively low resistance; however, change in the gate bias can bring such devices from a conductive state to an almost insulating state, and then back to a conductive state. Such devices will be described in detail in Section 3.3 and are attributed to small-gap semiconducting (or semimetallic) carbon nanotubes. The third category corresponds to devices with high resistance and strong gate dependence, corresponding to semiconducting nanotubes.

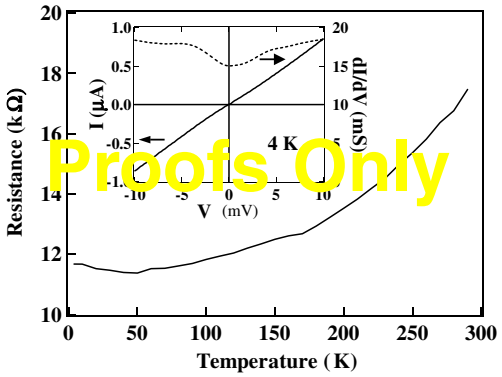

Figure 8. Temperature-dependent resistance of a metallic SWNT. Inset: I-V and dI/dV–V curves recorded at 4 K.

3.2. Electronic Properties of Metallic Carbon Nanotubes

For metallic nanotubes, the two-terminal resistance is usually dominated by the metal/nanotube contacts, even though metallic nanotubes should exhibit an ideal intrinsic resistance of only $h/4e^2$, as a result of the existence of two propagating sub-bands crossing at the Fermi level. With the controlled CVD method, many SWNT devices are found to exhibit two-terminal resistance less than 100 kΩ. Figure 8 shows the results obtained with a SWNT ($d \sim 2.2$ nm, length ~ 3 μm) that exhibited metallic characteristics. The resistance of this device displays both weak gate dependence and temperature dependence, generally regarded by previous studies as the signature of metallic carbon nanotubes. The resistance of this tube decreased from ~17.5 kΩ at 290 K to ~11.5 kΩ at 50 K. Below 50 K, the resistance curve made a slight upturn, but remained below 12 kΩ. At 4 K, the dI/dV versus V curve exhibited a slight conductance suppression near $V = 0$ (Fig. 8, inset). Importantly, for various V_g in the range of −100 to 100 V, no well-defined region with diminished conductance was observed, suggesting that the SWNT was metallic with no detectable bandgap. The zero-bias conductance suppression in this case could be due to electron-electron interaction effects. Note that the lowest resistance measured with this 3-μm-long tube was ~11.5 kΩ.

In contrast, for devices fabricated with the spin-on method in early transport measurements, the two-terminal resistance is typically in the range of 1 MΩ. The high resistance can be a result of extrinsic causes such as granularity of the evaporated metal, as well as intrinsic causes such as the electron coupling between the metal atoms and the nanotubes [43–45]. Reduction in the contact resistance has been achieved by using different metals and changing the annealing conditions [46, 47]. For those metallic nanotube devices with high contact resistance, Coulomb blockade, that is, single-charge tunneling effect, has been consistently observed. Single-electron transistors (SET) [7, 8] are very promising as a potential substitute to conventional silicon-based transistors for future integrated circuits; however, most SET structures are built upon ultrasmall metallic or semiconductive particles that are hard to fabricate and control, and can function only at low temperatures. Among all the candidates for single-electron transistors, carbon nanotubes have their unique advantages: nearly perfect crystalline and well-defined dimensions.

The first SET made of carbon nanotubes were realized by Tans et al. [7] and Bockrath et al. [8], followed by more in-depth studies [48–51]. Their three-terminal transistor structures are formed by the spin-on method and the silicon substrate is used as the gate electrode. Coulomb blockade transport characteristics are clearly observed on their devices at temperatures lower than 10 K, as shown in the "Coulomb diamond" in Figure 9a. When one or

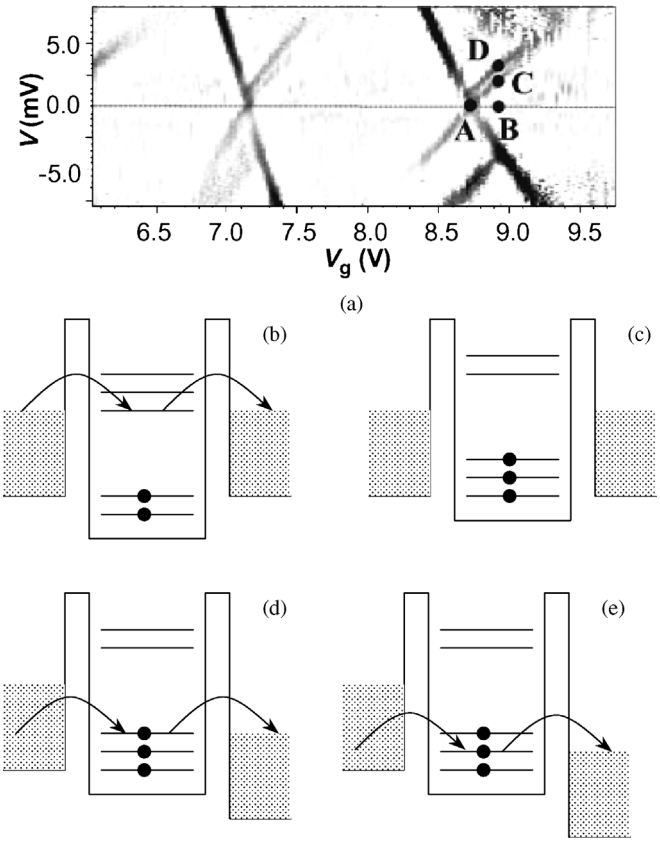

Figure 9. SET on carbon nanotube rope. (a) Differential conductance dI/dV, which is plotted invertly with dark corresponding to large value, as a function V and V_g. (b)–(e) are the schematics corresponding to the measurement points A–D in part (a). In (b), corresponding to A, when the bias is 0 and an energy level is on the Fermi level, the conductance is high because of resonant tunneling. In (c), corresponding to B, no energy level is on Fermi level, thus it is within the blockade regime. In (d), corresponding to C, and (e), corresponding to D, the bias voltage is applied, transport occurs through the first and the second occupied states, respectively. Reprinted with permission from [8], M. Bockrath et al., *Science* 275, 1922 (1997). © 1997, American Association for the Advancement of Sciences.

more energy levels reside within the chemical potential window between the left and right electrodes (points A, C, and D in Fig. 9a), the differential conductance is high since electrons can resonantly tunnel through the nanotube. However, if there is no energy level within the range between the chemical potentials of the electrodes, the transport will be blocked, corresponding to point B in Figure 9a.

Despite the excitement generated by the above-mentioned work, the operation temperatures of such nanotube single-electron transistors were still very low. In addition, a nanotube rope was used instead of an individual single-walled nanotube. Recently Dekker's group demonstrated a new method to make SET based on individual metallic SWNTs at room temperature [52]. Their method involves creating a single-electron island by forming two buckles in series on a carbon nanotube via AFM manipulation. The isolated segment of the nanotube, approximately 25 nm long, serves as the island and those two buckles serve as the energy barriers for electron transport [53]. With such devices Coulomb blockade is convincingly demonstrated at room temperature.

Chemical doping is another way to form quantum dots along a SWNT. Kong et al. fabricated quantum dots on a SWNT by doping a semiconductive SWNT with potassium [54]. Because of the nonhomogeneous distribution of potassium atoms along the SWNT, the conductance band bends below the Fermi level for certain part of the nanotube, thus forming a quantum dot. Coulomb blockade and Coulomb diamond were observed with such devices up to 80 K, pointing to a segment of the nanotube of $0.1 \sim 0.15$ μm in length working as the single-electron island.

In addition to the single-electron tunneling effects, intriguing phenomena, such as the proximity effect [55, 56], have also been observed with metallic carbon nanotubes. Carbon nanotubes are interesting candidates for studying the proximity effect because of their long phase coherence lengths and also their one-dimensional nature. A key to observe the proximity effect in a metallic nanotube contacted by two superconductive leads is to obtain low contact resistance and hence high superconductor-nanotube interface transparency. This has been achieved by Kazumov et al., who observed Josephson supercurrents in metallic nanotubes suspended between two superconductive electrodes (gold/rhenium and gold/tantalum) [55]. Gate controlled proximity effect has been observed by Morpurgo et al., who used Nb to contact CVD-grown individual metallic carbon nanotubes [56]. Metallic nanotubes are also ideal systems for the study of many other important physical phenomena, including Luttinger liquid behavior [57–59], which results from the strong electron-electron interaction in one-dimensional metals, and phase coherence studies [60–62].

3.3. Electronic Properties of Small-gap Semiconducting Carbon Nanotubes

As described in Section 3.1, for SWNTs with (m, n) indices and $m - n = 3 \times integer$, the bandgaps depend on specific (m, n) indices and are in the range of 2–50 meV for $d = 3$–0.7 nm. These nanotubes are usually called small-gap semiconducting or semimetallic nanotubes. The small bandgaps are expected to have nontrivial consequences to the electrical properties of SWNTs. Electron transport [4–8, 13] and scanning tunneling experiments [63, 64] have identified individual metallic and semiconducting SWNTs. Electronic measurements performed at the early stage with individual nanotubes did not obtain evidence for the existence of small-gap semiconducting SWNTs. In transport studies, large metal-SWNT contact resistance has led to Coulomb charging effects [7, 8] that obscure the intrinsic electrical properties of SWNTs. In 2000, Zhou and his co-workers reported the observation of individual semiconducting SWNTs with bandgaps on the order of 10 meV. Low metal-tube contact resistance enables the elucidation of the intrinsic electrical properties of the SGS-SWNTs.

Two-terminal individual-SWNT devices were obtained by the above-mentioned CVD method. We used 20-nm-thick titanium (with 60-nm-thick gold on top) as metal contacts. The lengths of the SWNTs between electrodes were typically ≥ 3 μm. A degenerately doped silicon wafer with 500-nm-thick thermally grown oxide on the surface was used as the substrate. The underlying conducting silicon wafer was used as a back-gate. Figure 10 shows a tapping mode atomic force microscopy (AFM) image of an individual SWNT exhibiting small-gap semiconducting characteristics. The diameter of the SWNT

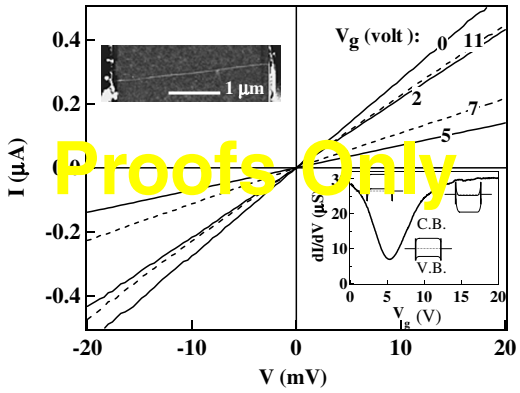

Figure 10. Room temperature I–V characteristics of an SGS-SWNT. Top inset: AFM image of the $d \approx 1.3$ nm SWNT. Bottom inset: dI/dV vs. V_g with diagrams showing the alignment between the Fermi levels of metal electrodes and the conduction band (CB) and valence band (VB) of the nanotube. Increasing the gate bias moves the nanotube bands downward, resulting in a transition from conduction through valence band at low gate bias to conduction through conduction band at high gate bias. The black vertical bars represent the contacts between the metal electrodes and the nanotube.

was ~1.3 nm, determined by AFM topographic measurements. The current-voltage I-V curves obtained at room temperature are shown in Figure 10. The linear I-V curve under zero gate-voltage (V_g) showed a resistance of 36 kΩ. Increasing V_g reduced the conductance of the sample and reached a minimum at $V_g \sim 5$ V. Further increase in V_g led to conductance recovery, as seen in the conductance versus gate-voltage curve (Fig. 10, inset) recorded under $V = 1$ mV. The conductance of the sample was suppressed by ~4 times at $V_g \sim 5$ V before the recovery, resulting in a valley in the conductance versus gate-voltage curve.

We have recorded 400 I-V curves at 2 K in the bias range of $V = -40$ to 40 mV with $\Delta V = 400$ μV, under gate voltages in the range of $V_g = 0$ to 20 V with $\Delta V_g =$ 50 mV. Figure 11a shows a gray-scale two-dimensional conductance map obtained by plotting the conductance values at various (V, V_g) points. In the central region of the map within $V = -8$ mV to 8 mV and $V_g = 7.5$ to 10 V, the sample conductance is highly suppressed and the resistance is ~5 MΩ. However, the system is highly conducting in the corner regions where $|V| > 10$–20 mV and $V_g \sim 0$ or 20 V. The resistance in the corner regions is ~20 kΩ, more than two orders of magnitude lower than that in the central region. Figure 11b shows that as V_g increases from 0 to 8 V, the conductance versus bias voltage ($dI/dV - V$) curves shift downwards, but shift upwards upon further increase in V_g. The I-V curves are nonlinear near zero bias where dips of reduced conductance are observed. Under $V_g = V_g^* \sim 8$ V, the conductance is highly suppressed for small biases $|V| < 8$ mV, as seen in the bottom curve in Figure 11b. The suppression is nearly exponential in V, indicating a gap-like structure in I-V. For gate voltages far away from V_g^*, only slight dips are seen in the dI/dV curves near $V = 0$ and the high bias conductance is $\sim 5 \times 10^{-5}$ S. We have also measured the zero-bias conductance dI/dV versus V_g using a lock-in technique, as shown in Figure 11c. A gap-like region with highly suppressed conductance is observed between $V_g \sim 9$ to 12 V in the $dI/dV - V_g$ curve. Outside the gap, the sample exhibits high conductance and some fluctuations.

The results presented above illustrate the small-gap semiconducting nature of the SWNT. Several band diagrams are included in the bottom inset of Figure 10 and Figure 11b to illustrate the relative alignment between Fermi levels of the metal electrodes and the conduction band and valence band of the nanotube under various gate biases and source-drain biases. Under V_g^* (V_g^* corresponds to the gate-voltage under which the Fermi level of the nanotube is in the middle of the bandgap), the Fermi level of the nanotube is in the middle of the bandgap. The physics of the system is similar to that of back-to-back Schottky diodes. Barriers exist to electrical transport at the metal-tube junctions, which leads to low conductance of the system. For $V_g \ll V_g^*$, the Fermi

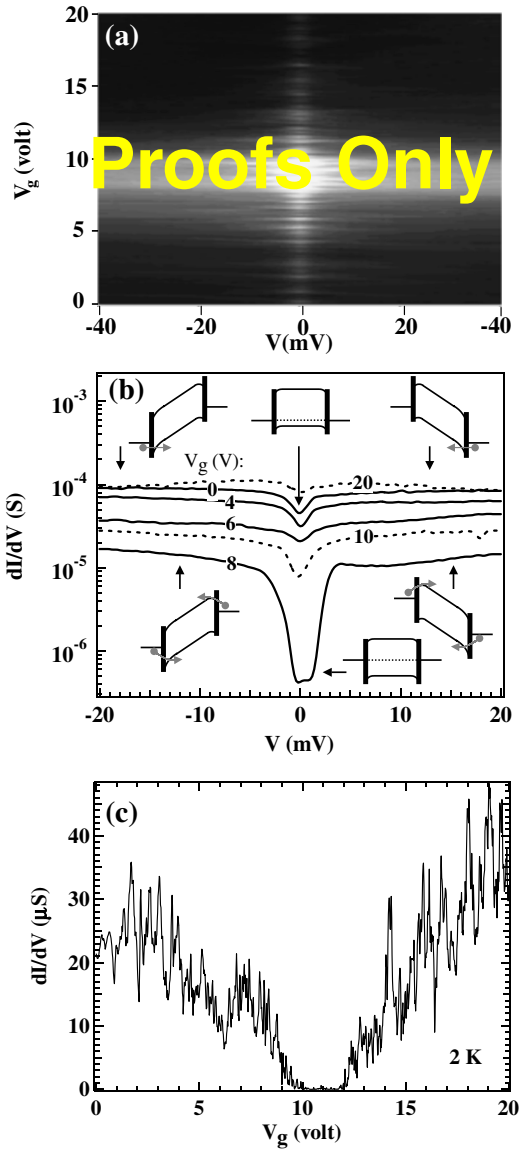

Figure 11. (a) Gray-scale 2D conductance plot $\log(dI/dV)$ vs. (V, V_g) recorded at 2 K. The brightest color corresponds to the lowest conductance $\sim 1 \times 10^{-7}$ S. The darkest color corresponds to the highest conductance $\sim 4 \times 10^{-5}$ S. (b) dI/dV vs. V curves recorded at various V_g. Top three insets illustrate the band diagrams under negative bias, zero bias, and positive bias, respectively, with $V_g = 0$ V. Bottom three insets illustrate corresponding band diagrams with $V_g = V_g^* = 8$ V. (c) Zero-bias dI/dV vs. V_g recorded at V_g^*.

level is inside the nanotube valence band and the system exhibits significant conductance since transport through the valence band can occur (p-type). For $V_g \gg V_g^*$, the Fermi level is shifted into the conduction band, through which electron transport occurs (n-type). This leads to a valley in the conduction versus gate bias curve, which is clearly observed at both room temperature (Fig. 10, bottom inset) and 2 K (Fig. 11c). At any given gate bias, a nonzero (positive or negative) source-drain bias tilts the bands of the carbon nanotube, resulting in a suppression

of the barrier height compared to the zero source-drain bias case. This leads to the observed dips in dI/dV versus V centered at zero bias for all gated biases, as shown in Figure 11b. As the gate bias increases from 0 V to V_g^* ($\sim$8 V), the nanotube energy bands shift downward relative to the Fermi levels of metal electrodes, leading to increasing barrier height for electrons or holes to go through. This is manifested in Figure 11b by the widened and deepened dip in the curve of dI/dV versus V with $V_g = 8$ V, as compared to the dip in the curve with $V_g = 8$ V. As gate bias increases further, the conductance recovers and the dip shrinks due to the turn-on of n-type conduction. The bandgap can be estimated from the conductance versus gate-voltage data shown in Figure 11c, where the gap region exhibiting highly suppressed conductance spans $\Delta V_g \sim 3$ V. Using a gate efficiency factor $\alpha \sim 2.5$ mV/V, the bandgap is estimated to be $\sim$7.5 meV.

The low-temperature data shown in Figure 11 exhibit no clear signatures of Coulomb blockade. Thus, Coulomb charging effects are not dominant over the observed small-gap semiconducting characteristics. However, we do observe significant conductance fluctuations upon gate-voltage variations, especially under low bias voltages ($|V| < 10$ mV), as streaking lines are seen near the central region in Figure 11a. These fluctuations could be due to electron interaction effects, but their precise origins are not understood at the present time. At 2 K, the resistance of the SWNT sample away from the central suppressed region in Figure 11a is $\sim$20 kΩ, which is close to the resistance quantum h/2e^2. The low resistance points to excellent metal-tube coupling, which is consistent with the fact that Coulomb charging is not the dominant phenomenon observed with the sample.

We have also elucidated the temperature-dependent electrical properties of the small-gap semiconducting SWNT. The linear conductance versus gate-voltage curves measured at 290 K, 60 K, and 10 K under V = 1 mV are shown in Figure 12a. It is observed that V_g^* drifts as the temperature is decreased. The drifts can be interpreted as due to changes in the electrostatic charge-state of the substrate, as the temperature is lowered. To correct for this unwanted effect, we determine the temperature-dependent resistance of the SWNT sample under conditions with fixed Fermi level position relative to the bands at all temperatures. At $V_g^*(T)$, the valley resistance is found to scale as $\exp(-E_a/K_{\rm B}T)$ with $E_a \sim 6$ meV, as shown in Figure 12b. This suggests that when the Fermi level resides inside the bandgap, transport through the SWNT under small bias voltages is thermally activated across a barrier $\sim E_g/2$. The small-gap semiconducting nature of the SWNT is thus fully manifested. On the other hand, under $V_g = V_g^*(T) - 5$ V, the resistance of the SWNT exhibits drastically different dependence on temperature, as shown in the inset of Figure 12b. The resistance *decreases* from $\sim$36 kΩ to 25 kΩ as temperature

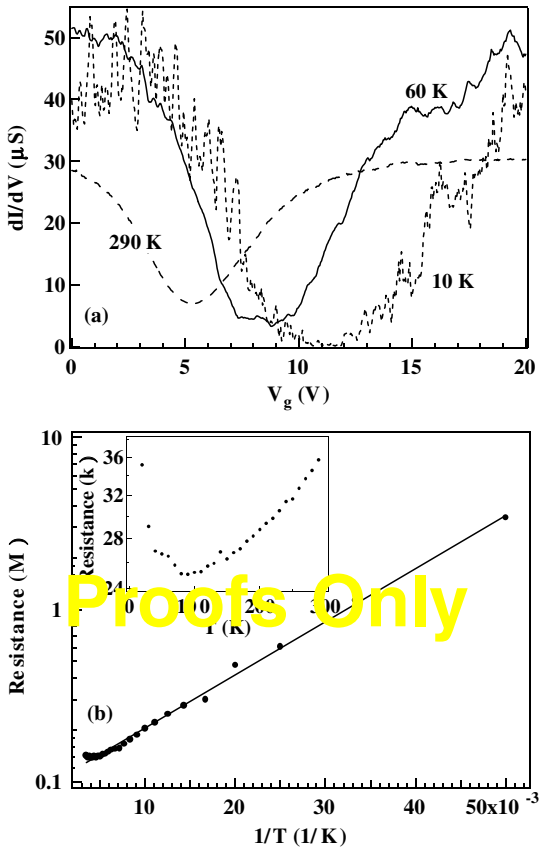

Figure 12. (a) dI/dV vs. V_g curves recorded at 290, 60, and 10 K, respectively. (b) Linear resistance vs. $1/T$ measured under $V_g^*(T)$. Solid line: fitting of $R(T) \sim \exp(-E_a/K_{\rm B}T)$ with $E_a \sim 6$ meV. Inset: resistance vs. T measured under $V_g^*(T) - 5$ V and a bias of $V = 1$ mV.

decreases from 290 K to 80 K. At even lower temperatures, the I-V curve exhibits nonlinearity with suppressed conductance near $V = 0$, and the resistance increases with decrease in temperature. These results show that, when the Fermi level resides within the valence (or conduction band, data not shown), the small-gap semiconducting SWNT sample behaves like a quasi-metal. The positive slope in $dR(T)/dT$ for $T > 80$ K can be attributed to reduced phonon (e.g., twiston) scattering [42, 65] as temperature decreases. The resistance upturn at lower temperatures could be due to small barriers existing at the metal-tube junctions due to band bending effects.

The origin of the observed small bandgap could be attributed to the nontrivial curvature effects predicted to exist in small-diameter SWNTs [40–42]. The SWNT is not an S-SWNT with large primary bandgap on the order of 600 meV expected for an S-SWNT with $d \sim 1.3$ nm. The transport characteristics of the SGS-SWNT differ significantly from S-SWNTs described in [4–6]. Out of approximately 20 systematically characterized individual SWNT samples so far, we observed three SWNTs exhibiting small-gap semiconducting behavior described above. The electrical properties of SGS-SWNTs can also be

distinguished from metallic SWNTs, which usually show weak gate and temperature dependence, as described in Section 3.2. Indeed, the intrinsic electrical properties of individual small-gap semiconducting SWNTs are fully elucidated because of the low contact resistance produced with the controlled CVD fabrication apparoach, and our results present unambiguous evidence for the existence of small-gap semiconducting nanotubes.

3.4. Electronic Properties of Semiconducting Carbon Nanotubes

SWNTs with (m, n) indices are semiconducting when $m - n \neq 3 \times integer$, and the bandgap can vary from $\sim$2 eV to below 0.5 eV. Devices consisting of such nanotubes display strong dependence on both the temperature and the gate bias, and therefore have great potential to be used as building blocks for nanoelectronic systems. Extensive studies have been carried out by many groups [4–6]. We will focus our review on nanotube devices fabricated via the CVD method. This growth method produces SWNTs with diameters dispersed in the range of $\sim$0.7–3 nm, and the resulting semiconducting tubes have energy gaps $\sim$1–0.25 eV according to band structure calculations. We review temperature-dependent transport characteristics of individual semiconducting SWNTs of various tube diameters. Transport mechanisms through semiconducting SWNTs at various temperatures are elucidated. SWNT transistors exhibiting I-V characteristics resembling those of silicon-based p-MOSFET are obtained, with transconductance two orders of magnitude higher than previous tube-transistors.

Results reviewed here were obtained with two SWNTs (sample #1 and sample #2) contacted by 20-nm-thick nickel electrodes with 60-nm-thick gold on top. The lengths of the SWNTs between electrodes were $\geq$3 μm. Degenerately doped silicon wafers with 500-nm-thick thermally grown oxide on the surface were used as the substrates. The heavily doped substrate is conducting at low temperatures and was used as a back-gate. The diameters of SWNTs were determined from AFM topographic height data.

I-V curves obtained at room temperature with sample #1 are shown in Figure 13a. The nanotube has a relatively large diameter of 2.8 ± 0.1 nm and exhibits a highly linear I-V curve with resistance $\sim$340 kΩ measured at zero gate-voltage (V_g). Positive gate-voltages progressively reduce the linear conductance of the sample (Fig. 13a). At $V_g > 3$ V, the conductance is suppressed by four orders of magnitude from that at $V_g = 0$. These I-V characteristics are signatures of hole-doped semiconducting SWNTs acting as p-type transistors. When the gate-voltage is further increased, the conductance of the sample remains suppressed until the gate-voltage reaches $\sim$40 V, where appreciable recovery in the conductance is observed (Fig. 13a, inset).

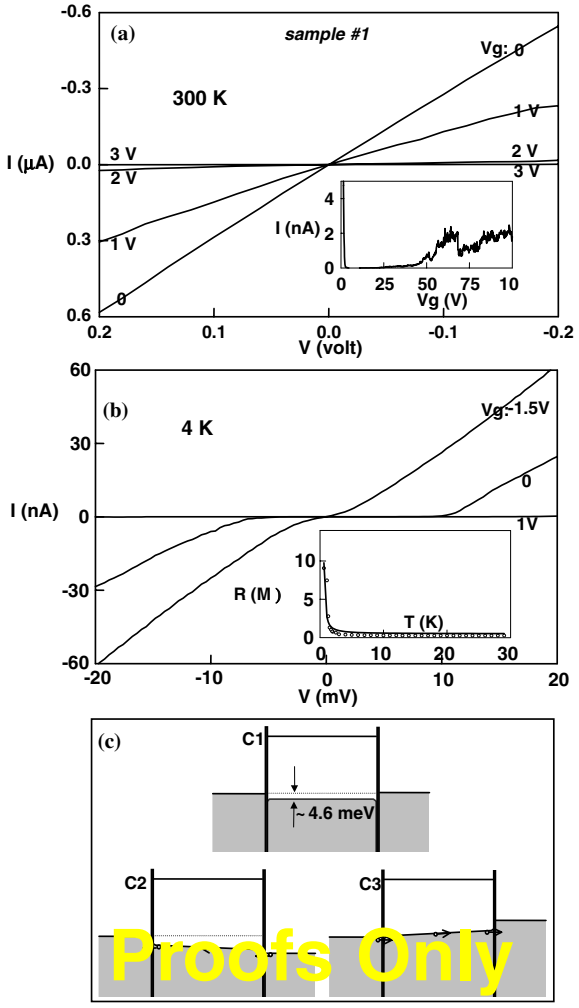

Figure 13. (a) Room temperature I–V curves of sample #1. Inset: current vs. gate voltage recorded at 300 K under a 10-mV bias voltage. (b) I-V curves under $V_g = -1.5$, 0, and +1 V at 4 K. Inset: R vs. T. Solid line shows the $\exp(-E_a/K_BT)$ fit. (c) Band diagrams.

The zero-gate linear resistance versus temperature curve for the $d = 2.8$ nm semiconducting tube is shown in the inset in Figure 13b. The resistance increases from 340 kΩ to 1 MΩ as temperature is lowered from 300 K to 25 K. Below 25 K, the temperature-dependent resistance can be fitted into $\sim \exp(-E_a/K_BT)$ with $E_a \sim 4.6$ meV (solid line in Fig. 13b, inset). At 4 K, a gap $\sim$20 mV is observed in the I-V curve and the sample is insulating in the bias range $|V| < \sim$10 mV under zero gate-voltage (Fig. 13b). The insulating region is found to be significantly suppressed by applying a -1.5 V gate-voltage. Applying a positive gate-voltage (e.g., $V_g = +1$ V in Fig. 13b) leads to a larger insulating region in the I-V curve.

The results obtained with sample #1 are interpreted by the diagrams shown in Figure 13c. First, the nanotube is suggested to be uniformly hole-doped along its entire length. It is not plausible in our sample that hole-doping

at the contacts due to the work function mismatch [4] ($\phi_{\rm Ni} = 5.5$ eV vs. $\phi_{\rm NT} \sim 4.5$ eV) extending throughout the 3-μm tube length. We also used Ti, Al, and Ag with similar work functions as graphite, and Mg and Sm with lower work functions than graphite to contact nanotubes. The resulting semiconducting tubes were all hole-doped. The dope mechanism acts upon the entire length of a nanotube, instead of being localized near the contacts. Uniform hole-doping along the length of a semiconducting SWNT was also suggested to be the case in [4]. Second, each contact is suggested to consist of a serial resistance (black bar in Fig. 13c) and a junction formed with the p-type nanotube bridge. The junction formation arises from the separation between the nanotube Fermi level and the valence band $E_{\rm FV} = E_{\rm F} - E_{\rm V}$ and sets a barrier to electron transport.

The junction barrier is responsible for the observed thermally activated transport shown in Figure 13b, and is determined to be $E_a \sim 4.6$ meV for sample #1 from the temperature-dependent linear resistance data. At room temperature, the sample exhibits low resistance (340 kΩ) and linear I-V (under zero gate-voltage) since the junction barrier is easily overcome by thermal energy $E_a < K_{\rm B}T = 26$ meV. Positive gate-voltages cause the valence band to shift down away from the Fermi level, leading to higher barriers and thus less conducting states, as seen in Figure 13a. At 4 K where $K_{\rm B}T \ll E_a \sim$ 4.6 meV, thermally activated transport through the system is quenched. The sample is in an insulating state near zero bias as seen in Figure 13b. For bias voltages $|V| > \sim$10 mV, the sample is turned into a conducting state. Analyses of the I-V curve after the turn-on find that current increases by approximately three orders of magnitude in the bias range of 7 mV to 14 mV, and can be fitted into $I \sim \exp(-{\rm c}/V)$ where c is a constant. These results suggest that electron transport at 4 K is via a tunneling mechanism. Under a sufficiently high bias voltage V, electron tunneling occurs through the reverse biased junction as shown in schemes C2 and C3 in Figure 13c. Similar transport mechanisms were reported in conventional metal-semiconductor-metal systems by Lepselter and Sze [66].

The observed conductance recovery suggests that high positive gate voltages convert the sample into an n-type system from p-type, with further increase in gate voltage enhancing the conductance of the n-type system. The bandgap can be estimated to be on the order of $E_g \sim 150$ meV, compared to the theoretically expected $E_g \approx 200$ meV for the $d = 2.8$ nm semiconducting tube.

Figure 14 shows the results obtained with sample #2 consisting of a semiconducting SWNT with $d = 1.3 \pm 0.1$ nm and length $\sim$5 μm. Linear resistance of the sample $\sim$3.4 MΩ at room temperature, and increases upon cooling according to $\sim \exp(-E_a/K_{\rm B}T)$ with $E_a \approx$ 25 meV (Fig. 14, inset). At 4 K, an insulating gap is observed within $\sim \pm 0.6$ V in the I-V curve shown in

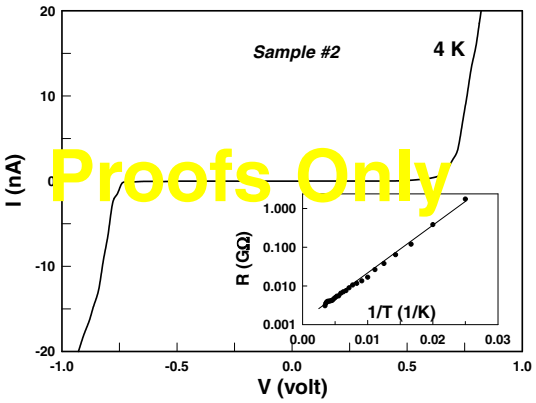

Figure 14. I-V curve recorded at 4 K with sample #2 ($V_g = 0$). Inset: R (in log scale) vs. $1/T$.

Figure 14. Within our model, the junction barrier height is $E_a = E_{\rm FV} \sim 25$ meV, which is comparable to the room temperature thermal energy. Note the expected energy gap for the $d \sim 1.3$ nm tube, $E_g \sim 0.6$ eV. Beyond the insulating gap in I-V, the current is found to increase by three orders of magnitude when the bias is increased from 0.5 to 0.9 V, which points to the tunneling transport mechanism described earlier. Because of a higher junction barrier than that in sample #1, the small-diameter tube sample requires much higher bias voltage to establish significant tunneling currents through the reverse biased junction.

We found that at room temperature and zero gate-voltage, the resistance of semiconducting SWNTs were typically in the range 160–500 kΩ for tube diameters > 2.0 nm. The resistance of smaller-diameter SWNTs with $d \leq 1.5$ nm were typically on the order of megohms or higher. Hole-doping to larger-diameter tubes led to smaller $E_{\rm FV}$ and thermal activation barriers, as found by temperature-dependent measurements. The lower resistance for larger-diameter semiconducting SWNTs can be attributed to the lower transport barrier at the metal-tube junctions, and better electrical coupling may have been made with larger-diameter tubes and contributed to their low resistance. For small-diameter tubes, we observed no conductance recovery under gate-voltages up to +100 V. This can be attributed to the large energy gaps ($\geq$0.6 eV) relative to the gate efficiency and large band bending effects at the junctions.

All of our semiconducting nanotube samples exhibit an interesting feature in the I-V curves under high bias voltages. The I-V curves show remarkable asymmetry with respect to the polarity of the bias voltage when $|V| > \sim$1 V. I-V curves obtained at room temperature with sample #1 over a bias range of 3 to -3 V are shown in Figure 15. In the negative bias side, the current initially scales linearly as $|V|$ but reaches saturation and stays constant under large negative biases. In the positive bias side, the current increases continuously as the bias voltage increases. The asymmetry in I-V is

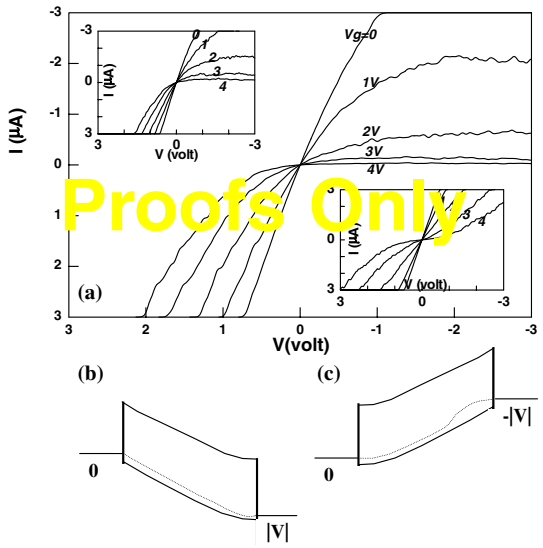

Figure 15. (a) I–V curves recorded at 300 K with sample #1 for $V = 3$ to -3 V. Left inset: I–V curves recorded after exchanging the source-drain electrodes. Right inset: symmetrical I–V curves obtained under symmetrical bias. (b), (c) Band diagrams for positive and negative drain bias, respectively.

found to be independent of which metal electrode is ground (source) or biased (drain). Data recorded after exchanging the source and drain electrodes show nearly unchanged asymmetry in I-V (Fig. 15, left inset). Symmetrical I-V curves can be obtained (Fig. 15, right inset) under symmetrical bias by scanning V in the range of -3 to 3 V while biasing the two electrodes at $-V/2$ and $+V/2$, respectively. These results suggest that the observed asymmetrical I-V curves are not caused by asymmetrical parameters such as different contact resistances at the two metal-tube interfaces, but are inherent to the metal/tube/metal system. It is concluded that for a significantly high bias voltage, the current flow $|I|$ is not solely determined by the absolute value of voltage $|V|$ across the system and can be influenced by the bias configuration.

The I-V asymmetry in bias polarity was consistently observed in all of the six independent semiconducting SWNT samples studied. We suggest that the origin of this asymmetry is local-gating of the biased drain electrode. Under a given positive gate-voltage (e.g., $V_g = 2$ volts), the nanotube can be considered to have a constant hole-density along its length. In a negative bias configuration $[0, -|V|]$ (e.g., $|V| = 3$ V), the quasi-Fermi level, shown as dotted line in Figure 15c, of the nanotube is further away from the valence band near the drain where the local-gating voltage is more positive relative to the drain. This results in a reduced hole-density in the tube section near the drain and thus reduced conductance. Saturation occurs for large $|V|$ because of the competing roles of driving and gating of the drain bias voltage. This phenomenon can be related to local carrier depletion and channel pinch-off by negative drain bias in a conventional p-type MOSFET [67]. In a positive bias configuration $[0, |V|]$, local hole enrichment is induced in the nanotube section near the drain where the quasi-Fermi level is closer to the valence band as shown in Figure 15b, which results in a more conducting system.

The results presented here are significant in terms of enabling high-performance nanotube transistors. First, the I-V curves of our samples resemble those of conventional p-MOSFET [67]. Second, high voltage gain and transconductance are obtained with our devices. Sample #1 shown in Figure 13 exhibits positive voltage gain of $\Delta V_{ds}/\Delta V_g|_{I=3\ \mu\text{A}} \sim 3$ compared to the maximum gain of $\sim$0.35 obtained previously [4]. A transconductance of $\partial I_{ds}/\partial V_g\ |_{V=100\ \text{mV}} \sim 200$ nA/V is obtained with this sample, which is two orders of magnitude higher than previous results with SWNTs [5]. Transconductance normalized by the tube width is $\sim$0.1 mS/μm, which is comparable to silicon-based p-MOSFETs. Three independent SWNTs with diameters in the range 2.5–3 nm are found to exhibit high transconductance between 100 to 200 nA/V. The high transconductance is a direct result of the low linear resistance of these samples (hundreds of kilohms). Samples consisting of small-diameter tubes ($d < 1.5$ nm) exhibit lower transconductance in the range of 1 to 10 nA/V because of their high resistance (>several megohms).

To summarize this section, we presented detailed results of electron transport measurements of individual semiconducting SWNTs. Hole-doping to the nanotubes is found to be independent of the type of contacting metal. Transport in semiconducting SWNT samples involves thermal activation at high temperatures and tunneling through a reverse biased metal-tube junction at low temperatures. Electrical properties of SWNTs with various diameters are elucidated. Local-gating effects lead to a bias polarity-associated transport phenomenon and high-transconductance SWNT transistors.

3.5. Nanotube *p-n* Junctions

Energy band engineering employing techniques such as doping [68] and epitaxial growth [69] has played a revolutionary role in microelectronics in the past fifty years. By selectively doping a semiconductor such as silicon or germanium into n- or p-type, rectifying current-voltage (I-V) characteristics have been observed with p-n junctions. Remarkably, negative differential resistance (NDR) has been observed in devices such as Esaki diodes [70] exploiting the interband tunneling in degenerately doped p-n junctions, and double barrier resonant tunneling diodes [69] (DBRTD) exploiting resonant tunneling through an epitaxially grown double barrier system in GaAs/AlGaAs. These devices have found widespread

applications as high-frequency amplifiers and oscillators. Inspired by the above-mentioned success in microelectronics, one of the authors (C. Zhou) focused on studying energy band engineering of carbon nanotubes for future nanoelectronics while working at the Dai group at Stanford. By selectively doping part of a semiconducting nanotube into *n*-type with potassium vapor while the rest remained *p*-type, we have demonstrated nanoscale *p*-*n* junctions with rectifying *I*-*V* characteristics. Interestingly, Esaki diodes have been realized by fine-tuning of the doping level and a back-gate potential. These diodes exhibit a negative differential resistance up to 180 K and a remarkable peak valley ratio (PVR) $\sim 2:1$ at 10 K. Below 10 K, this nanotube system exhibits strong single-electron tunneling effect due to nonuniform doping; however, negative differential resistance is observed instead of orthodox Coulomb staircase. This result points to resonant tunneling through a double barrier system with semiconducting emitter and collector, resembling the GaAs/AlGaAs DBRTD.

Our devices consist of individual single-walled carbon nanotubes grown by a chemical vapor deposition method on catalytically patterned SiO_2 surface. As shown in Figure 16, this tube is contacted at both ends by Ni/Au pads serving as the source and drain electrodes. The degenerately doped silicon substrate is used as a back-gate electrode, separated from the nanotube by 500 nm SiO_2. Upon finishing, the left half of the nanotube is covered by 340-nm polymethylmethacrylate (PMMA) while the right half remains exposed. The nanotube used in this study has a diameter ~2 nm and a length of 3.5 μm

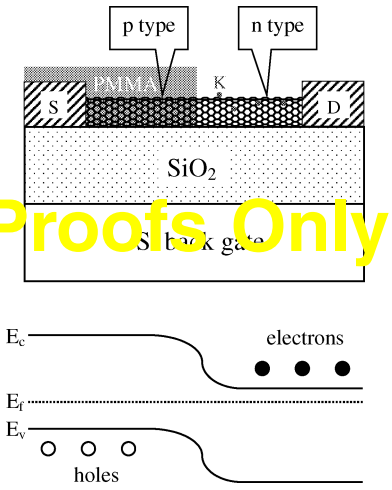

Figure 16. A schematic diagram of the nanotube *p*-*n* junction. The nanotube is grown atop the Si/SiO_2 substrate with a chemical vapor deposition method. Both ends of the tube are contacted with deposited Ni/Au pads working as source and drain electrodes with the underlying silicon substrate serving as a back-gate. The left half of the tube is covered by ~4000 Å PMMA. Upon exposure to potassium vapor, the right half can be doped into *n*-type by the adsorbed potassium atoms while the left half remains *p*-type, yielding a *p*-*n* junction. A band diagram is also shown in this figure, where E_c, E_f, and E_v represent the conduction band, the Fermi level, and the valence band, respectively.

between the source and drain electrodes. Prior to doping this tube device has been confirmed to be *p*-type, as manifested by a monotonically reduced conductance under positively increasing gate biases. Such an unintentional doping has been consistently observed by other groups [4, 5] and is believed to result from electron transfer from the nanotube to the environment such as adsorbed gas species, trapped charges in the silicon oxide, and the metal electrodes.

Potassium doping is carried out in high vacuum by heating up a potassium source placed 2 cm away from the sample while the conductance of the devices is carefully monitored [54]. The right half of the nanotube is in direct contact with the adsorbed potassium atoms, and hence sufficient electron transfer from potassium atoms to the tube can revert the doping of this segment from *p*-type to *n*-type. In contrast, the left half segment of the tube should remain *p*-type since it is separated from the potassium atoms by a thick layer of PMMA. A band diagram for such a *p*-*n* junction is shown in Figure 16. During the doping the conductance of the device first decreases to almost zero, indicating holes in the right half tube are neutralized by electrons donated by K atoms and hence no charge carriers exist. Continued doping restores the conductance, albeit lower than the starting value, pointing to enriched electrons in the right half tube. Upon further doping the conductance seems to saturate and the time duration for the whole doping process is about five to ten minutes.

Detailed electric measurements are first taken at room temperature to elucidate the *p*-*n* junction characteristics, as shown in Figure 17. Figure 17a displays the current-gate bias (I-V_g) characteristics with 1 mV bias applied to the drain electrode and the source electrode grounded. The I-V_g curve shows very rich structures: while the conductance with V_g between -20 V and -12 V (regime I) is almost zero, a conductance bump is observed at -12 V $< V_g < -7$ V (regime II); the conductance becomes suppressed again for V_g between -7 V and -1 V (regime III); thereafter the conductance increases almost monotonically with increasing gate bias (-1 V $< V_g <$ 20 V, regime IV). This result is dramatically different from the results of a simple *p*-type or *n*-type nanotube, which should exhibit monotonic decrease or increase of conductance under positively increasing gate bias. Instead these features can be explained as a *p*-*n* junction with electron and hole concentrations controlled by the back-gate: from left to right, regime I, II, III, and IV can be assigned as p^+n, p^+n^+, pn^+, and nn^+, respectively. In regime I, a high negative gate moves the conduction band and valence band up relative to the Fermi level, and thus degenerately dopes the left half tube with holes and depletes electrons from the right half tube, resulting in a p^+n junction. As shown in Figure 17b, a rectifying I-V is observed at $V_g = -12$ V with a rectifying ratio $\sim 3:1$, qualitatively consistent with a leaking *p*-*n* junction

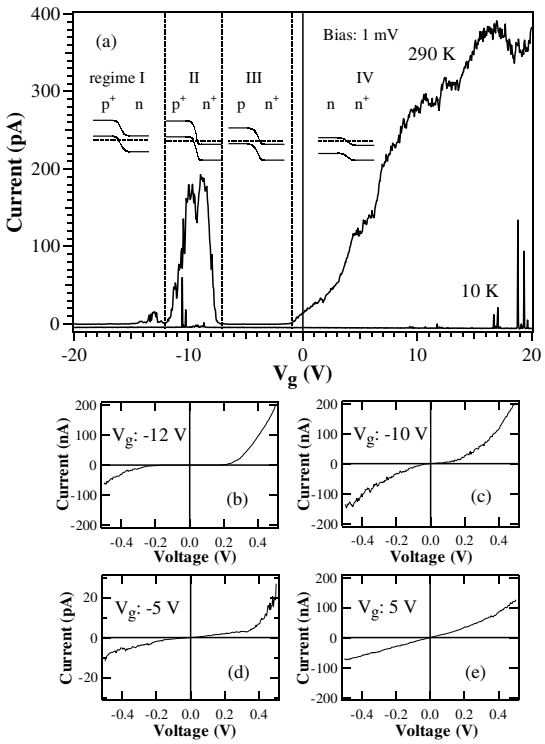

Figure 17. (a) Current-gate bias curves of the nanotube device taken after the potassium doping. The top curve is taken at room temperature, which can be divided into regime I, II, III, and IV, corresponding to p^+n, p^+n^+, pn^+, and nn^+ junctions, respectively. Typical I-V curves taken at these four regimes are shown in (b), (c), (d), and (e). The lower curve in (a) is taken at 10 K, exhibiting Coulomb blockade.

predicted by [9, 10]. In regime II, the negative gate is insufficient to deplete electrons in the right half tube, therefore rendering a p^+n^+ junction. Substantial tunneling can occur due to a thin depletion layer, yielding an almost symmetrical I-V curve at $V_g = -10$ V, as observed in Figure 17c. In regime III, the gate bias is sufficient to reduce the hole concentration in the left half tube, resulting in a pn^+ junction and significant reduced conduction. This is confirmed once again by the rectifying I-V curve at $V_g = -5$ V seen in Figure 17d with $\sim 3:1$ rectifying ratio. Further increase of the gate bias reverts the left half tube from p-type to n-type and hence a monotonic increase in conduction is observed. I-V curves taken in this regime show little rectifying behavior, as seen in Figure 17e.

We now estimate the number of potassium atoms adsorbed on the nanotube surface. When $V_g = 0$ V, contribution from the electrostatic doping induced by the gate should be negligible; therefore, it is reasonable to assume all the electrons at the right half tube are donated by the adsorbed potassium atoms at zero gate bias. Since the right half tube seems to be depleted of electrons at $V_g = -12$ V, the number of electrons in the right half tube at zero gate bias can be estimated as $C_g * 12$ V,

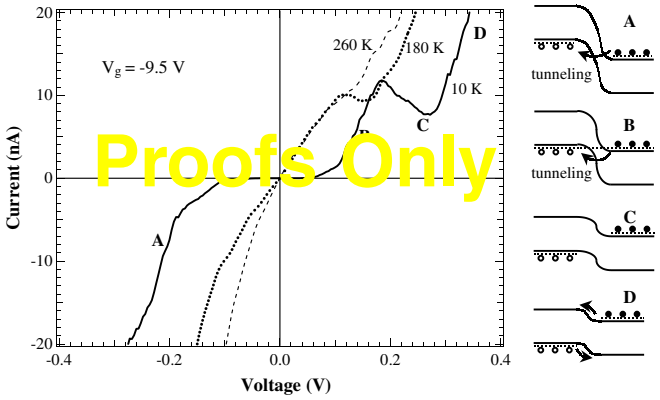

Figure 18. Current-voltage curves of the p^+n^+ junction at $V_g = -9.5$ V taken at 260, 180, and 10 K. The NDR feature is observed at 180 K and becomes more pronounced at lower temperatures. The peak valley ratio in the curve taken at 10 K is $\sim 2:1$. The underlying Esaki diode mechanism is shown in the insets. Around zero bias (the top left inset), substantial interband tunneling can occur due to a thin depletion layer. Under proper forward bias (the lower right inset), the conduction band in the n-region is lined up with the midgap of the p-region, leading to suppressed tunneling and the negative differential resistance.

where C_g is the gate capacitance of the nanotube. This value is found to be ~ 1428 e/μm with the gate capacitance estimated to be 19 aF/μm utilizing the method reported in [5]. Such an electron concentration corresponds to ~ 6.3 potassium atoms per 1000 carbon atoms, sufficiently high to cause degenerate doping [71]; that is, the Fermi level is moved into the conduction band.

Thereafter the sample is cooled down to liquid helium temperature without breaking the vacuum. Decrease in conductance is observed over all the V_g regimes at lower temperatures and the I-V_g curve breaks into periodic discrete peaks with regions of suppressed conduction in between at 10 K, indicating Coulomb blockade behavior [7, 8], as shown in the lower curve in Figure 17a.

We first focus on regime II where the device should behave as a p^+n^+ junction. Figure 18 shows three I-V curves at $V_g = -9.5$ V taken at 260 K, 180 K, and 10 K, respectively. A monotonic I-V characteristic is observed at 260 K, whereas the I-V curve taken at 180 K exhibits a striking NDR feature with the peak at $V = 0.12$ V and the valley at 0.16 V. This NDR feature becomes increasingly pronounced as the temperature goes down, and a PVR of $\sim 2::1$ is observed in the I-V curve taken at 10 K. This observation can be explained with the well-known Esaki diode mechanism [70]. As shown in the band diagrams in Figure 18, an Esaki diode consists of a p-n junction with both the p-side and the n-side degenerately doped. At zero bias, electrons can tunnel from the conduction band of the n-region into the valence band of the p-region, provided the depletion region is sufficiently thin. This leads to a finite resistance (linear I-V) around zero bias and substantial conduction under reverse bias. Under a proper forward bias, the conduction band in the n-region is shifted up and lined up to the midgap

of the p-region. With no available state for electrons to tunnel into, the interband tunneling is suppressed, leading to reduced conduction and the NDR feature. Further increase in forward bias lowers the potential barriers for the electrons and holes and hence the normal conduction mechanism of a forwardly biased p-n junction becomes dominant, leading to an increasing current.

Since the right half tube is depleted of electrons around -12 V and the left half is depleted of holes around -7 V, we can estimate both the electron and hole concentration at $V_g = -9.5$ V to be $C_g * 2.5$ V $\sim$298 e/μm. This doping concentration corresponds to 1.32 electrons or holes per 1000 carbon atoms. From this we estimate the depletion width to be $\sim$2 nm according to the calculation in [71], sufficiently thin for the interband tunneling of the Esaki diode mechanism to occur. It is interesting to note that this depletion width yields an active device size of 1.6 nm in diameter and 2 nm in length, with a volume of only 4 nm^3, a true nanoscale electronic device. Our observation is also consistent with the Esaki diode mechanism on the following merits: (1) as long as $T > 10$ K where the system is not complicated by the charging effect, the NDR feature appears only around $V = 0.16$ V, consistent with the fact that the NDR of an Esaki diode should appear only at forward bias; (2) this NDR feature is observed only in the "conductance bump" region in regime II, indicating the necessity of a p^+n^+ junction; (3) this NDR feature can be observed even at 180 K, inferring the energy scale involved is very large compared to the thermal energy at 180 K. Assume the valley ($V = 0.16$ V) of the I-V curve at 180 K corresponds to the conduction band in the n-region lined up with the midgap of the p-region; we can estimate the bandgap of this tube to be 0.32 eV, close to the 0.35 eV estimated from the diameter of this tube.

The peak in the I-V curve taken at 10 K is shifted to larger bias compared to the I-V curve at 180 K. In addition, a gap opens around zero bias in the I-V curve at 10 K. These two features were not observed with orthodox Esaki diodes; however, this can be understood since our device has two metal-nanotube junctions connected in series with the intratube Esaki junction. The electrical characteristics of such metal-tube junctions typically evolve from linear I-V curves with low resistance at high temperatures to I-V curves with gaps around zero bias and very high resistance at low temperatures, as reported in previous sections. These increased series resistances at low temperatures lead to the shift of the peak position to higher bias and the appearance of a gap in the I-V curves.

Thus far the NDR feature induced by the Esaki diode mechanism has been completely elucidated. Interestingly, at low temperatures ($\sim$10 K) more NDR features are observed in both regime II and regime IV, where the system is dominated by Coulomb blockade. Hereafter we focus on the I-V characteristics in regime IV

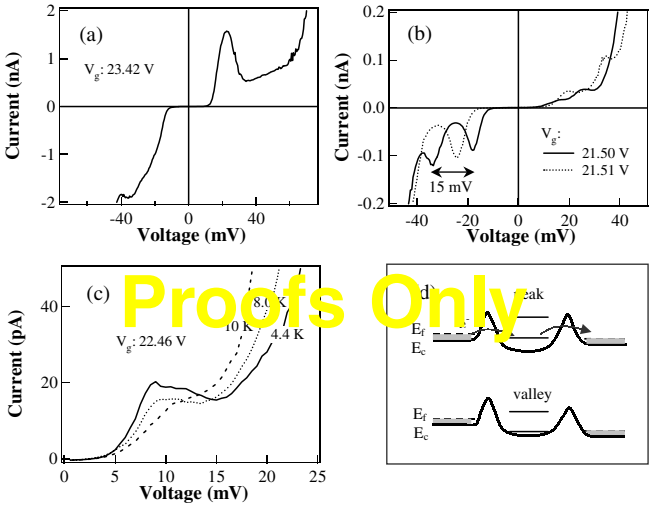

Figure 19. (a) A typical I–V curve of the nn^+ junction taken at 4 K showing a NDR feature with a PVR $\sim$ 3:1. (b) Two I–V curves taken at $V_g = 21.50$ V and 21.51 V, showing very sensitive gate dependence. (c) Temperature dependence of a NDR feature at $V_g = 22.46$ V. This NDR feature is very pronounced at 4.4 K, but evolves into a step at higher temperatures. (d) Proposed band diagrams for a nonuniformly doped carbon nanotube. Part of the tube becomes separated from the rest by two lightly doped tunneling barriers. When a single-electron level resides between E_f and E_c of the emitter (the upper diagram), electrons can tunnel from the emitter onto the quantum dot and then to the collector, leading to substantial conduction. Further increase in bias can bring the single-electron level below E_c, and hence no resonant tunneling can occur, leading to a NDR feature.

to avoid the complication brought by the Esaki diode behavior in regime II. Several typical I-V curves in this gate bias regime are shown in Figure 19a and b. Instead of Coulomb staircase expected from an orthodox single-electron transistor, pronounced NDR features are observed in all these plots, with PVR as high as 3 : 1.

These NDR features are qualitatively different from the NDR feature shown in Figure 18, as summarized below. (1) NDR is observed in both bias directions and sometimes multiple peaks can be observed, as shown in Figure 19b. (2) These NDR features are very sensitive to the gate. For example, the gate bias for those two curves in Figure 19b differs by just 0.01 V and the I-V curves are very different. (3) Compared to the Esaki diode NDR occurring $\sim$0.16 V, these NDR features typically show up at relatively low bias (<50 mV), indicating a small energy scale is involved. (4) Consistently, these NDR features generally exhibit very sensitive temperature dependence. As shown in Figure 19c, the NDR feature evolves from a very pronounced peak at 4.4 K to a knee at 10 K.

This phenomenon can be explained by a nonuniform doping profile along the nanotube. Fluctuations in the dopant concentration along the carbon nanotube cause the conduction band to fluctuate relative to the Fermi level, presumably due to the random aggregation of the deposited potassium atoms. Under a proper gate bias, part of the heavily doped tube with E_c below E_f becomes

separated from the rest by two lightly doped segments (Fig. 19d), resulting in a system similar to a single-electron tunneling transistor (SET). A remarkable difference is that the electrons in the emitter and collector of this system have a narrow distribution in energy (between E_c and E_f), as compared to a continuous occupation below E_f in metallic electrodes in an orthodox SET. Such a device should show a blockade of conduction around zero bias and an increase in current when the bias is sufficiently high to bring one single-electron level into the bias window. Further increase in the bias brings this single-electron level below E_c, and hence there is no state available in the quantum dot for electrons in the emitter to tunnel onto, leading to a reduction in conduction and the negative differential resistance. In this regard the physics is similar to that of a double barrier resonant tunneling diode realized in epitaxially grown GaAs/AlGaAs structures, except that the discrete energy levels are dominated by charging effect instead of quantum confinement effect.

From the maximum gap size (~80 mV) in the I-V curves, we can estimate $U + \Delta E$ to be about 40 meV, where U is the charging energy and ΔE is the energy level spacing. Since both U and ΔE are inversely proportional to the length of the nanotube dot [7, 8] with a typical ratio of $U/\Delta E \sim 6:1$, we can estimate the charging energy to be ~34 meV and the energy level spacing to be ~6 meV. This corresponds to a nanotube quantum dot length of 0.1–0.15 μm, consistent with the assumption that the quantum dot is only part of the nanotube. The width of the peaks displayed in Figure 19b, c, and d is typically ~5 meV, indicating the level of degeneracy $(E_f - E_c)$ in this system is about 5 meV. It is important to note that the PMMA coverage is not necessary to observe this type of NDR features. Indeed, similar behavior has been observed in devices with the whole tube exposed to the potassium vapor.

To summarize our work on nanotube p-n junctions, we have successfully demonstrated nanotube p-n junctions, Esaki diodes, and double barrier resonant tunneling diodes by selectively doping part of a semiconducting nanotube. By tuning the back-gate bias from -20 V to 20 V, p^+n, p^+n^+, pn^+, and nn^+ junctions have been realized. Both p^+n and pn^+ junctions exhibit diode-like I-V characteristics with small rectifying ratios ~3:1 at room temperature. The p^+n^+ junction behaves as an Esaki diode with negative differential resistance observable up to 180 K and a peak-valley ratio ~2:1 at 10 K. A second type of NDR features has been observed at low temperatures for both p^+n^+ and nn^+ junctions, resulting from a double barrier system induced by nonuniform doping along the carbon nanotube. Further exploitation of this doping technique should lead to more interesting nanotube devices as well as intriguing physics.

3.6. Carbon Nanotube Complementary Field-Effect Inverters

Inspired by the success of the CVD technique, we decided to exploit the unique advantage of the CVD technique to demonstrate small integrated nanotube systems, that is, logic gates. Initially a p-type metal-oxide-semiconductor (PMOS) inverter is demonstrated by connecting a load resistor to a p-type nanotube FET, which consists of a CVD grown individual single-walled nanotube with metallic source/drain electrodes and the silicon substrate back-gate. Further integration of this p-type nanotube FET with an n-type nanotube FET produced by potassium vapor doping leads to the demonstration of a more sophisticated complementary metal-oxide-semiconductor (CMOS) inverter.

All the SWNT devices used in this study were prepared with patterned chemical vapor deposition and microfabrication for the source/drain contacts [6, 22, 23]. By utilizing a p-type nanotube transistor with I-V characteristics shown in Figure 20a, an inverter can be readily constructed to output logic "1" when the input is "0" and to output "0" when the input is "1." As shown in the inset in Figure 20b, a resistor is connected between ground and the source of this nanotube device, while a bias of

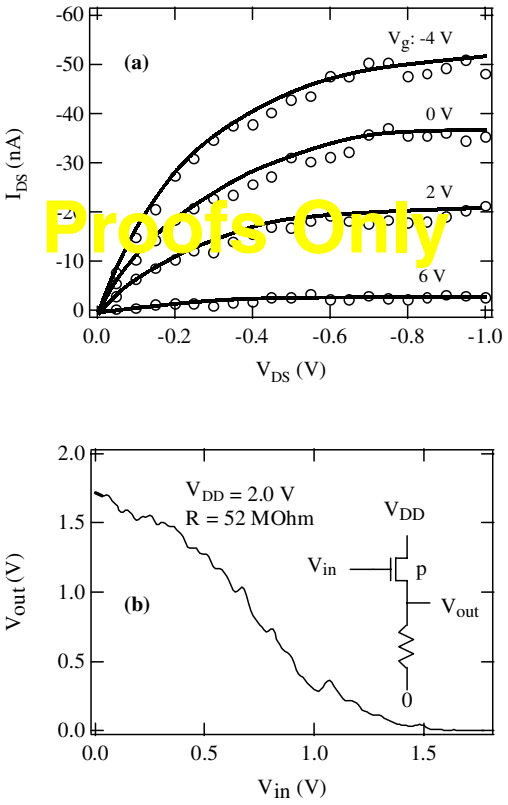

Figure 20. (a) I–V characteristics of a typical p-type nanotube field-effect transistor showing both linear and saturation regimes. (b) Transfer characteristics of a PMOS inverter. Inset: Schematic diagram of the PMOS inverter.

2.0 V is supplied to the drain. The silicon gate is used as the input while the potential of the output electrode is monitored. As shown in Figure 20b when the input voltage is swept from 0 to 2 V, the output varies from 1.7 V to almost 0 V, working just like an inverter. When the input is low, that is, logic "0," the *p*-type transistor is on, and hence most of V_{DD} is dropped across the resistor, leading to a high output, that is, logic "1." On the other hand, as we increase the gate bias from 0 V to 2.0 V, the nanotube transistor is gradually turned off and becomes increasingly resistive. Consequently more and more voltage is dropped across the nanotube instead of the load resistor and eventually the output voltage is almost 0, fulfilling the function of an inverter. In our experiment, the inverter turns on (logic "1") at 0 V and turns off at 1.5 V and a gain of about 1 has been measured. Furthermore, since the voltage ranges of input and output are almost the same, these inverters can be integrated in a cascade manner without malfunctioning.

Despite the proper functioning of the above-mentioned system, it does not stand as an integrated system since an external resistor is used. In addition, PMOS inverters are inferior to CMOS inverters when power consumption, stability, and noise suppression are considered. Therefore, we decided to pursue complementary inverters by integrating a *p*-type nanotube transistor with an *n*-type nanotube transistor. *n*-Type nanotube transistors are obtained by doping a nanotube with potassium vapor, following previous effort [9, 54]. Figure 21 shows *I*-*V* characteristics of a typical *n*-type nanotube transistor obtained this way. The conductance is found to increase under positively increasing gate bias, going from 34 nS at $V_g = 0$ V to 600 nS at $V_g = 6$ V. This kind of behavior is the signature of *n*-type field-effect transistors. Interestingly, *I*-*V* curves of this device are rather linear as compared to the saturated *I*-*V* curves in Figure 20a. The origin of such a difference is not fully understood at this moment.

Combining *p*-type and *n*-type transistors, complementary field-effect inverters can be easily demonstrated. We utilize two separate nanotube transistors and connect them together with a bonding wire about 2 mm in length. One nanotube transistor is exposed to the potassium vapor and hence doped into *n*-type, while the other is hidden from the potassium vapor and remains *p*-type. Details of this process can be found in our previous publication [6]. Figure 22a and b displays the I-V_g characteristics of a *p*-type and an *n*-type nanotube transistor, respectively. Under a source-drain bias of 10 mV, the *p*-type nanotube exhibits substantial conduction (17 nA) at $V_g = 0$ V and little conduction with V_g beyond 2.5 V, signature of a depletion-mode *p*-type transistor. On the contrary, the *n*-type nanotube transistor displays little conduction around $V_g = 0$ V and significant conduction with $V_g > 2.5$ V, indicating an enhancement-mode *n*-type transistor. These two devices are then biased in the configuration depicted in Figure 22c, inset. We applied a 2.9-V bias to the V_{DD} terminal and swept the gate electrode (input) from 0 V (defined as logic "0") to 2.5 V (defined as logic "1"), and the transfer characteristic

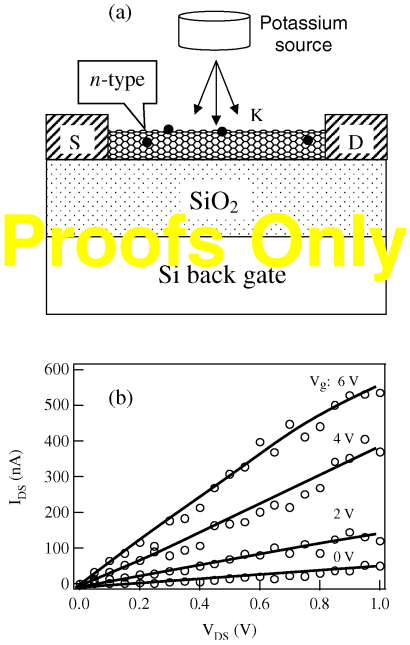

Figure 21. (a) Schematic diagram of the potassium doping set-up. (b) *I*–*V* characteristics of a potassium doped nanotube transistor showing *n*-type behavior.

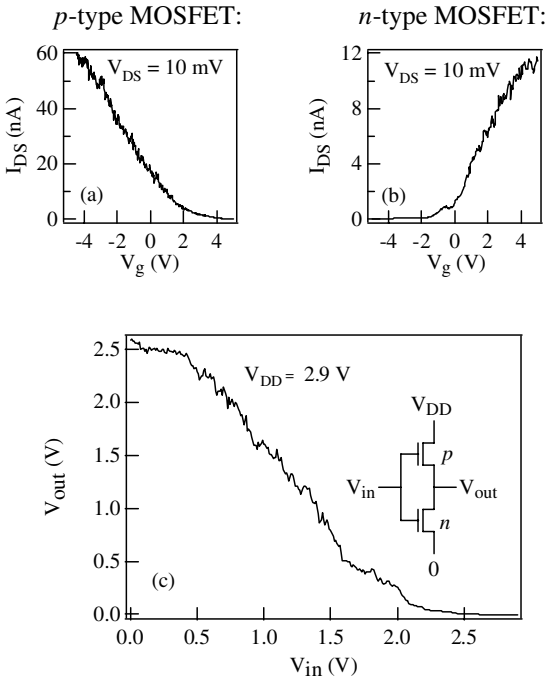

Figure 22. (a) I–V_g curve for a *p*-type nanotube transistor. (b) I–V_g curve for an *n*-type nanotube transistor. (c) Transfer characteristics of a CMOS nanotube inverter constructed by connecting the *p*-type transistor with the *n*-type transistor.

curve is shown in Figure 22c. When the input voltage is low (logic "0"), the *p*-type transistor is on, meaning the conductance is high, and the *n*-type transistor is off, meaning the conductance is low. As a result, the output of this inverter is close to V_{DD}, thereby producing an output of logic "1." As the input voltage is increased, the conductance of the *p*-type nanotube decreases and the conductance of the *n*-type nanotube increases, leading to a decreasing output voltage. With sufficiently high input, the *p*-type nanotube is turned off, whereas the *n*-type nanotube is turned on. The combined effect is an output voltage close to the ground, that is, the logic "0," as clearly demonstrated in our experiment. Our results show that the output starts to decrease at $V_{in} = 0.4$ V and is cut off at $V_{in} = 2.0$ V, leading to a gain as high as 1.7. Thus far the operation of a CMOS nanotube inverter is fully demonstrated, though an ideal inverter should exhibit a stepwise V_{out} versus V_{in} behavior, whereas our results in Figures 20 and 22 show a small flat region at low and high values of V_{in} with almost a linear variation in between. The observed behavior may be due to the fact that the *p*-MOS tube transistor is somewhat leaky and the threshold control for both transistors is not perfect, all of which reflects the fabrication difficulties in nanoelectronics at this early stage. An additional drawback is that the system must be kept in vacuum because of the potassium doping used. Further advance should involve development of doping methods that are stable in ambient atmosphere.

Thus far we have demonstrated both PMOS and CMOS inverters based on carbon nanotubes. Although the PMOS inverter requires an external load resistor, the CMOS inverter represents a rudimental integrated system by connecting a *p*-type nanotube transistor with an *n*-type nanotube transistor. Both types of inverters can function at room temperature and possess gains equivalent to or greater than 1. Our work demonstrates the advantage of the CVD growth technique and should stimulate more effort toward integrated nanoelectronic systems.

3.7. Logic Gates Using Carbon Nanotubes

Parallel to our successful demonstration of complementary carbon nanotube inverters, significant progress has been made in producing integrated nanotube systems by Avouris and co-workers at IBM [72] and Dekker and co-workers [73] at Delft University independently. While a silicon substrate back-gate is used by Avouris and colleagues [72], a local aluminum gate is used in Dekker's transistor structure [73], which enables substantial electrostatic doping and also allows independent gating of individual transistors in an integrated system. This new fabrication approach starts with patterning of aluminum gates on top of Si/SiO_2 substrates using e-beam lithography, followed by the formation of a native oxide layer

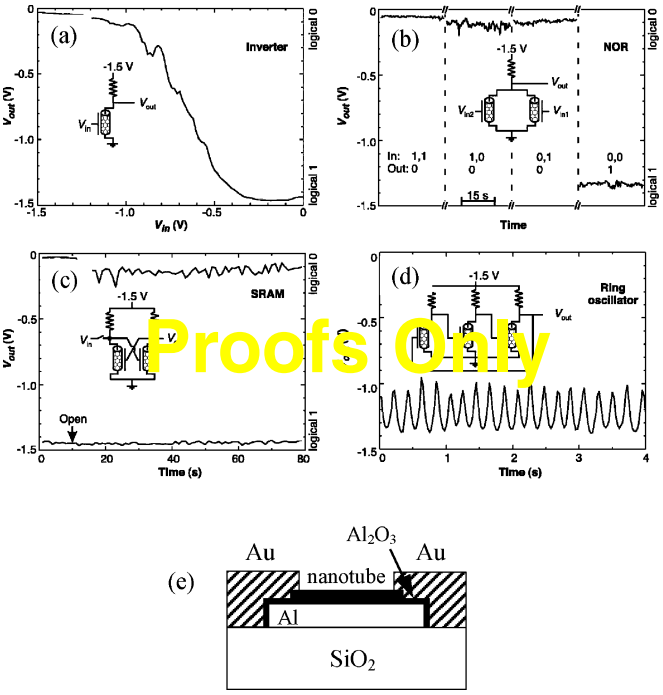

Figure 23. Nanotube logic circuits. (a) Input–output characteristics of a nanotube inverter. (b) Output of a nanotube NOR gate for the four possible input states (1,1), (1,0), (0,1), and (0,0). A voltage of 0 V corresponds to logic "0" and a voltage of −1.5 V represents logic "1." (c) Output voltage of a nanotube SRAM vs. time. The device is shown to hold its state after it is forced into a stable state and the input switch is opened. (d) Output of a three-inverter ring oscillator. (e) Schematic diagram of the transistor structure showing Al_2O_3 as the gate dielectric. Modified from [29], J. F. Colomer et al., *Chem. Phys. Lett.* 317, 83 (2000). © 2000, Elsevier Science.

atop upon exposure to air, as shown in Figure 23d. Subsequently, single-walled carbon nanotubes are spun onto the substrates from a dichloroethane suspension. Those nanotubes lying atop the Al/Al_2O_3 gates are located and contact electrodes serving as the source and the drain are fabricated with e-beam lithography. This method produces nanotube transistors with only ∼2 nm Al_2O_3 working as the gate dielectric, leading to substantial electrostatic doping.

Such transistors can be classified as enhancement-mode *p*-type field-effect transistors, since a strong modulation of the channel current can be achieved by applying a small negative gate bias. Based on this fabrication approach, Dekker and colleagues have demonstrated a family of logic gates, including an inverter, a NOR gate, a static random access memory (SRAM), and a ring oscillator [73], as shown in Figure 23a–d. The inverter is constructed by connecting a nanotube transistor with an off-chip 100-MΩ resistor (shown in Fig. 23a), similar to the *p*-type inverter described in Section 3.5. In addition, by simply replacing the single transistor in the inverter with two nanotube transistors in parallel, a NOR gate has been demonstrated. The output is logic "1" (∼−1.5 V) only when both inputs are logic "0" (∼0 V), so that

both transistors are turned off, as shown in Figure 23b. Furthermore, Dekker and co-workers have also demonstrated a SRAM based on the architecture of conventional flip-flop memories using two inverters, where the output of each inverter is connected to the input of the other inverter. There are two possible stable states for such devices: $(0, 1)$ or $(1, 0)$ for $(V_{\text{in}}, V_{\text{out}})$. Figure 23c clearly shows this device can hold its state after being forced into either the $(0, 1)$ or $(1, 0)$ state, therefore working as a memory device. Finally, the ring oscillator has been demonstrated by connecting three inverters in a loop, where a 5-Hz oscillation is observed since it has no stable state. Overall, the demonstration of such digital logic circuits with nanotubes represents an important step toward molecular scale electronics, though this approach still suffers from the lack of control over the nanotube positioning.

4. CONCLUSIONS

We have presented an overview of nanotube synthesis and electronic devices. Progress in nanotube science and technology has been built upon the success in nanotube synthesis. It is shown that the chemical vapor deposition technique produces high-quality individual single-walled carbon nanotubes at desired sites directly on substrates. This technique has led to the demonstration of a series of nanotube devices and integrated systems such as field-effect transistors, *p-n* junctions, nanotube Esaki diodes, and complementary inverters, in addition to single-electron transistors demonstrated with more conventional means. It can be envisioned that nanotubes will play a revolutionary role in nanoscale science and technology.

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