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Two-Dimensional Semiconductors: From Materials Preparation to Electronic Applications

Bilu Liu, Ahmad Abbas, and Chongwu Zhou**

Two-dimensional (2D) materials are layered materials featuring strong in-plane covalent bonding and weak intra-plane bonding, which allow them to be easily cleaved into atomically thin materials, and be stable in such thin forms. Initiated by graphene, there has been increasing research interest in the past few years in studying growth, electronic and optoelectronic applications, and many other applications of 2D materials. In this review, recent achievements in the controlled preparation of monolayer and few-layer 2D semiconductors are summarized, with an emphasis on transition metal dichalcogenides (TMDCs). General understanding for TMDC growth as well as approaches to grow large single crystalline TMDCs and wafer-scale manufacturing of continuous TMDC films are discussed. In the second part, the focus is on applications of 2D semiconductors in electronics, where several key issues—including how to form good electrical contacts between electrodes and 2D semiconductors, charge carrier scattering mechanisms, and short-channel effects—are discussed in detail. In the last section, the authors' perspective on the challenges and opportunities in the growth and electronic applications of 2D semiconductors is presented.

1. Introduction

In the past decade, two-dimensional (2D) materials such as graphene,[1] transition metal dichalcogenides (TMDCs),[2] and black phosphorus (b-P)[3–5] have gained the interest of scientists and engineers due to their versatile, unique properties, and their applicability in a wide range of applications. The large number of potential applications comes from the fact that 2D materials have a large variation in electronic, optical, thermal, chemical, and mechanical properties that makes them attractive for one or more particular applications. Currently, some of the most important electronic applications for 2D materials, especially 2D semiconductors, are digital electronics, radio-frequency (RF) devices, chemical sensing, optoelectronics, etc.

In general, 2D materials are composed of a layered structure that has strong in-plane chemical bonds and weak interaction in the out-of-plane direction (i.e., among different layers), which makes it possible to directly grow or cleave bulk materials to prepare monolayers or few-layers of most 2D materials. Compared to traditional bulk semiconductors, the fully depleted structure of 2D semiconductors has a clear advantage in terms of immunity against short channel effects, due to the very thin structure of monolayer 2D semiconductors (<1 nm). Consequently, researchers have aimed to demonstrate the use of field-effect transistors (FETs) made of 2D semiconductors in digital electronics, in order to potentially use highly scaled 2D devices in future digital applications.[6–8] For example, CMOS logic gates (e.g. NAND, NOR, XNOR), latch, edge-triggered register, and DC–DC converters have been demonstrated using MoS_2-based devices.[6,9] Moreover, the high charge mobility of some 2D materials, such as graphene and b-P, is attractive for high-speed RF devices, and demonstrations of the use of 2D material RF devices, on rigid or flexible substrates, have been shown. Digital inverters, frequency doublers, and analog amplifiers have been fabricated using various 2D materials.[10–14] In addition, chemical sensing is an important application of 2D semiconductors, because of their large surface-to-volume ratio, which enables a significant modulation of the electronic properties of materials by changing the interfacial environment. For instance, demonstrations of sensors based on various 2D material devices to detect NO_2 and NH_3 gases with high sensitivity have been made, in which the conductivity of the devices changed upon gas-species absorption due to charge transfer and contact modulations.[15–17] Finally, with a thickness-tunable band-structure and long exciton lifetimes, optoelectronics using 2D semiconductors appear to be of great importance for applications such as photodetectors, photovoltaic devices, light emission, etc.[18–24] For example, Xia et al. reported photodetectors

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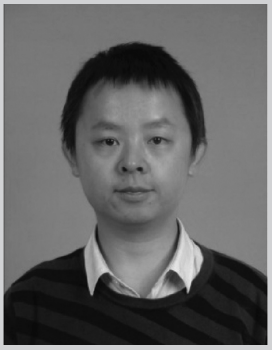
DOI: 10.1002/aelm.201700045

based on few-layer b-P that can detect light with wavelengths as long as 3.39 μm, which is in the mid-wavelength infrared regime.[25] The small bandgap of ≈0.3 eV makes b-P an appropriate 2D material for mid-wavelength infrared light absorption and consequently its detection.

In order to ensure proper and predictable utilization of 2D devices, understanding and control of key device metrics must be undertaken. **Figure 1** illustrates the key issues observed in a typical 2D semiconductor FET. These issues are arranged into four main categories: quality of channel materials, metal contacts, interfacial effects, and short channel effects. Although many of these issues are observed in traditional bulk semiconductor devices, the severity and impact of these issues on the device performance are expected to be different in the case of 2D semiconductors. For instance, because electrons in a 2D FET are confined in close proximity to the gate dielectric and substrate interfaces, the effects of interfacial scattering are more severe in comparison with traditional FETs made of bulk semiconductors. Moreover, there are some differences in the device structure and fabrication processes between 2D FETs and traditional FETs. For example, in most 2D FETs, the source/drain metal contacts the 2D semiconductors directly. On the other hand, highly doped source/drain regions are formed before metal contacts in traditional FETs. As a result, it is important to understand and solve major problems with 2D FETs in unique ways, so that optimized device performance may be achieved.

In this review, we will discuss major issues and obstacles associated with 2D electronics, and major scientific efforts to address these issues. First, we will discuss the structure, growth techniques, and problems associated with 2D semiconductor growth. The materials quality, uniformity and scalability are of extreme significance to the proper operation of 2D devices, and can influence major device metrics. In the second section, a detailed overview of 2D device contact concepts, techniques, and research efforts to improve the electrical contact will be discussed. The high contact resistance in most 2D devices severely degrades device current, affects device linearity, and presents a hurdle for scaling 2D FETs. Accordingly, using novel techniques to lower the contact resistance is crucial to the continuous progress of 2D electronics. In the third section, we will present and analyze different scattering mechanisms influencing the operation of 2D devices. Due to the atomically thin structure of 2D materials, various scattering mechanisms and charge traps have severe effects on the charge transport, thus preventing the device from approaching the theoretical predicted values of mobility, subthreshold swing (SS), and linearity. We will present recent research efforts guided toward understanding and reducing the unwanted effects from scattering and interfacial traps. In the fourth section, we will discuss short-channel effects in 2D semiconductor devices. It is known that the atomically thin and fully depleted structure of 2D semiconductors is a great platform for highly scaled short-channel FETs, due to the strong electrostatic control of the thin 2D channels compared to the drain electric field. We will analyze various short-channel effects, and their impact on different 2D semiconductor devices. Moreover, we will compare fully depleted silicon-on-insulator (FDSOI) technology with some 2D semiconductors, to highlight the advantages of using 2D semiconductors in electronics. Finally, we will discuss challenges facing the 2D electronics field and our deliberations on potential solutions that may solve these problems. We will also offer an outlook on the 2D electronics field based on



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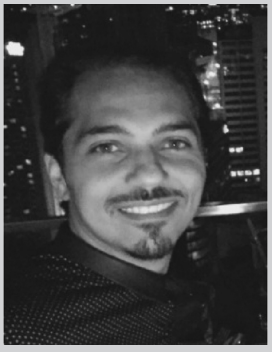

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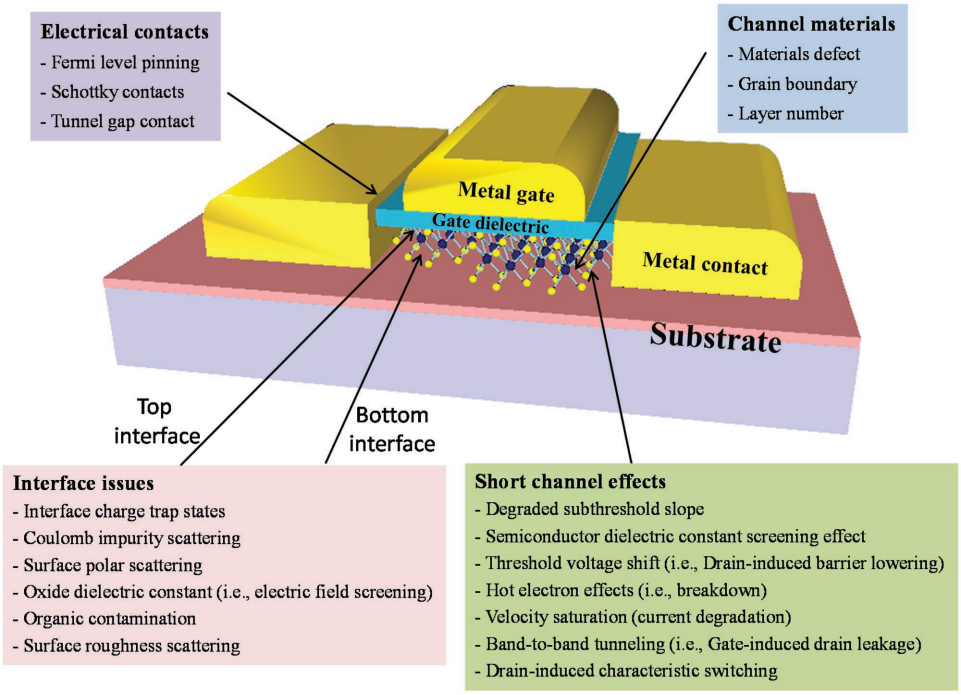

Figure 1. Schematic of a typical 2D semiconductor FET. The figure states key issues affecting 2D device performance related to channel materials, metal contact, 2D dielectric interfaces, and short channel effects.

current research efforts. This review will serve as a guideline of issues, concepts, and most recent progress associated with the 2D electronic device field, and it is complementary to the other specialized reviews and detailed studies that addressed some of the topics mentioned here.[26–29]

2. Preparation of 2D Semiconductors

Materials preparation is the first step towards their property investigation and any applications. The scotch-tape-based mechanical exfoliation approach has demonstrated successful isolation of many 2D materials from their bulk crystals to prepare monolayer or thin flakes of, for example, graphene, hexagonal boron nitride (h-BN), TMDCs including MoS_2, $MoSe_2$, WS_2, WSe_2, PtS_2, $PtSe_2$, b-P and black arsenic-phosphorus (b-AsP), and many others.[30–36] Usually, mechanical exfoliation can produce 2D materials with the best accessible quality, and thus the method is widely used to prepare samples for fundamental physics and device studies. However, this method is time consuming and cannot be scaled up. Liquid-phase exfoliation of 2D materials using various solvents with suitable interactions with 2D materials is a promising method to produce large quantity of 2D materials and their suspensions with low cost.[37,38] However, the quality of the produced materials is usually of concern for electronics, and the flake sizes are usually small. In this regard, high-temperature vapor-phase deposition methods such as chemical vapor deposition (CVD), metal-organic CVD (MOCVD), and physical vapor deposition (PVD), serve as promising approaches to produce monolayer or few-layer 2D materials with good quality, low cost, and scale-up capability. In this section, we will review recent achievements on how to synthesize large single crystals and how to achieve wafer-scale growth of 2D semiconductors with an emphasis on semiconducting TMDCs.

TMDCs with a general formula of MX_2 comprised of two elements, chalcogen (X) and transition metal (M). Therefore, precursors of X and M need to be introduced into the growth system to grow MX_2. There are several different ways to introduce such precursors, and **Figure 2** illustrates some representative setups for the growth of TMDCs reported so far. Figure 2a shows a PVD setup for the growth of MX_2, where powders of MX_2 can be directly used as source materials. Upon heating, MX_2 will sublimate or evaporate and can be transported by carrier gas to the high-temperature zone, and later deposited onto the receiving substrates, which are usually placed on the downstream side.[39,40] Usually there is no chemical reaction involved in such PVD processes. Figure 2b shows a CVD setup using two different sources for X and M for the growth of MX_2. This setup is the most commonly used configuration for TMDC growth based on the current literature. In this setup, a chalcogen source is usually loaded in the low-temperature zone in a furnace, while the metal source is loaded in the high-temperature zone. The commonly used chalcogen sources include powders of sulfur and selenium for the growth of MS_2 and MSe_2, while metal oxides or chlorides are common metal sources. The temperatures of the solid sources of chalcogen and metal can be controlled separately by using multi-zone furnaces, or by adding a heating belt for the chalcogen sources, which can be placed outside the heating zone of the furnace. In the PVD process shown in Figure 2a, the major parameters one can play with are the temperatures of MX_2 source and substrates, and the distance between them. In contrast, the process is much more complicated in the CVD method because two

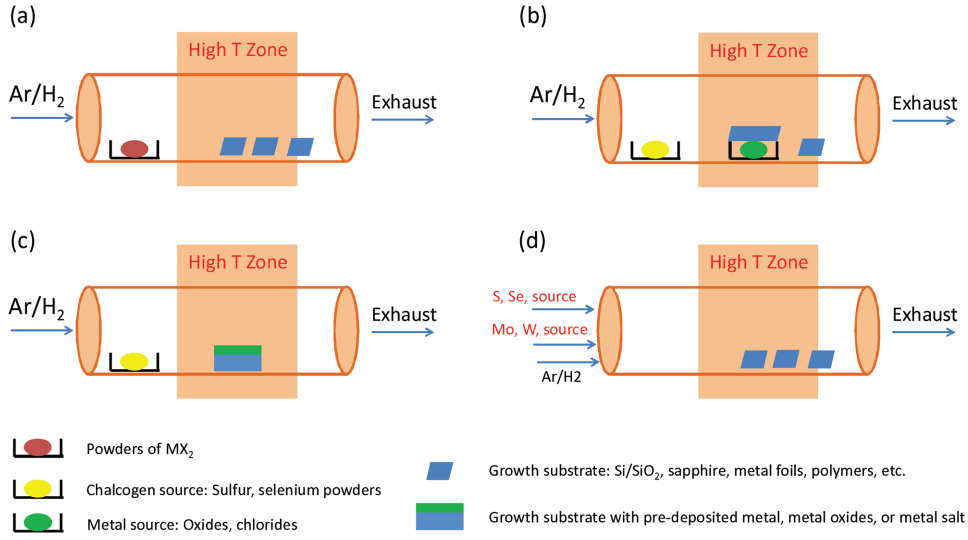

Figure 2. Representative set-ups for vapor phase deposition of TMDCs. a) PVD process using TMDC themselves as source materials. b) CVD process using solid powders of sulfur or selenium as chalcogen source, and metal salts (metal oxides or chlorides) as metal source. c) CVD process using solid powders of sulfur or selenium as chalcogen source, and sputtered metal film or spin-coated metal solution as metal source, to grow wafer-scale continuous TMDC films. d) MOCVD process using chalcogen and metal-containing gas phase sources.

precursors are used in CVD (metal and chalcogen), while only one precursor is needed in PVD (MX_2 itself). Nevertheless, one advantage of CVD over PVD is that one can potentially control the stoichiometry of the produced MX_2 sheets via tuning the amounts and temperatures of source materials, which is difficult in the PVD process. This point is important, especially considering the fact that chalcogen atom vacancy is a major defect type in TMDCs. Due to the use of solid precursors in Figure 2a and b, it is usually challenging to prepare uniform films of 2D materials. One alternative method, as shown in Figure 2c, is to pre-deposit metal sources via film deposition or spin-coating, followed by the introduction of sulfur or selenium vapors from evaporation of their powders, to achieve uniform growth of 2D materials. Another method is to use all-gas-phase precursors, where one can control the concentrations of each source precisely and separately, as shown in Figure 2d.

Large single-crystal growth is an important direction in the 2D materials growth field, because grain boundaries may hurt charge transport in 2D materials. There are two strategies to grow large crystals of 2D materials. The first is the use of single crystalline substrates, which can nucleate and epitaxially grow one single nucleus of 2D materials, or multiple 2D nuclei with the same orientation. When different nuclei merge together, they may have a chance to form one large single crystal, as reported in CVD growth of graphene.[41] Another strategy is to control and reduce the nucleation density of 2D materials, making the nuclei far away from each other and, therefore, each nucleus can have enough space to grow and eventually evolves into a large crystal. After several years of developments, the growth of large single-crystal domains of graphene is now relatively mature.[42,43] In a recent study, Wu et al. used a CuNi alloy catalyst and local feeding of gas precursors, and realized fast growth of inch-size single-crystal graphene with good quality.[42] The growth of large single crystals of h-BN of 0.3-mm size was also reported via catalyst engineering and nucleation density reduction.[44,45] For TMDCs, usually solid precursors are used (Figure 2a), which is different compared to graphene growth and brings inherent difficulty in fine controlling of the concentrations of precursors. Nevertheless, monolayer MoS_2 with edge size of 120 µm has been synthesized in some very early generation of MoS_2 synthesis papers (**Figure 3**b).[46] Recently, Chen et al. have developed an oxygen-assisted CVD process and realized the synthesis of 350-µm monolayer MoS_2 on c-plane sapphire substrate (Figure 3c).[47] The use of a small amount of oxygen is proposed to be able to prevent MoO_3 from poisoning the growth, and thus increases the lifetime of the precursor to grow large MoS_2 domains. Notably, via suppressing the nucleation density of MoS_2 and optimizing the concentration of gaseous precursor, Chai et al. have successfully realized the growth of large MoS_2 domains with edge length >300 µm in a routine CVD setup.[48] In another work, Gong et al. have reduced the nucleation density of $MoSe_2$ by tuning the flow rate of carrier gas, and reached millimeter-size single-crystal $MoSe_2$ growth.[49] The use of metal foils as substrates is another effective path to produce large grains of TMDCs.[50–54] For example, Gao et al. have used a Au foil as a substrate, sulfur and WO_3 powders as sulfur and tungsten sources, and realized the growth of triangular monolayer WS_2 with edge sizes on the order of a millimeter (Figure 3b).[50] Note that the sizes of single-crystal domains of TMDCs are still much smaller than that of graphene, and it is certainly true that lessons learned in graphene CVD can be used to increase the sizes of TMDCs in future synthesis, such as suppressing the nucleation density of 2D nuclei, and local feeding of reactants.

Wafer-scale manufacturing of 2D materials with good uniformity and controlled physical properties is important to move towards fabricating 2D electronics with uniform and reproducible performance. As mentioned above, the synthesis of TDMCs usually uses solid powder precursors such as MoO_3 and sulfur, which is hard to control and results in isolated

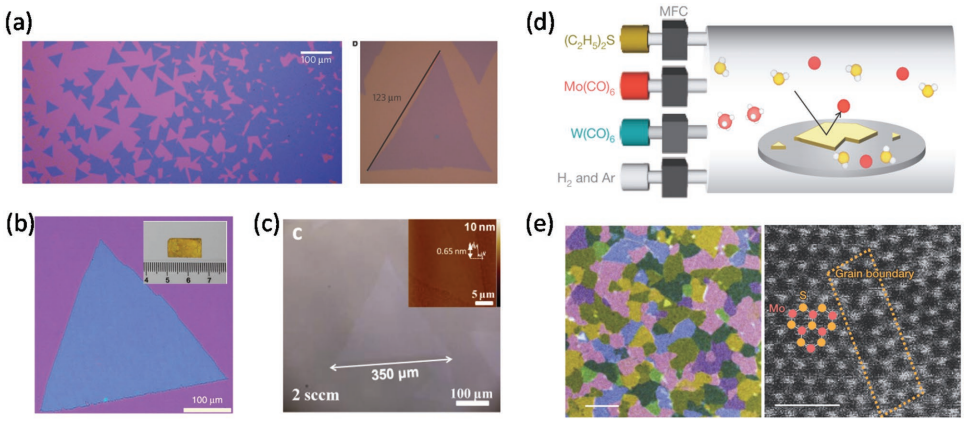

Figure 3. Recent advances in the growth of single crystalline large domains and wafer-scale manufacturing of monolayer 2D TMDCs. a) Growth of MoS_2 on Si/SiO_2 substrate, with edge length of single MoS_2 domain ≈120 μm. Reproduced with permission.[46] Copyright 2013, Nature Publishing Group. b) Growth of millimeter-size WS_2 on gold substrate. Reproduced with permission.[50] Copyright 2015, Nature Publishing Group. c) Growth of MoS_2 on sapphire substrate using oxygen-assisted CVD, with edge length of single MoS_2 domain reaching 350 μm. Reproduced with permission.[47] Copyright 2015, American Chemical Society. d, e) MOCVD setup and false-color dark-field TEM images of wafer-scale-manufactured continuous MoS_2 film. Reproduced with permission.[63] Copyright 2015, Nature Publishing Group.

domains of MoS_2 flakes. Several methods have been developed to grow relatively large-area uniform 2D films, including the use of pre-deposited thin films of metal oxides or metals (MoO_3, WO_3, Mo, W, etc.)[55–60] on growth substrate, or spin-coating a solution of $(NH_4)_2 \cdot MoS_4$, which serves as precursors for both Mo and S, followed by subsequent annealing.[61] These methods can improve the uniformity of the process and resulted in successful large-scale synthesis (Figure 2c). Atomic-layer deposition (ALD) techniques have recently been used to deposit uniform MoO_3 film, which was converted into centimeter-scale uniform MoS_2 films by reacting with sulfur in a later process.[62] Usually the controllability in terms of layer numbers is not great, and the grain size is very small (tens of nanometers) in the as-synthesized films, which limits the use of such 2D films for high-performance electronic applications due to the existence of a large number of grain boundaries. For ALD (and some other growth processes), a thin film of metal or metal oxide precursors is pre-deposited onto the growth substrates, followed by sulfurization process. Upon heating and sulfurization, metal or metal oxide film will be converted to huge numbers of small particles, leading to the formation of MX_2 films with rather small crystal sizes and consequently poor electronic performance. As shown in graphene growth[42] as well as MoS_2 growth[48] if one can reduce the nucleation density of MX_2 in such processes, it is entirely possible to grow large domain and wafer-scale coverage of MoS_2 films with high electronic performance via ALD and similar methods.

The use of all gas-phase precursors for both metal and chalcogen species may greatly improve the uniformity and controllability. Kang et al. have recently developed a MOCVD process which used $(C_2H_5)_2 \cdot S$ as a gas-phase source for sulfur, and $Mo(CO)_5$ or $W(CO)_5$ as a gas-phase source for Mo or W.[63] Using such a technique, they achieved 4-inch-wafer-scale growth of MoS_2 and WS_2 films on quartz substrates, and the as-grown monolayer films showed structural continuity and uniformity over the whole wafer (Figure 3a). The MOCVD growth was found to follow a layer-by-layer growth manner, which facilitated the growth of uniform monolayer films of MoS_2 and WS_2 with grain sizes as large as 10 μm. It is noted that the MOCVD growth needs a relatively long time—26 hours—to achieve a full coverage of the substrate with monolayer materials. The use of the MOCVD method for the growth of WSe_2 has also been reported,[64] but MOCVD-grown WSe_2 has much smaller grain sizes than that of MoS_2. The difference between MoS_2 and WSe_2 growth may stem from the use of different precursors and low reactivity of Se-based precursors.

In addition to the advances in the growth of single-crystalline 2D domains with large grain sizes and wafer-scale manufacturing, there are some other interesting and important aspects that deserve further investigation for 2D-materials synthesis. For example, low-temperature growth of 2D materials on flexible polymeric-based substrates,[65,66] which can utilize the good mechanical robustness of 2D materials for flexible, wearable, and bendable devices. The growth of TMDC alloys is another important topic, as one can easily tune electronic and optical properties of TMDCs by alloying with other metals or chalcogen elements.[4,57,67]

Understanding the growth mechanism of TMDCs is very important towards growth of large single crystals and wafer-scale manufacturing of TMDCs.[68–71] In a recent work,[68] Chai et al. studied the nucleation and growth mechanism of MoS_2 via in situ TEM observations, in which $(NH_4)_2 \cdot MoS_4$ was used as precursors for both S and Mo. They found that the growth of MoS_2 follows a temperature-dependent two-step growth behavior, i.e., low temperature vertical growth (<400 °C) and high temperature horizontal growth (>800 °C). This study is very helpful to understand the growth mechanism of MoS_2 and other MX_2 in both TEM environment and in CVD environment. Overall, compared to graphene growth, the microscopic mechanism of 2D semiconductor growth is far less understood and definitely needs more research efforts.

As another interesting 2D semiconductor, the synthesis of b-P is more challenging than graphene and TMDCs, as b-P synthesis usually requires high pressure (≈12 000 atm) or toxic bismuth- or mercury-based catalysts. Notably, Nilges et al. have developed a mineralizer-assisted vapor transport method,

which requires neither high pressure nor toxic catalysts, and demonstrated its great success in the growth of b-P and b-AsP bulk crystals.[34,72–74] It is definitely important to explore direct synthesis of thin b-P flakes or films, which can eliminate the mechanical cleavage process, and can significantly accelerate research of b-P. It is noted that Li et al. have demonstrated the synthesis of continuous b-P film on PET substrate by applying high pressure to red phosphorus; despite that, the domain sizes of b-P crystal are rather small at this stage.[75]

3. Electrical Contacts to 2D Semiconductors

2D semiconductors possess several advantages that make them very promising for next-generation electronics and optoelectronics, especially in the fields of short-channel transistors, flexible electronics, and new concept devices. First, 2D semiconductors with atomic thicknesses are the thinnest possible channel materials for electronics, which allows for extreme scaling-down of device dimensions and efficient gate-channel coupling.[76,77] Second, the surface of 2D semiconductors is dangling-bond free at the atomically thin limit, which is a significant advantage compared to silicon and III–V compound semiconductors, because the properties of those traditional semiconductors will change significantly when their thicknesses go down to a few nanometers. Third, despite the fact that they are atomically thin, 2D materials are usually mechanically robust, which allows for the fabrication of flexible electronics. It is known that Moore's law predicted that the density of transistors per unit area would double every 18 months. However, this trend became more and more difficult to maintain because we are encountering a fundamental physical limit as well as difficulties in nano-fabrication processes. In this regard, 2D semiconductors stand out and hold great potential to surpass silicon and III–V materials in the area of nano-electronics (i.e., devices with a short channel length).

Contact is a critical issue for many electronic and optoelectronic devices, especially for short-channel devices. In short-channel devices, the relative contribution of contact resistance to the whole device resistance will increase when compared to long-channel devices, and eventually contact may even dominate the performance of the whole device. Therefore, it is critical to achieve low-resistance contacts to 2D semiconductors. However, it is quite a challenge to achieve good contact for 2D semiconductors for the following reasons. First, the pristine surface of 2D materials is usually intact, without unsaturated atoms, which makes it difficult for them to form strong interface bonds with contact metals, leading to an increased contact resistance. Second, the commonly used approach to decrease contact resistance in silicon and III–V semiconductor electronics is degenerate substitutional doping. This doping technique is difficult to apply to 2D semiconductors because it will inevitably modify the properties of the 2D semiconductor channels, due to the ultrathin 2D-semiconductor body. Third, the contact areas between 2D semiconductors and contact electrodes are usually small, especially for small-dimension devices, which results in large contact resistance. In the past several years, researchers have developed several strategies aimed at improving the contacts in 2D semiconductor electronics (**Figure 4**), as will be discussed in the following paragraphs.

Figure 4a shows a typical structure of a back-gated FET using 2D semiconductors as channel materials, which are electrically contacted by two contact electrodes (i.e., source (S) and drain (D)). It is well documented that the contact nature (Ohmic or Schottky) and the Schottky barrier height at metal–semiconductor junctions are determined by the work function of contact metals (φ_{Metal}) and the electron affinity (χ) of semiconductors. For example, for an n-type semiconductor, the nominal height of the as-formed Schottky barrier (φ_{SB}) can be described as

$$\varphi_{SB} = \varphi_{Metal} - \chi \quad (1)$$

Based on this principle, one can, to a certain degree, control the metal–semiconductor contact nature by using metals with different work functions.[78–82] For example, Das et al. have studied contacts between multi-layer MoS_2 and four kinds of metals with different work functions, and found that the Schottky barrier heights are related to the work functions of the metals used.[78] Among the four metals Sc, Ti, Ni, Pd, Sc has the lowest work function of 3.5 eV, and it forms the smallest Schottky barrier height with MoS_2. Accordingly, the Sc-contacted MoS_2 devices showed the best performance among these four contact metals. By selecting metals with different work functions, one can make either n-FET or p-FET by aligning the metal Fermi energy to either the conduction or valance bands of the semiconductors. For example, MoS_2 is usually an n-type semiconductor when using metals as contacts; however, with

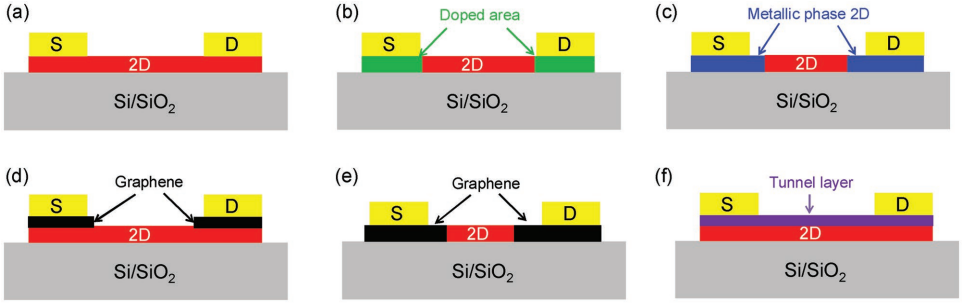

Figure 4. Current strategies to improve electrical contacts in 2D semiconductor FETs. a) Play with types of contact metals and processing recipe. b) Doping of contact areas. c) 1T-2H phase-engineered in-plane heterojunctions. d) Graphene top contact. e) Graphene edge contact. f) Inserting a tunnel layer between 2D semiconductors and contact electrodes.

the use of very high work function MoO_x as contacts, Javey et al. have successfully demonstrated p-FET based on MoS_2.[80,81] In the case of WSe_2, the polarity of the transistors can be easily tuned into either p-type or ambipolar by using high-work-function metals such as Pd, or relatively low-work-function metals like Au or Ti. This fact has been demonstrated in both mechanically exfoliated samples and CVD-grown WSe_2.[71,82,83] However, it should be noted that the Fermi level pinning effect exists in many TMDC-metal systems, which makes the situation quite complicated, and one cannot directly calculate the height of a Schottky barrier using simple equations. In addition to the types of metals, the process parameters are also found to be very important in determining the contact properties of TMDC devices. For example, English et al. have recently revealed that by improving the chamber vacuum from 10^{-6} to 10^{-9} Torr during Au-electrode deposition, a three-times-lower contact resistance (R_c) of 740 Ω μm can be achieved in Au-contacted few-layer MoS_2 devices.[84] The contact resistance value was measured based on the transfer length method (TLM), and the devices were found to be stable for four months. The authors believe that high-vacuum processing can yield a cleaner interface between Au and MoS_2, which in turn will reduce R_c and improve the device performance. It is well known that after device fabrication, a post annealing step, either in vacuum or in an inert environment, is routinely used to improve device performance and stability.[32,85] In general, an additional annealing step may remove surface contaminants (such as absorbents or resist residues) leading to a more close-to-perfect interface between the metal electrodes and semiconductors. It has also been reported that annealing graphene devices leads to the dissolution of carbon into contact metals (Ni or Co), which will form strong covalent bonds and results in a small R_c.[85]

The second approach to reduce R_c is to dope the contact area, as shown in Figure 4b. A similar approach is using in the current semiconductor industry. For example, Javey et al. have demonstrated potassium- or NO_2-doping of WSe_2 transistors, which could improve the device ON current significantly.[82,86] In addition, by selectively doping the contact areas while protecting the channel part against exposure to potassium or NO_2, both high ON current and high ON/OFF ratio transistors have been obtained. Doping of a TMDC transistor using other chemicals such as chloride molecules or amine-rich chemicals has also been reported by Ye et al.[87] However, there are a few drawbacks of such chemical doping techniques. For example, the dopants are not stable over time, and the technique may not be able to achieve high spatial resolution. As TMDCs represent a large family of materials, it is possible to form substitutional doping (i.e., using another metal atom to substitute matrix metal atoms in MX_2). Recently, Zhou et al. have fabricated such devices using unintentionally doped WSe_2 as channel materials and intentionally doped WSe_2 as the contact part. The intentionally doped WSe_2 was put between the metal electrode and unintentionally doped WSe_2.[88] Specifically, WSe_2 doping was realized by adding Nb during synthesis, to obtain $Nb_{0.005}W_{0.995}Se_2$. With such a 2D/2D (unintentionally doped WSe_2 layer as channel/intentionally doped $Nb_{0.005}W_{0.995}Se_2$ layer contact) architecture, the authors have achieved low R_c of 300 Ω μm, high ON/OFF ratio $>10^9$, and ON-current exceeding 320 μA μm^{-1} for few-layer WSe_2 transistors. However, this method relies on multiple transfer steps and cannot be scaled up at this point. In the future, if one can realize CVD growth of WSe_2 with Nb-doped edges, it will be possible to fabricate wafer-scale WSe_2 transistors with low R_c and high performance.

Figure 4c shows another approach to achieve low R_c contact in TMDC transistors, i.e., formation of 1T/2H phase junctions. TMDCs have different phases, for example, 1T and 2H, which possess distinct properties. For example, 2H-phase WSe_2 and MoS_2 are semiconductors, while metastable 1T-phase WSe_2 and MoS_2 are metals. It has been noted that 1T and 2H phases have reasonably similar structures and lattice constants, and can transform to each other reversibly. For example, by immersing 2H MoS_2 or WSe_2 in n-butyl lithium for tens of hours, it will convert into 1T MoS_2 or WSe_2.[89,90] Taking advantage of this unique feature, Chhowalla et al. have fabricated an in-plane heterostructure between 1T and 2H MoS_2. Later, by using 2H MoS_2 as channel and 1T MoS_2 as contact, they fabricated transistors based on such phase-engineered MoS_2 and achieved a record low R_c of 200–300 Ω μm.[89] The same approach also works for CVD-grown MoS_2 and WSe_2, demonstrating the generality of such a phase-engineered in-plane heterojunction method in obtaining low R_c and high-performance TMDC transistors.[76,90,91] In principle, such a seamless heterojunction contact concept is a rather general approach and could be adopted to many other materials systems; for example, carbon nanotube and graphene nanoribbon (GNR) systems, and graphene and GNR systems.[92] This approach could be important in GNR transistors because a large Schottky barrier is a key limiting parameter toward high performance GNR transistors, especially for narrow width GNRs. Similar to the situation of chemically doped contact, 1T-phase MoS_2 and WSe_2 are not stable, and the device performance will degrade during exposure to air. This drawback limits practical applications of such phase-engineered in-plane heterojunction devices. One approach to solve this problem is to encapsulate the whole device immediately after phase conversion, to avoid exposure to air and to make it stable.

Using graphene is another effective approach to achieve good contacts to 2D semiconductors. There are two kinds of graphene based contacts, i.e., top contact (Figure 4d) and edge contact (Figure 4e). Graphene has a zero bandgap and its Fermi level can be easily tuned by applying an external field, which may result in a perfect energy-band alignment between graphene and different semiconductors. In principle, graphene can form ohmic contact to many semiconductors if a sufficiently high potential is applied to graphene to tune its Fermi level significantly. Duan et al. have fabricated MoS_2 transistors with graphene top contacts. The transistors showed a linear I_{ds}–V_{ds} relationship even at cryogenic temperatures down to 1.9 K, demonstrating the formation of real barrier-free contacts between graphene and few-layer MoS_2.[93] Accordingly, the authors have observed metal–insulator transition in such graphene-contact MoS_2 transistors, which could be easily masked if the contacts to the devices are Schottky contacts, further supporting the realization of a barrier-free contact. Such graphene-contacted few-layer MoS_2 transistors show two-terminal extrinsic mobility up to 1300 $cm^2\ V^{-1}\ s^{-1}$ at low temperatures. Here, one should note that barrier-free ohmic contact does not necessarily mean small contact resistance. This is because

there is no strong bonding between graphene and 2D semiconductors; instead, there is a van der Walls gap between them, which may lead to a relatively large R_c. Another drawback of this approach is that a sufficiently large overlap between graphene and 2D semiconductors is needed to achieve low-resistance contacts. To eliminate such van der Walls gaps between graphene and 2D semiconductors, a graphene-edge contact approach has been demonstrated (Figure 4e).[94] Such graphene-edge-contacted 2D devices can be fabricated by multiple scotch-tape-exfoliation and aligned-transfer methods, as shown by Hone et al.[94] In a more recent work, Park et al. developed a MOCVD process to grow lateral junctions of graphene and MoS_2 and WS_2.[95] They first patterned CVD-grown graphene with stripe gaps, and then filled in the gaps via MOCVD-grown TMDCs. In this way, wafer-scale lateral junctions between graphene and TMDCs have been grown. The transistors fabricated using graphene-contacted TMDC channels showed a linear I_{ds}–V_{ds} at room temperature and liquid helium temperatures, and a contact resistance of 30 kΩ μm. In this work, the authors raised the point that not only should the contact resistance be small, the total device volume (including contact volume) should be small as well. In this regard, this work demonstrates an interesting approach to realize relatively low-resistance ohmic contact with minimum possible device volume and at wafer-scale capabilities.

The last common approach to achieve good contact is to insert a thin tunneling layer between the 2D semiconductors and contact metals.[96,97] For example, Wong et al. used the ALD method to deposit thin Ta_2O_5 on top of CVD-grown MoS_2 and studied the effect of Ta_2O_5 thickness on the device performance of a MoS_2 transistor.[77] They found that the reduction of the Schottky barrier height by inserting a Ta_2O_5 layer leads to an exponential reduction of the contact resistance. Specifically, temperature-dependent measurements showed that a 1.5-nm-thick ALD-deposited Ta_2O_5 layer can reduce the Schottky barrier height of metal-contacted MoS_2 transistors from 95 meV to 29 meV. More recently, a similar approach was used by Liao et al.[96] Instead of using ALD-grown oxides, they used CVD-grown h-BN as a tunneling layer, which was inserted between metal electrodes and MoS_2. By using monolayer or bilayer BN, the Schottky barrier was greatly reduced without significant increase of the tunneling resistance. The Schottky barrier height and contact resistance were improved from 158 meV and 5.1 KΩ μm to 31 meV and 1.8 KΩ μm, after inserting such a thin BN layer. Consequently, MoS_2 transistors with such tunneling contacts showed an output current of 330 μA μm^{-1} and a mobility of 73 $cm^2\ V^{-1}\ s^{-1}$ at room temperature. These values were further increased to 572 μA μm^{-1} and 321.4 $cm^2\ V^{-1}\ s^{-1}$ at 77 K. The underlying mechanism of improved device performance by inserting such a thin tunneling layer is related to the formation of metal–insulator–semiconductor (MIS) contacts. The attenuation of metal-induced gap states in the insulator and/or electronic dipole formation at the insulator–semiconductor interface are believed to be responsible for the reduction of the Schottky barrier height during the formation of MIS contacts.[97]

4. Charge Scattering

Due to the atomically thin structure of 2D materials, electron transport is severely affected by the interface. Charge impurities, charge traps, surface optical (SO) phonons and interface roughness (**Figure 5**) can affect the charge transport in 2D

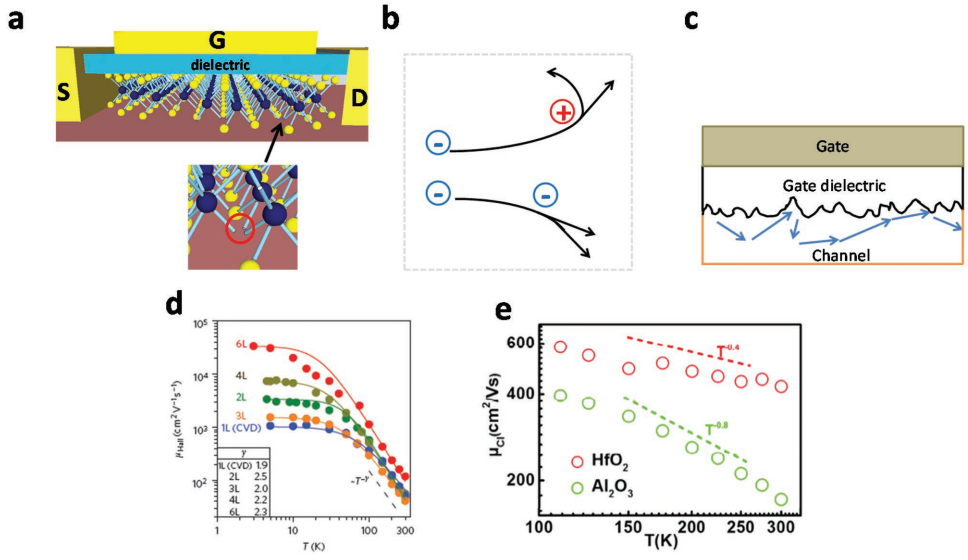

Figure 5. Scattering mechanisms and temperature dependent mobility of 2D TMDC FETs. a) Schematic of a MoS_2 FET with a sulfur vacancy in the channel identified by a black arrow. The magnified image in the bottom shows the site of the sulfur vacancy circled in red. b) An illustration of Coulomb impurity scattering showing an electron trajectory (black arrows) during a Coulombic interaction with a positive charge (top) and a negative charge (bottom). Various electron trajectories represent electrons with different energies and velocities. c) An illustration of surface roughness scattering at the dielectric–channel interface due to the gate electric field and uneven interface. The electron trajectory is shown in blue. d) Phonon-limited mobility of MoS_2 (monolayer to six layers) encapsulated in BN with γ of 1.69. Reproduced with permission.[103] Copyright 2014, Nature Publishing Group. e) CI-limited mobility of MoS_2 with HfO_2 and Al_2O_3 gate dielectrics, and with γ of 0.4 and 0.8, respectively. Reproduced with permission.[100] Copyright 2015, Wiley-VCH.

materials and consequently influence important device metrics such as subthreshold swing (SS), electron mobility, and threshold voltage. Additionally, scattering mechanisms in 2D materials induced by structural defects or vacancies (Figure 5a) can negatively affect the device performance in 2D materials. In this section, we will discuss some of the non-ideal effects in 2D-material-based FETs and the solutions to such effects in order to approach the ideal performance. These non-ideal effects are part of the reason for the large differences between theoretical predictions and experimental results. Accordingly, eliminating such effects is of extreme importance to the advancements of 2D electronic and optoelectronic applications.

Coulomb impurity (CI) scattering in 2D materials is the most common effect shared by different types of 2D materials (Figure 5b). In thin samples, such as monolayer 2D materials, CI scattering is pronounced because the interaction distance (d) of carriers transporting in the 2D materials with the impurities on the interface is very small. The scattering rate is proportional to $1/d^2$ which is very large for monolayer 2D-material FETs, where d is typically less than a nanometer. For a multilayer or a few-layer sample, the CI scattering is relatively small.[98] In order to minimize the effect of CI scattering, reducing the sources of CI (e.g., structural defects, dielectric dangling bonds, and interface contaminants) must be considered.

SiO_2 has commonly been the gate dielectric of choice for 2D-material FETs. However, the existence of non-passivated dangling bonds on the SiO_2 interface leads to large CI scattering in 2D FETs. Additionally, due to its relatively small dielectric constant compared to other high-k dielectrics, the screening of charge impurities is weaker in SiO_2 than in high-k dielectrics, which leads to higher scattering rates in SiO_2.[98–101] In recent years, the 2D dielectric h-BN has been introduced as an alternative dielectric for high-quality graphene, TMDC, and b-P electronics.[102–108] h-BN is free of dangling bonds and surface charge traps, and it is atomically flat, which significantly reduces CI scattering in 2D FETs. In addition, the optical phonon modes of h-BN have energies twice as large as those of SiO_2, which yields improved performance under high temperatures or high applied electric fields, and higher saturation velocities.[102] In the case of CI scattering being the dominant scattering mechanism, the use of h-BN with various 2D materials has led to significant improvements in FET mobility. For instance, Cui et al. achieved a low-temperature electron mobility of ≈1000 $cm^2\ V^{-1}\ s^{-1}$ for MoS_2 FETs where a MoS_2 flake was encapsulated between two h-BN flakes.[103] At low temperatures, the mobility is limited by interfacial scattering including contributions from CI due to the elimination of phonon scattering. However, the room-temperature mobility reported is still far from the theoretically predicted phonon limited mobility of MoS_2 (≈410 $cm^2\ V^{-1}\ s^{-1}$), which is possibly due to the contribution of polymer contamination during the transfer process.[109] Using similar techniques, Xu et al. achieved a low temperature mobility of ≈6000 $cm^2\ V^{-1}\ s^{-1}$ in a few-layer WSe_2 FET.[105] Nevertheless, more research on the CVD of h-BN and the control of area coverage, uniformity, thickness, and quality must be undertaken to improve the scalability of such a method.[110,111]

The measurements and characterization of CI scattering in a 2D material is important to the development of future 2D-material FETs. One powerful method to characterize CI scattering is variable temperature transport measurements (Figure 5d and e). As the temperature increases or electron density decreases, charge screening in 2D FETs weakens. Accordingly, the effect of CI scattering increases as the temperature increases due to the dependence of the 2D dielectric function on the static charge polarizability, which is a function of the temperature.[112] This can be seen by examining the scattering potential (φ_s) of a single CI for the long wavelength approximation which is $\varphi_s = -\frac{1}{\Pi}$, where Π is the temperature-dependent static polarizability and, for the long wavelength limit, is equal to,

$$\Pi = \frac{-gm_{\text{eff}}}{2\pi\hbar^2}\left\{1 - e^{\frac{-\pi\hbar^2 n}{2m_{\text{eff}}k_B T}}\right\} \tag{2}$$

where g is the valley-spin degeneracy, m_{eff} is the effective electron mass, n is the charge density, k_B is the Boltzmann constant, $\hbar$ is the Planck constant, and T is the temperature. The mobility trend resulting from the above phenomena must not be confused with the phonon-limited mobility, which gives rise to similar trends but with a different power exponent (γ) (i.e. mobility (μ) ~ $T^{-\gamma}$). In the case of MoS_2, the phonon-limited monolayer mobility has a theoretically predicted γ of 1.69,[109] while experimentally observed values up to ≈1.9 have been reported (Figure 5d).[103] On the other hand, γ values less than 1.69 have been observed due to CI scattering and interface charge traps. For instance, in CI-limited MoS_2 devices, Wang et al. observed γ values of 0.4 and 0.8 for HfO_2 and Al_2O_3 dielectrics, respectively (Figure 5e).[100]

Another route to reduce the effect of CI scattering is by screening the electric field perturbations induced by CI.[98–101] Using large-dielectric-constant materials (e.g. Al_2O_3 or HfO_2) instead of SiO_2 as gate dielectrics leads to increased screening of CI by the reduction of the electric field strength from charge impurities (*i.e.* $E = \frac{Q}{\varepsilon}$, where E, Q, and ε are the electric field induced by CI, CI charge per unit area, and the dielectric constant of the gate dielectric material, respectively). For example, Kim et al. used Al_2O_3 back-gate dielectric with multilayer MoS_2 to achieve an electron mobility >100 $cm^2\ V^{-1}\ s^{-1}$ and a nearly ideal SS (70 mV per decade).[113] Moreover, using this technique along with carrier screening at large electron densities yielded a room temperature mobility of ≈150 $cm^2\ V^{-1}\ s^{-1}$ in MoS_2,[100] approaching ideal phonon-limited mobility. However, using high-k dielectrics will limit the room-temperature mobility due to SO phonon scattering in polar dielectrics.[99,113] Dielectric screening using PMMA as a dielectric was reported to also provide a screening medium, but structural degradation and variations in PMMA properties are significant factors and may prevent further utilization of PMMA as a dielectric for 2D materials.[101]

Structural defects, contaminants and atomic vacancies in TMDCs can also induce significant CI scattering. Fixing or reducing such defects significantly improves the FET mobility and SS, which calls for the growth of high quality TMDC samples.[98,99,109,112–115] Moreover, charge traps in TMDCs can cause an unnecessary sink for charges, which reduces the field-effect mobility, and can cause Fermi-level pinning at the metal contact/TMDC interface.[99,113–119] Additionally, charge traps can

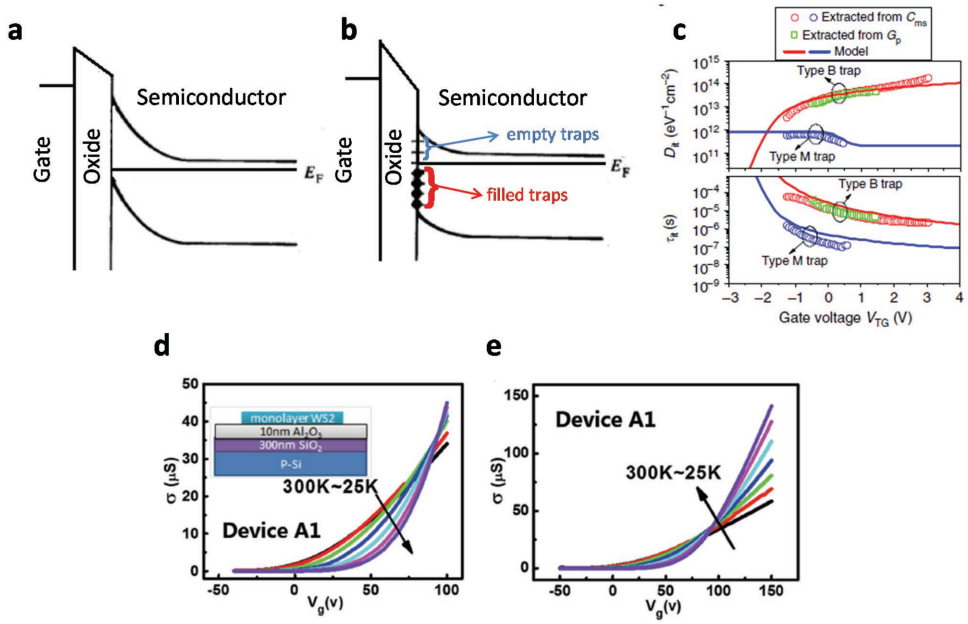

Figure 6. Charge-trap effects in 2D FETs. a, b) A gate-oxide-semiconductor band diagram of an ideal case of an interfacial-trap-free semiconductor, and a case showing interfacial traps at the oxide–semiconductor interface, respectively. It can be seen that in case (a) the gate voltage drop is divided between the oxide capacitance and the semiconductor capacitance causing large band bending in the semiconductor. Comparatively, case (b) shows less band bending in the semiconductor due to the fact that the gate voltage is partially dropped to charge the trap states. c) Trap state density (D_{it}) and time constant (τ_{it}) vs. top gate voltage (V_{TG}) of a monolayer MoS_2 FET. Reproduced with permission.[116] Copyright 2014, Nature Publishing Group. d, e) Conductance (σ) vs. gate voltage (V_g) of a WS_2 FET before and after thiol functionalization, respectively. Reproduced with permission.[99] Copyright 2015, Wiley-VCH.

cause a deviation from the ideal SS (≈60 mV dec^{-1} at 300 K) due to the addition of an interface trap capacitance that is directly related to the interface trap density.[113] **Figure 6**a and b shows an energy-band diagram of a metal-oxide semiconductor (MOS) in the cases of no interfacial traps (a) and the case of existing interfacial traps (b). It can be observed that the band bending, for the same applied gate voltage, in the ideal case (Figure 6a) is more than the case of interfacial traps (Figure 6b). This is due to the finite voltage drop across the interface trap capacitance which traps and de-traps charges in the interface trap states. Zhu et al. experimentally confirmed two types of charge traps in MoS_2, with the charge traps at the band edge being more prominent (i.e., higher density) than mid-gap traps.[116] It can be seen that the trap state density (D_{it}) for states close to the band edge is more than an order of magnitude higher than mid-gap traps (Figure 6c). This phenomenon is what causes the Fermi-level pinning close to the conduction band of metal contacts in MoS_2 FETs. Moreover, Qiu et al. observed that localized trap states in MoS_2 produce a hopping transport current that is dominant at low carrier densities, which explains the deviation from the band-like transport expected in ideal MoS_2 FETs.[117]

Reducing charge-trap densities can cause a transition from an insulating behavior to a metallic behavior evident by the increase of field-effect mobility and variable temperature behavior.[99,114] In MoS_2 and WS_2, trap states can be caused by sulfur vacancies, interfacial traps, and extrinsic contamination. Several methods to reduce or heal vacancies and defects in TMDCs have been reported. Wang et al. reported a technique of using thiol functionalization to reduce the number of sulfur vacancies and accordingly reduce the CI and trap densities, which can help achieve a room-temperature back-gated monolayer MoS_2 and WS_2 mobilities of 81 and 83 cm^2 V^{-1} s^{-1}, respectively.[99,114] Figure 6d and e shows the effect of thiol functionalization on WS_2 FETs. It can be observed that the on-state conductance for the WS_2 FET after thiol functionalization (Figure 6e) is ≈3 times higher than the pristine case, which highlights the effect of reducing charge-trap states in 2D material devices. Additionally, Lu et al. demonstrated oxygen healing of deep traps in WSe_2 using surface laser modification, which led to improvements in the conductivity of WSe_2.[115] Moreover, oxygen plasma cleaning was reported to reduce organic contamination and consequently reduce the charge-trap density in MoS_2.[98] Recently, Javey et al. reported using organic superacids to enhance the photoluminescence quantum yield of MoS_2, which can also be used to reduce trap densities in MoS_2 FETs.[120] On the other hand, similar vacancies and other defects do not produce deep trap states in b-P and they are electronically inactive,[121] which leads to a nearly ideal SS.[122]

For MoS_2 and other TMDCs, in the absence of CI scattering and charge traps, the room-temperature mobility is limited by optical phonon scattering, while the mobility is dominated by acoustic phonon scattering at temperatures <100 K.[109] Another extrinsic factor is the surface optical phonon induced on the interface between 2D materials and dielectrics, which can limit the mobility at room temperatures when the charge impurity density is low and the CI scattering is not dominant at room temperature.[109,113] Nevertheless, the use of a high-*k* top gate can improve the mobility dramatically in the non-ideal

case of CI-limited mobility, by screening the electric field and quenching the characteristic homopolar phonon mode, which is polarized in the out-of-plane direction.[99,100,113]

5. Short-Channel Effects in 2D Semiconductors

Due to the continuous scaling of silicon-based FET devices in the past decades, new effects and physical phenomena have emerged and altered the performance of such devices. As the transistor dimensions and doping densities are scaled, the threshold voltage of such devices does not scale by the same factor, and is further varied significantly due to short-channel effects. Consequently, to maintain proper transistor operation, constant field scaling was not possible with the introduction of SC effects. This fact leads to an increase in the drain electric field for shorter-channel devices compared to longer ones. With this increase in electric fields, SC effects have become common in new-generation devices and circuits. Effects such as drain-induced barrier lowering (DIBL) (**Figure 7**a and b), gate-induced drain leakage (GIDL), band-to-band tunneling (Figure 7c) non-ideal SS due to high depletion capacitances, velocity saturation, threshold voltage variations, punch-through, and device breakdown among other factors have become real concerns due to the undesired drain electric field control over the channel. This effect has led to the utilization of new geometries to enhance the gate control of devices and reduce SC effects. Tri-gate technology[123] and fully depleted silicon-on-insulator (FDSOI) technology[124–126] are some of the geometrical modifications applied to traditional planar devices in order to mitigate SC effects. Silicon-on-insulator technology has proved to have better electrostatics than traditional silicon devices, leading to reduced threshold voltage variability in integrated circuits and reduced DIBL.[124–126]

The electrostatic scaling length (λ) is defined as

$$\lambda = \sqrt{t_s t_{ox} \frac{\varepsilon_s}{\varepsilon_{ox}}} \tag{3}$$

where t_s, t_{ox}, ε_s, and ε_{ox} are the depth of the semiconductor depletion layer, thickness of the gate dielectric oxide layer, dielectric constant of the semiconductor, and the dielectric constant of the gate dielectric oxide, respectively.[116,127] λ is a metric for the distinction between short-channel and long-channel regimes, where no significant SC effects appear. For fully depleted device structures, where the thickness of the semiconductor is smaller than the depletion width, the value of t_s in the previous equation becomes the thickness of the semiconductor body, which yields a much smaller λ. DIBL has an effect of lowering the potential barrier at the source side due to the high electric fields from the drain side (Figure 7b). Due to this lowering of the source barrier, a reduction of the threshold voltage is observed. The change in the threshold voltage is approximately ($\Delta V_t \alpha\ V_{ds}\ e^{-L/\lambda}$), where L is the channel length and V_{ds} is the drain-source voltage. Typically, in order to avoid short channel effects, L should be ≈4–5 times longer than λ.[116] For channel lengths much shorter than λ, significant DIBL, increased hot-carrier injection, reduction in SS due to punch-through, and other SC effects are expected to dominate the device performance. Hence, a reduction of the semiconductor thickness (t_s) will yield a smaller λ and better performance for short-channel devices (Figure 7d). Additionally, punch-through effects can be mitigated in fully depleted device structures. However, for SOI technology the scalability is limited compared

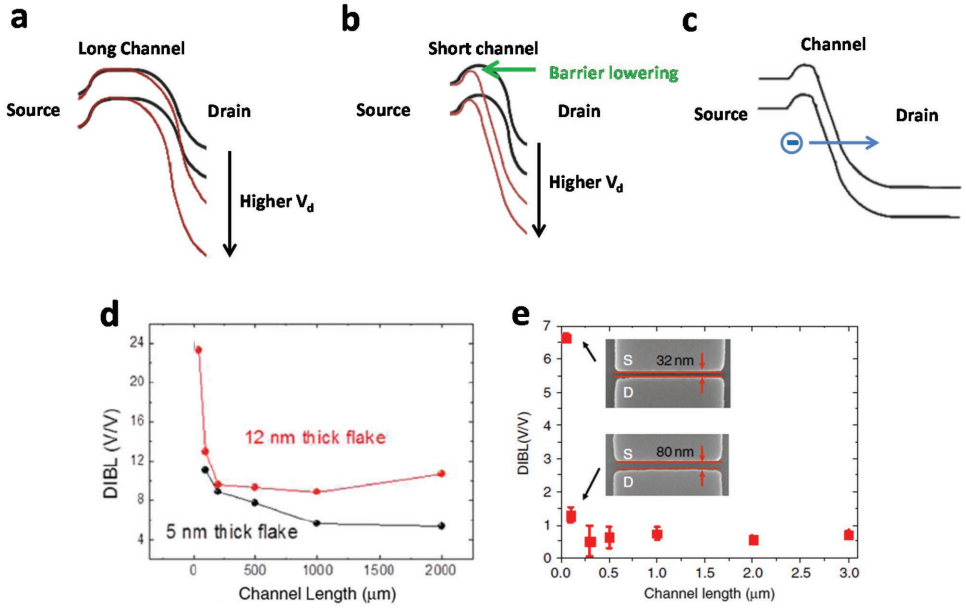

Figure 7. Short-channel effects in MoS_2 FETs. a) Energy-band diagram of a long-channel FET showing no change in the energy barrier in the source side. b) Energy-band diagram of a short-channel FET showing a reduced barrier height at higher drain bias (red) compared to low drain bias (black). c) Energy-band diagram of a FET under large electric field demonstrating the idea of band-to-band tunneling and GIDL (electron tunneling direction is in blue). d) Semiconductor (MoS_2) thickness effect on DIBL. Reproduced with permission.[127] Copyright 2012, American Chemical Society. e) DIBL in monolayer MoS_2 FET with 34–60 nm HfO_2/AlO_x gate dielectric. Reproduced with permission.[116] Copyright 2014, Nature Publishing Group.

to 2D materials due to the thickness limit of ≈5 nm. This thickness limit is due to the manufacturing burden of reducing the ultra-thin body (UTB) silicon and the carrier-energy quantization for ultrathin silicon, which results in a threshold voltage shift, degraded capacitance, reduced inversion charge, and reduced current on/off ratios.[124,128–130] Although a thinner silicon body (2.5 nm) has been demonstrated, the significant mobility degradation of thin films hinders its future technology utilization.[128]

The atomically thin and dangling-bond free structure of 2D materials along with the small dielectric constant of some TMDCs (3.3 for MoS_2), can achieve very small λ values, which can yield negligible SC effects in devices as short as ≈8 nm.[7,131,132] $\mathrm{DIBL} = \left|\frac{V_{\mathrm{th(dd)}} - V_{\mathrm{th(low)}}}{V_{\mathrm{dd}} - V_{\mathrm{low}}}\right|$ is an important SC metric indicating the threshold voltage shift relative to long channels, where $V_{\mathrm{th(dd)}}$, $V_{\mathrm{th(low)}}$, V_{dd}, and V_{low} are the threshold voltage at the applied drain supply voltage, threshold voltage at a low drain voltage, the supply drain voltage, and the low drain voltage value, respectively. Theoretically speaking, compared to UTB silicon, MoS_2 shows 52% smaller DIBL than a 3-nm-thick silicon UTB technology at 10-nm channel length.[132] DIBL of 10 mV V^{-1} and 100 mV V^{-1} were predicted for 15-nm and 8-nm MoS_2 FETs, respectively. Experimental measurements extrapolated to a MoS_2 FET with 3-nm HfO_2 predicted no significant DIBL down to a channel length of ≈7 nm (Figure 7e).[116,127,131,132] Additionally, Javey et al. experimentally demonstrated a MoS_2 FET with a 1-nm physical channel showing DIBL of 290 mV V^{-1}, which could theoretically go down to ≈30 mV V^{-1} with a 2-nm ZrO_2 gate dielectric.[133] These comparisons and facts highlight the potential for using TMDCs or other 2D materials in future sub-10-nm technologies. Other 2D materials such as b-P are also expected to be promising materials with SC effect immunity. For instance, bilayer b-P is expected to experience negligible DIBL and nearly ideal SS for devices down to ≈8 nm. It is also predicted that b-P at 9-nm channel length will have a higher current ON/OFF ratio than MoS_2 and WSe_2.[134] Nevertheless, due to the instability of b-P,[135] only multilayer b-P has been used for experimental device study, which affects the scaling limit of b-P based devices. Miao et al. demonstrated a 20-nm-channel-length b-P FET with a current ON/OFF ratio of ≈100, which is significantly smaller than the long-channel current ON/OFF ratio of ≈10^4.[136] This large drop in the current ON/OFF ratio may be overcome by using thinner b-P flakes, but further improvements on the processing of b-P to reduce sample degradation must be taken into account.

Velocity saturation is caused by scattering of high-energy electrons with the optical phonons of a material or the SO phonons. Velocity saturation causes a reduction in the operating current of the material, which is more prominent in short-channel devices due to the large electric fields.[127,136–138] Accordingly, larger optical phonon energies and saturation velocities are desirable. In MoS_2, the saturation velocity of 3×10^6 cm s^{-1} and contact resistance can reduce the field-effect mobility by ≈50% when reducing the channel length from 2000 nm to 50 nm.[127,138] In b-P FETs, the reduction of the channel length accompanied by velocity saturation substantially degraded the field-effect mobility (≈20 cm^2 V^{-1} s^{-1}) from the long-channel regime mobility (≈200 cm^2 V^{-1} s^{-1}).[136,137] Accordingly, operating the transistor in the ballistic regime is an important route for future 2D-material FETs. For example, a double-gated MoS_2 FET with a channel length of 8 nm is expected to have a current on/off ratio ≈10^4 due to the large effective mass of MoS_2 which reduces direct source-to-drain tunneling.[132] Although the large effective mass of MoS_2 is a reason for the small mobility, this large mass makes MoS_2 transistors more attractive when operated in the ballistic regime (i.e., channel length <10 nm). It has been shown that a 1-nm MoS_2 device will have up to 2 orders of magnitude lower direct source-to-drain tunneling than silicon.[133] Moreover, for 2D materials in the ballistic regime, the transistor on-current is directly proportional to the density of states, which is proportional to the effective mass, giving an advantage over small effective mass materials.[7]

Another SC effect is GIDL, which limits the off current in transistors due to band-to-band tunneling (Figure 7c) in proximity to the drain, which reduces the current on/off ratio of a transistor. It has been reported that GIDL in MoS_2 is significantly less than in silicon because of the large bandgap and electron mass which reduces the band-to-band tunneling.[131] Further systematic studies of GIDL in 2D materials are yet to be undertaken.

Small bandgap majority carrier transistors (i.e., Schottky contacted FETs) can experience drain-Induced-characteristic switching (DICS), which was reported by Du et al. in few-layer b-P transistors. This effect allows more pronounced ambipolar transport in shorter channels due to the small bandgap and the drain electric fields reducing the Schottky barrier width on the source side, which facilitates carrier tunneling from the contact to the channel.[137] This effect is an issue that has to be addressed, especially for small bandgap materials, because it degrades the current ON/OFF ratio and increases SS.

Finally, the breakdown voltage of transistors due to larger electric fields in scaled devices, which causes avalanche breakdowns and other effects, has been reported to be much larger in MoS_2 (≈30 V μm^{-1}) than in SOI technology with 100-nm thickness.[116] This is important for the long-term stability of FETs and circuits based on 2D materials. More reliability tests to compare transistor lifetimes of 2D materials with silicon will be important to the progress of this field.

6. Summary and Perspective

In this review, we highlighted recent major achievements in the controlled growth and electronic applications of 2D semiconductors with a focus on TMDCs including MoS_2 and WSe_2. We summarized state-of-the-art metrologies scientists have developed toward growth of large crystals and continuous films of TMDCs. Regarding electronic applications of TMDCs, we focused on three major aspects: contact engineering, charge scattering mechanisms, and short-channel effects. We reviewed current approaches to reduce contact resistances and Schottky barrier heights in 2D-semiconductor transistors. The scattering mechanisms of charge carriers in 2D transistors have been discussed, as a deep understanding of the scattering of charges in 2D semiconductors would help to improve device performance.

Lastly, we discussed short-channel effects in 2D semiconductor devices, as short-channel transistors are a direction where atomically thin 2D semiconductors may surpass traditional bulk silicon and III–V semiconductors.

In the past five years, there have been great successes in materials fabrication and electronic applications of 2D semiconductors. Meanwhile, this field is still in its early age with several major challenges ahead. We envision that the following directions need to devote more efforts to further push the science and technology of 2D semiconductors and electronics.

6.1. Controlled Growth of 2D Semiconductors

Compared to graphene, the growth of 2D semiconductors is far less mature. First, the sizes of single crystalline MoS_2 and WSe_2 domains we can grow now (at approximately the hundreds of μm level) is far smaller than the sizes of single crystalline graphene domains (inch level). As grain boundaries have a detrimental effect on the electronic applications of 2D materials, it is highly desirable to grow 2D domains with large domain size and as few grain boundaries as possible. Second, researchers can grow and manufacture continuously and electrical conductive polycrystalline graphene films with sizes as large as meter levels. As a comparison, continuous and uniform MoS_2 and WSe_2 thin layers can only be grown at inch level. The capability to fabricate large 2D semiconductor films with large area uniformity is another important direction. Third, the growth mechanism of TMDC is far less understood than that of graphene growth. For example, what are the active species during TMDC growth? What is the function of substrates and how do TMDC nucleate? A deep understanding of these questions will definitely be beneficial to 2D semiconductor growth. Fourth, currently there are many defects in gas-phase-grown TMDCs, for example, chalcogen atom vacancies. Therefore, how to reduce defect density or heal the defects, either before or after their growth, is another important direction worth studying. The exploration and use of some catalytic active substrates (instead of inactive Si/SiO_2 substrates used in most of current research) may help to decrease defect density and obtain high-quality TMDC samples. Fifth, TMDC growth can leverage the lessons learned from the growth of graphene. For example, the use of all-gas-phase precursors during TMDC growth, as in the graphene growth case, has led to the growth of wafer-scale uniform TMDC films via a MOCVD approach. This achievement benefited from the fact that gas-phase precursors can be introduced into the CVD furnace at constant concentrations during the TMDC growth period, which is impossible when using solid precursors as shown in most other TMDC-growth publications. In addition to the growth of Mo- and W-based TMDCs, the direct growth of monolayer or few-layers of other TMDCs such as those based on Pt,[35,36] which show high theoretical and experimental charge mobilities, is an important direction to pursuit.

6.2. Forming Better Electrical Contacts

As we discussed in the main text, electrical contact is a very important aspect, yet a challenging direction in 2D-semiconductor electronics. Several efficient methods have been developed aiming to achieve low-resistance ohmic contact in 2D electronics. However, many of these methods are based on mechanically exfoliated samples and rely on multiple transfer techniques; for example, graphene based contact, inserting an insulating tunnel layer between 2D semiconductors and metal electrodes, etc. Such sophisticated processes are time consuming and difficult to scale up. Therefore, developing a direct-growth approach that can prepare such device configurations is important for practical applications of 2D electronics. In addition, several methods such as chemical doping and 1T/2H phase engineered contacts, despite the fact that these methods result in good device performance, are not stable in ambient conditions. Therefore, developing methods to encapsulate devices to make them stable over the long term is another important issue that needs to be undertaken.

6.3. Reducing Scattering and Increasing the Mobility

The gap between the theoretical mobility and the experimental mobility in most 2D materials, except for graphene, is still large. This is for numerous reasons, including various scattering mechanisms and structural defects. Interfacial scattering due to CI is one major problem that is yet to be completely solved. As mentioned previously, the atomic thicknesses of 2D materials make the effect of scattering centers detrimental to the charge transport in 2D FETs. First, a contamination-free interface between the 2D material/supporting substrate, and the 2D material/gate dielectric has to be formed. Second, the interface has to be atomically smooth and free of dangling bonds because they can cause additional scattering in the 2D channels. Such an interface can be achieved by employing a transfer-free 2D dielectric (e.g., h-BN) as a supporting substrate and a top-gate dielectric. In order to achieve this feature, significant progress in growing h-BN and other 2D dielectrics has to be made. Issues such as uniformity, layer control, and growing different 2D materials on top of each other in a highly controllable and reproducible manner have to be thoroughly investigated. Additionally, the exploration of new 2D dielectrics with varying properties (i.e., dielectric constant and optical phonon energy) is important for utilization in different 2D-electronic applications. Another major issue is the adoption of a fabrication technique that maintains the pristine quality of 2D materials, and prevents various chemicals and fabrication processes from contaminating the 2D channels. This process can be done by continuously passivating the 2D material during various processing steps, so that pattern transfer and exposure to polymers and photoresists happens only on the passivation material, without affecting the underlying 2D material.

6.4. Achieving High-Performance Ultrashort-Channel 2D FETs

2D semiconductors possess ideal properties (e.g., atomic thicknesses, small dielectric constants) that allow them to achieve highly scaled devices. Nevertheless, several issues have to be considered and solved in order to achieve high-performance short-channel devices. The large contact resistance in

2D-semiconductor devices causes a major hurdle in achieving high current ON/OFF ratios and large ON-state currents in short channel devices. As we mentioned previously, this is due to the higher ratio of resistance contribution that the contact has compared to the channel as the channel gets shorter. Accordingly, techniques mentioned previously in this publication must be evaluated in order to achieve low contact resistivity. Moreover, suppression of various phenomena causing subthreshold leakage, which lowers the current ON/OFF ratio and increases SS, must be undertaken. These phenomena are mainly band-to-band tunneling and DICS. Band-to-band tunneling in 2D materials can be caused by trap-assisted tunneling, which can be significantly reduced by removing contaminants, defects, and interfacial dangling bonds. Using techniques mentioned in our recommendations to reduce scattering can be particularly useful to reduce trap-assisted tunneling. In the case of DICS, larger-bandgap materials can be used in cases where large current ON/OFF ratios are needed (e.g., digital electronics). In situations where velocity saturation is detrimental to the device performance, moving towards ballistic-transport-based devices is a fundamental solution to allow high-performance scaled devices. This can be done by reducing the channel length, and reducing scattering effects in order to reach the ideal mean free path of a material. Alternatively, using 2D semiconductors with large optical phonon energies will reduce the unwanted effects of velocity saturation.

Acknowledgements

B.L. and A.A. contributed equally to this work. This work was supported by the 1000-Talent Program of China, Tsinghua-Berkeley Shenzhen Institute (TBSI), the Development and Reform Commission of Shenzhen Municipality, and the US Air Force Office of Scientific Research (AFOSR)

Conflict of Interest

The authors declare no conflict of interest.

Keywords

black phosphorus, electronics, nanotechnology, TMDC, two-dimensional materials

Received: February 2, 2017
Revised: February 26, 2017
Published online:

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