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ARTICLE

Imperceptible and Ultraflexible p-Type Transistors and Macroelectronics Based on Carbon Nanotubes

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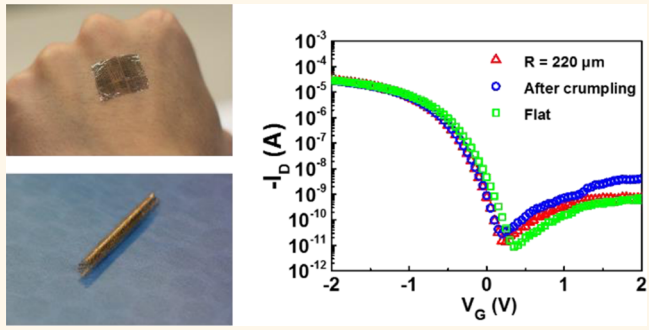
Supporting Information

ABSTRACT: **Flexible thin-film transistors based on semiconducting single-wall carbon nanotubes are promising for flexible digital circuits, artificial skins, radio frequency devices, active-matrix-based displays, and sensors due to the outstanding electrical properties and intrinsic mechanical strength of carbon nanotubes. Nevertheless, previous research effort only led to nanotube thin-film transistors with the smallest bending radius down to 1 mm. In this paper, we have realized the full potential of carbon nanotubes by making ultraflexible and imperceptible p-type transistors and circuits with a bending radius down to 40 μm. In addition, the resulted transistors show mobility up to 12.04 cm^2 V^{-1} s^{-1}, high on−off ratio (~10^6), ultralight weight (<3 g/m^2), and good mechanical robustness (accommodating severe crumpling and 67% compressive strain). Furthermore, the nanotube circuits can operate properly with 33% compressive strain. On the basis of the aforementioned features, our ultraflexible p-type nanotube transistors and circuits have great potential to work as indispensable components for ultraflexible complementary electronics.**



KEYWORDS: *carbon nanotubes, ultraflexible and imperceptible transistors, thin-film transistors, circuits, complementary electronics*

Single-wall carbon nanotubes (SWNTs) are an ideal channel material of thin-film transistors (TFTs) for flexible macroelectronics,[1−5] displays, and sensors.[6−8] Compared with traditional channel materials such as amorphous silicon and polysilicon, carbon nanotubes show excellent mechanical flexibility[9−15] and can be solution-deposited[10,11] or printed[16,17] onto flexible substrates at room temperature, enabling low-cost fabrication of large-area flexible electronics.[5,9] Besides, the outstanding intrinsic electrical properties of semiconducting SWNTs exhibit considerable advantages over organic materials for TFTs in terms of mobility, on−off ratio, and stability against moisture and oxygen.[5,9,10,18−20] Hence, intensive research efforts have been devoted to flexible SWNT TFTs for applications in digital circuits, active-matrix-based displays, and sensors.[1,21−25] TFTs, with SWNT networks as channel and thin films of metals as source, drain, and gate electrodes, have been experimentally demonstrated with relatively high mechanical flexibility and stability.[1,10] In order to improve the bendability of SWNT TFTs, researchers previously focused on optimizing dielectrics of TFTs, trying to find those that can sustain large tensile strains. Elastomeric dielectrics were proposed by Q. Cao *et al.*, and the flexible SWNT TFTs can be bent to a radius of curvature as small as 3.3 mm.[26] Importantly, C. Wang used atomic layer deposition and e-beam evaporation to deposit Al_2O_3 and SiO_2 as the dielectric layer and fabricated high-performance flexible SWNT integrated circuits with a minimal bending radius of ~1.27 mm.[10] Employing poly(vinyl alcohol) as the dielectric layer, S. Aikawa *et al.* pushed the bending radius down to 1 mm.[27] Overall, failure of the fragile dielectric layer remains as the obstacle limiting the flexibility of SWNT TFTs and circuits.

Recently, a new class of "imperceptible" or "epidermal" electronics has emerged.[28−32] Using ultrathin flexible substrates, the imperceptible electronics would be at low strain level at extremely small bending radius according to the calculations in the literature.[33,34] Based on this concept, ultraflexible organic electronics have been demonstrated for various applications.[29,30,33,35,36] However, the ultraflexible organic transistors show low mobility (~1 to 3 cm^2 V^{-1} s^{-1})[29,33] and might suffer from poor long-term stability in air. Although the reported indium−gallium−zinc oxide (IGZO) transistors exhibited high mobility (~26 cm^2 V^{-1} s^{-1}),[34] they

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are n-type and cannot be converted to p-type. However, modern electronics usually require complementary circuits, which would combine both n-type and p-type transistors to realize ultralow static power dissipation and reliable operation with large noise margin. As a result, the development of high-performance ultraflexible p-type transistors is highly desirable to realize ultraflexible complementary circuits.

Here we report imperceptible and ultraflexible p-type SWNT TFTs and circuits fabricated directly on 1.4 μm poly(ethylene terephthalate) (PET) film. The resulting SWNT TFTs exhibit excellent electrical performance with field-effect mobility up to 12.04 $cm^2 V^{-1} s^{-1}$ and an on−off ratio of $\sim 10^6$. Moreover, the ultralightweight SWNT electronics (3 g/m^2) show unprecedented mechanical flexibility compared with previously reported flexible SWNT electronics. Our fabricated TFTs showed little performance degradation when bent at a radius of curvature of ∼40 μm, crumpled like a piece of paper, or even under 67% compressive strain. The as-fabricated inverters, NAND gates, and NOR gates maintained their electrical performance and functionalities even when 33% compressive strain was introduced to form tiny microwrinkles on the electronic foil. The aforementioned good electrical performance, excellent flexibility, and unique lightweight property endow the SWNT-based ultraflexible electronics with a promising future for next-generation wearable electronics, flexible displays, sensing systems, and digital electronics.

RESULTS AND DISCUSSION

Figure 1a illustrates our proposed scheme for fabricating flexible SWNT macroelectronics on ultrathin PET substrates. First, a Si/SiO_2 substrate was spin-coated with polydimethylsiloxane (PDMS) as a reusable supporting substrate for easy handling. Second, an ultrathin PET film with a thickness of 1.4 μm, as the substrate for SWNT TFTs and circuits, was laminated onto the supporting substrate for the following fabrication. After that, microfabrication was carried out to produce SWNT TFTs and circuits with successive gate electrode patterning, gate dielectric deposition, SWNT deposition, and formation of source and drain electrodes and interconnects. A detailed fabrication process for SWNT TFTs and circuits is described in the Methods section. Finally, the as-made electronic foil was peeled off from the supporting substrate for further electrical characterization. Figure 1b shows a zoom-in schematic diagram of SWNT TFTs and circuits on the fabricated electronic foil. The inset of Figure 1b shows a scanning electron microscope (SEM) image of a typical carbon nanotube thin film that we use to make SWNT TFTs. Figure 1c shows a photograph of an as-fabricated electronic foil with a size of 3 cm × 4 cm. Significantly, the proposed scheme is compatible with a standard semiconductor manufacturing process, which enables accurate alignment to realize the complicated configuration of circuits and scalable manufacturing at relatively low cost.

Besides compatibility with the standard semiconductor manufacturing process, our fabricated SWNT TFTs and circuits are ultraflexible, extremely bendable, imperceptible, ultrathin (∼1.4 μm), and ultralightweight (3 g/m^2). Figure 1d shows the fabricated SWNT electronic foil laminated onto human skin, and the human subject reported that the foil was essentially imperceptible because of the ultralight weight and conformal lamination due to the ultraflexibility. The photograph in Figure 1e shows the SWNT electronic foil rolled up with a radius of curvature of ∼1 mm, and Figure 1f shows the SEM image of the

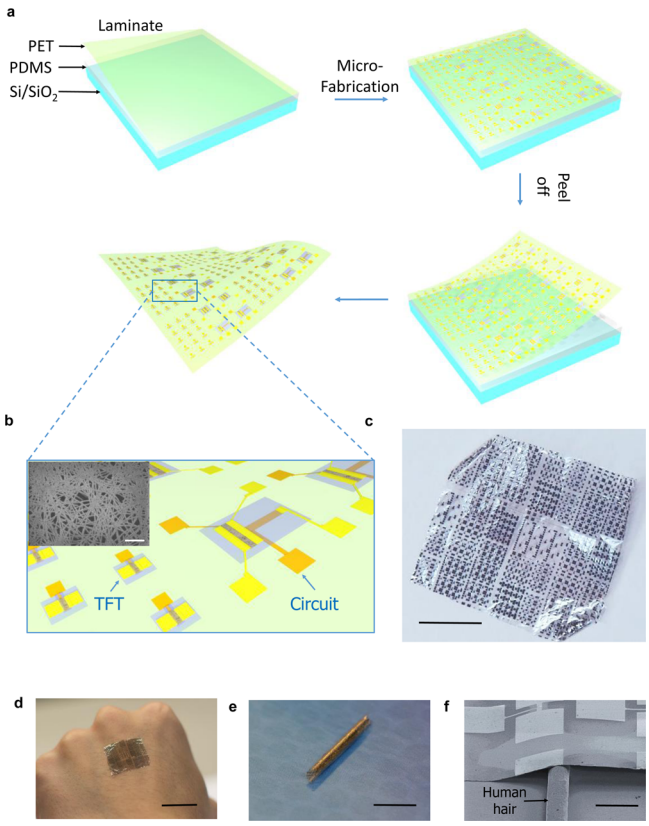

Figure 1. Imperceptible carbon nanotube macroelectronics. (a) Schematic diagrams showing fabrication procedure of carbon nanotube electronic foil. (b) Zoom-in schematic diagram of fabricated electronic foil, showing TFTs and circuits. Inset is a SEM image of a typical SWNT thin film. Scale bar is 500 nm. (c) Photograph of as-fabricated imperceptible nanotube macroelectronics. Scale bar is 1 cm. (d, e) Ultrathin carbon nanotube electronic foil laminated onto human skin (d) and in a rolled-up state (e). Scale bar: 2 cm in (d) and 1 cm in (e). (f) SEM image of the ultrathin SWNT electronic foil laminated onto human hair sitting on a substrate. Scale bar is 150 μm.

SWNT electronic foil laminated onto human hair sitting on a substrate, indicating the extreme bendability and minimal thickness of the nanotube electronics. We believe that ultralightweight, flexible, and imperceptible SWNT electronics are highly advantageous in large-area wearable electronics for sensor and display applications.

We first characterized the direct current (DC) performance of the as-fabricated SWNT TFTs on ultrathin substrates. Figure 2a shows the schematic diagram of an SWNT TFT on a 1.4 μm PET substrate. The SWNT TFT was controlled by an individual back-gate with Al_2O_3/SiO_2 (20 nm/5 nm) stacked in series as the gate dielectric. The purpose of the SiO_2 dielectric layer was to facilitate the deposition of ultrahigh semiconducting purity SWNT networks onto the gate dielectric. A 50 nm palladium (Pd) layer, together with 1 nm titanium (Ti) as an adhesion-promotion layer, was used as the metal for the source, drain, and gate electrodes. More details can be found in the Methods section. Figure 2b−d delineates the DC performance of a representative SWNT TFT with a channel length (L) of 10 μm and a channel width (W) of 100 μm. The SWNT TFT exhibited p-type transistor behavior with hysteresis that is typical for SWNT transistors (Figure 2b). With a drain-to-source bias (V_{DS}) of −1 V, the on-current was

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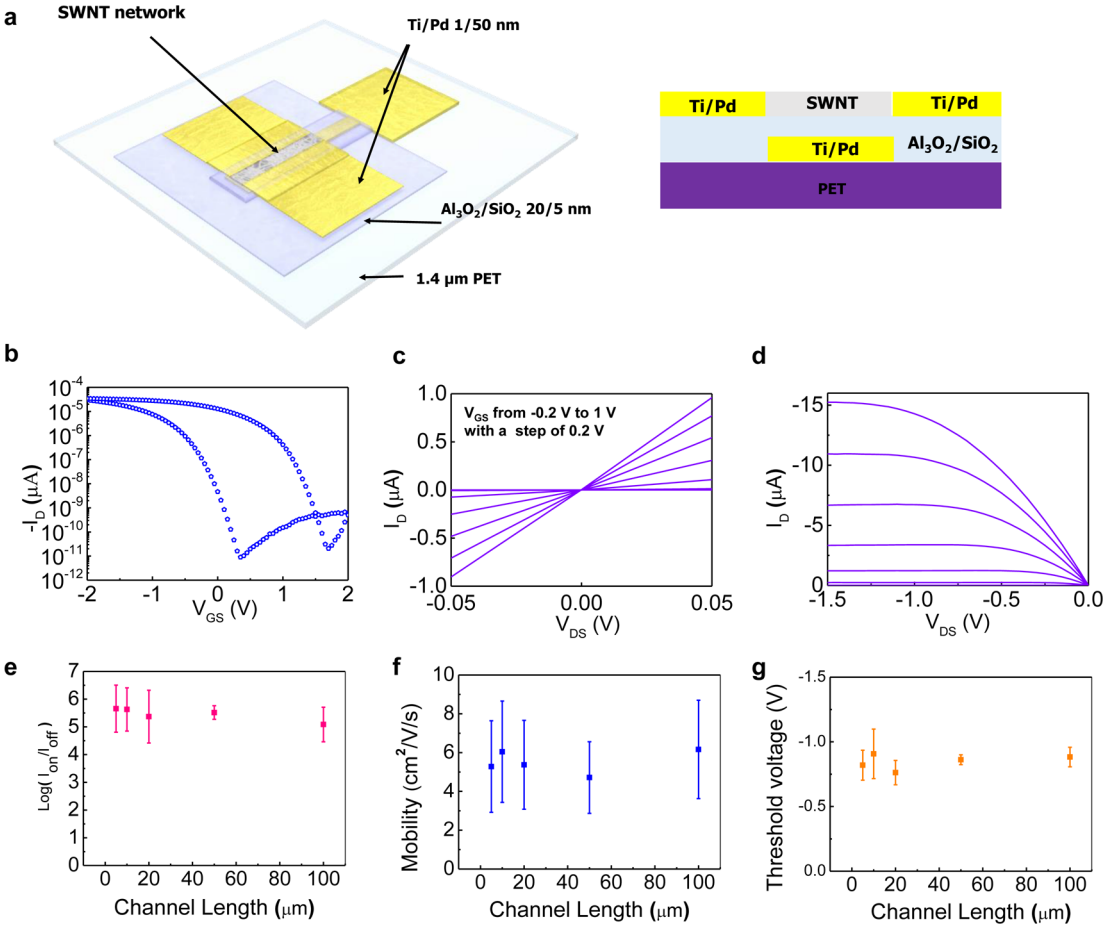

Figure 2. Electrical characterization of carbon nanotube thin-film transistors on 1.4 μm PET foil. (a) Schematic diagram showing device configuration of a SWNT TFT with individual back-gate on 1.4 μm PET substrate. (b) Transfer characteristics of a representative TFT with L = 10 μm and W = 100 μm under V_{DS} = −1 V. (c, d) Corresponding output characteristics in triode regime (c) and saturation regime (d), respectively. V_{GS} is from −0.2 to 1 V with a step of 0.2 V, corresponding to curves from top to bottom. (e, f, g) Statistical study of 50 nanotube TFTs showing on−off ratio (e), field-effect mobility (f), and threshold voltage (g) as functions of channel length.

−30 μA at a gate-to-source bias (V_{GS}) of −2 V, while the off-current of the TFT was −9 pA at V_{GS} = 0.35 V, indicating a high on−off ratio of 10^6. The field-effect mobility of the TFT is extracted to be 12.04 cm^2 V^{-1} s^{-1} using the formula $\mu = (L/W)[1/(CV_{DS})](dI_D/dV_{Gs})$, where I_D is the drain-to-source current, and C is the gate capacitance, estimated with the parallel plate model. The I_D−V_{DS} curves at different gate bias (Figure 2c) show excellent linear behavior, indicating good ohmic contacts between source/drain electrodes and SWNT networks. Output characteristics of the same SWNT TFT are shown in Figure 2d, and excellent current saturation behavior can be clearly observed. The mobility of our p-type ultraflexible SWNT TFTs is much higher than the mobility of other reported p-type ultraflexible organic TFTs (~1 to 3 cm^2 V^{-1} s^{-1} for the best devices)[29,33] and is comparable with the values reported for ultraflexible n-type IGZO TFTs (~26 cm^2 V^{-1} s^{-1} for the best device).[34] In order to evaluate the uniformity of the device performance, we also carried out a statistical study of 50 fabricated SWNT TFTs with various channel lengths, and the results are shown in Figure 2e−g. Our fabricated SWNT TFTs have an on−off ratio centered between 10^5 and 10^6, average mobility centered between 5 and 8 cm^2 V^{-1} s^{-1}, and threshold voltage centered between −0.5 and −1 V. Overall, the uniformity of our fabricated SWNT TFTs is very good and ready for practical applications.

In order to characterize the flexibility of the ultrathin SWNT electronic foil, two experiments that consist of extreme bending and crumpling were carried out. In the first test, as shown in the schematic diagram in Figure 3a, we tightly wrapped our fabricated SWNT electronic foil around a cylinder with a radius of curvature of ~220 μm. In this case, a tensile strain of ~0.3% (Supporting Information, S0), parallel to the drain-to-source current direction, was applied to the SWNT TFTs. The electrical performance of the SWNT TFTs under tensile strain was measured in ambient air. In the second test, the same fabricated SWNT electronic foil was severely crumpled and then flattened. Figure 3b shows the SWNT electronic foil severely crumpled from its original size as a 3 cm × 4 cm rectangle, and SEM images of the crumpled electronic foil can be found in the Supporting Information, S1. The electrical performance of the crumpled SWNT TFTs was also characterized in ambient air. Figure 3c compares the transfer characteristics of a representative SWNT TFT with L = 10 μm and W = 100 μm in three conditions: relaxed status, bent with a radius of curvature of ~220 um, and after crumpling. The SWNT TFT exhibited p-type behavior in all three conditions without any discernible change of its on-current. A measurable increase of off-current was observed in the case of the crumpled TFT, while the off-current in the other two cases showed no measurable change. This can be attributed to the increased

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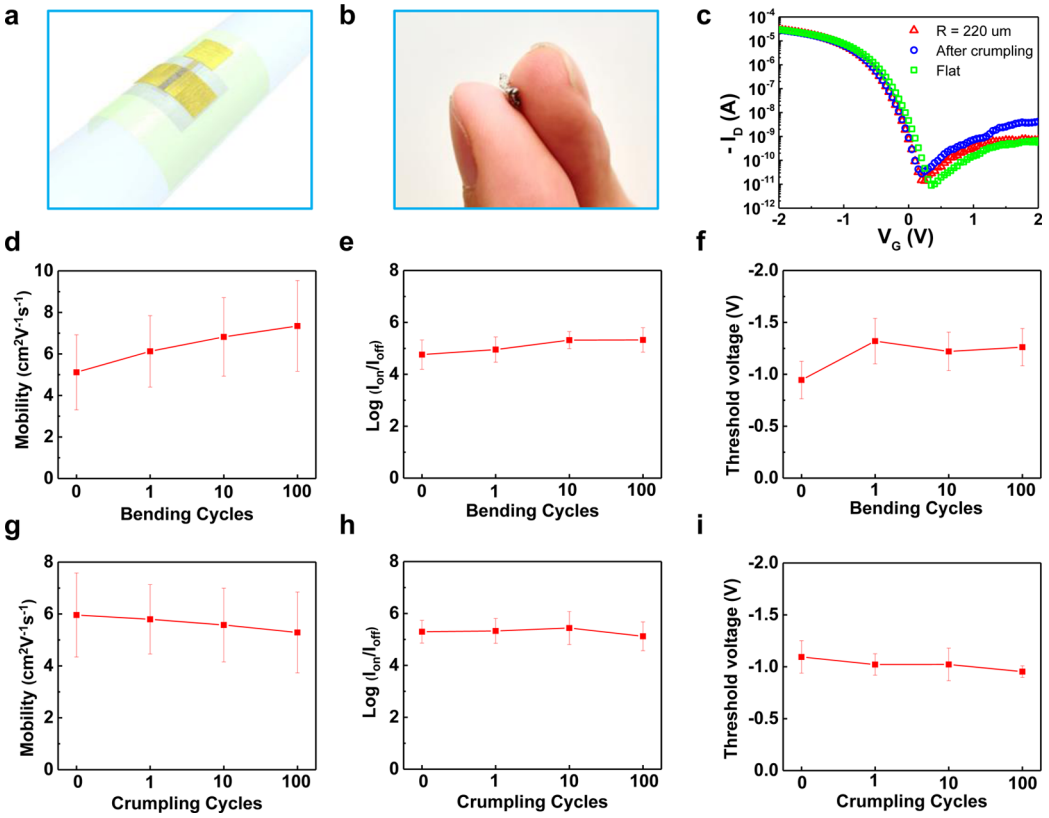

Figure 3. Flexibility of nanotube TFTs on a 1.4 μm PET substrate. (a) Schematic diagram showing the measurement of a TFT wrapping around a cylinder. (b) Crumpled CNT electronic foil (original size: 3 cm × 4 cm rectangle). Scale bar is 1 cm. (c) Transfer characteristics of a representative TFT with L = 10 μm and W = 100 μm under relaxed (flat) state, after crumpling, and bent with a radius of ~220 μm. (d) Mobility, (e) logarithm on−off ratio, and (f) threshold voltage of SWNT TFTs bent with a radius of ~220 μm after different bending cycles. (g) Mobility, (h) logarithm on−off ratio, and (i) threshold voltage of SWNT TFTs after different crumpling cycles.

leakage current through the gate dielectric after the TFT was crumpled (Figure S2a in the Supporting Information, S2). Figure S2a shows that the gate leakage currents of the TFT at bent and relaxed status exhibited no identifiable difference, while the gate leakage current of the crumpled TFT showed an increase by a factor of 10, which confirms our assumption. However, since the off-current for all three conditions was less than 100 pA and significantly smaller than the on-current, the electrical performance of the SWNT TFTs showed no big change (Figure S2b in the Supporting Information, S2). From Figure S2b, the mobility remained between 10 and 12 $cm^2\ V^{-1}\ s^{-1}$, the on−off ratio remained more than 10^6, and the shift of the threshold voltage was less than 0.2 V. As expected, there was no significant change of the electrical performance of the SWNT TFTs when the devices were in different bending conditions. In order to test the reliability of our platform, we further performed bending and crumpling tests with nine SWNT TFTs with 100 cycles of bending and 100 cycles of crumpling for each device. Figure 3d−f plot the mobility, the logarithm on−off ratio, and the threshold voltage of the devices under testing with 0 (before bending), 1, 10, and 100 bending cycles, respectively, and overall the changes in device performance were very small. The mobility changed from 5.12 ± 1.81 $cm^2\ V^{-1}\ s^{-1}$ to 7.35 ± 2.19 $cm^2\ V^{-1}\ s^{-1}$, the logarithm on−off ratio changed from 4.76 ± 0.57 to 5.33 ± 0.47, and the threshold voltage changed from −0.95 ± 0.18 V to −1.26 ± 0.18 V after 100 bending cycles. Figure 3g−i plot the mobility, the logarithm on−off ratio, and the threshold voltage of the devices under testing with 0 (before crumpling), 1, 10, and 100 crumpling cycles, respectively, and the changes in device performance were small as well. The mobility changed from 5.96 ± 1.62 $cm^2\ V^{-1}\ s^{-1}$ to 5.29 ± 1.55 $cm^2\ V^{-1}\ s^{-1}$, the logarithm on−off ratio changed from 5.30 ± 0.44 to 5.12 ± 0.55, and the threshold voltage changed from −1.09 ± 0.16 V to −0.95 ± 0.06 V after 100 crumpling cycles. On the basis of the test results, all nine SWNT TFTs under testing after a total of 200 bending and crumpling cycles still maintained good performance, confirming that our platform is reliable. Two reasons contribute to the ultraflexibility of our fabricated SWNT TFTs. First of all, metal thin films and carbon nanotubes have good intrinsic mechanical flexibility.[37−39] Several groups including our group have reported flexible carbon nanotube electronics.[2,8,10,21] In addition, by decreasing the thickness of the substrate to 1.4 μm, we significantly reduced the tensile strain under similar bending conditions. Therefore, the dielectric layer would survive even at sharp bending or crumpling. In terms of the bending experiments, thanks to the ultrathin PET substrate, the tensile strain applied to the SWNT TFTs was calculated to be ~0.3% (Supporting Information, S0) when the SWNT electronic foil was wrapped tightly around the cylinder with a radius of ~220 μm. The small tensile strain (~0.3%) would not cause significant failure of the dielectric layer, which explained the unchanged electrical performance. In terms of the crumpling experiments, the high yield that we observed (nine devices each surviving 100 cycles of crumpling) suggests that the crumpling did not lead to strain sufficiently high to cause Al_2O_3 dielectric failure due to the ultrathin PET substrate. Our platform of combining carbon

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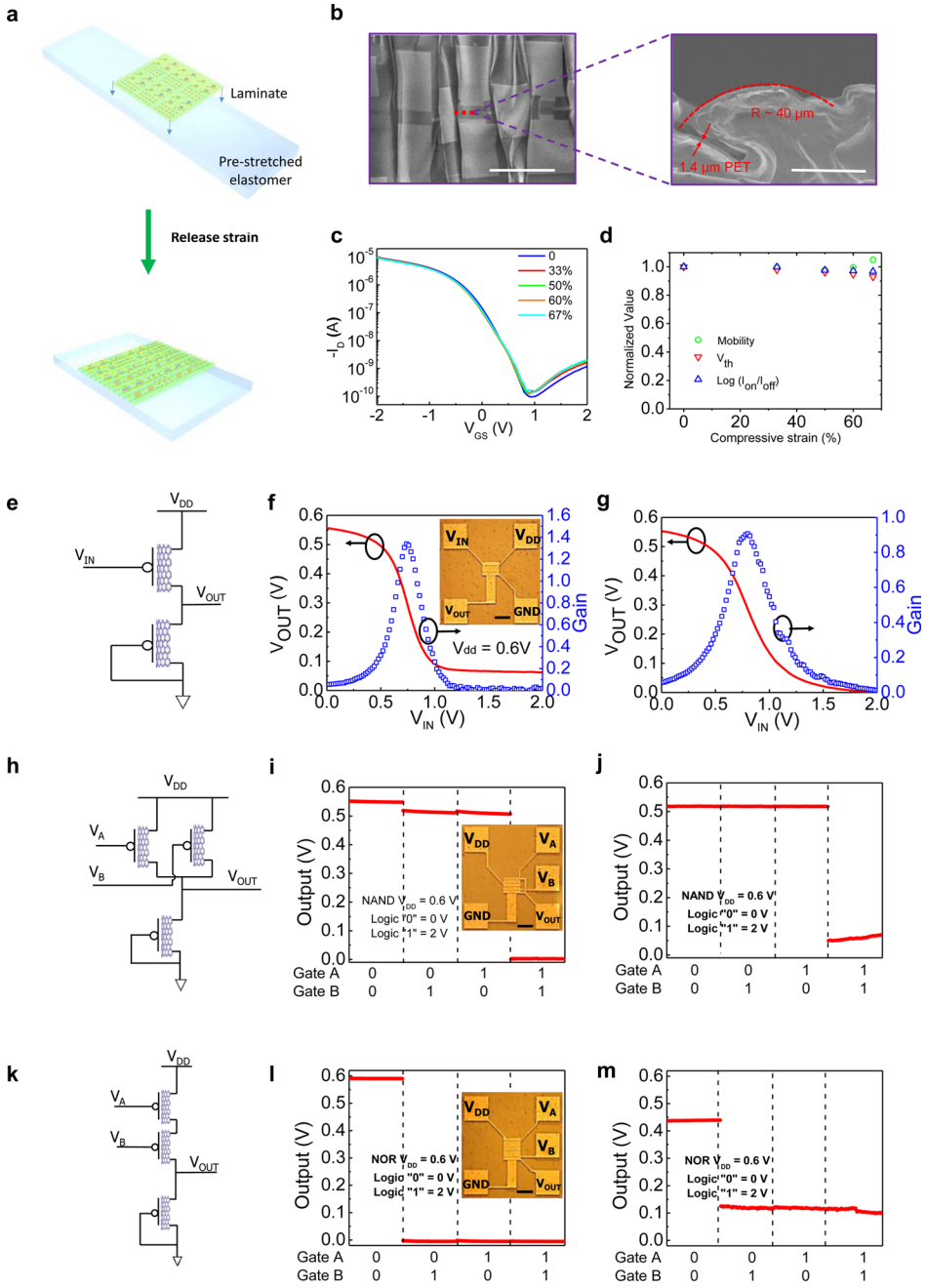

Figure 4. Stretch-induced effect of imperceptible carbon nanotube macroelectronics. (a) Illustration of stretchable carbon nanotube macroelectronics. (b) SEM images of top view and cross-section view of a wrinkled nanotube TFT under 67% compressive strain, showing the bending radius of the active channel region, ~40 μm. (c) Transfer characteristics of the same SWNT TFT under different compressive strains, measured at $V_{DS} = -1$ V. (d) Corresponding normalized values of mobility, threshold voltage, and on−off ratio as functions of compressive strain. (e) Schematic diagram of diode-load inverter. (f, g) Electrical characteristics of an inverter in relaxed state (f) and undergoing 33% compressive strain (g). Inset of (f): Photograph of an inverter in relaxed state. Scale bar is 100 μm. (h) Schematic diagram of diode-load NAND gates. (i, j) Output characteristics of NAND gates in relaxed state (i) and undergoing 33% compressive strain (j). Inset of (i): Photograph of a NAND gate in relaxed state. Scale bar is 100 μm. (k) Schematic diagram of diode-load NOR gates. (l, m) Output characteristics of NOR gates in relaxed state (l) and undergoing 33% compressive strain (m). Inset of (l): Photograph of a NOR gate in relaxed state. Scale bar is 100 μm.

nanotubes with ultrathin substrates greatly improves the flexibility and mechanical stability of carbon nanotube electronics when compared with previously reported flexible SWNT TFTs.[10,26,27]

With the bending test described above, it is usually experimentally challenging to achieve a bending radius below 100 μm. As a result, we adopted a stretch compatibility test to further reduce the radius of curvature for the electrical measurement and characterize the robustness of our platform. Figure 4a illustrates the process for the stretch compatibility and mechanical robustness test. The fabricated SWNT electronic foil with TFTs and circuits was laminated onto a prestretched elastomer (3 M VHB) with desired total strain. Then the prestretched elastomer was slowly released. Over the

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process, wrinkled microstructures of the electronic foil were formed due to the compressive strain applied on the ultrathin PET film. Figure 4b shows the SEM images of SWNT TFTs under 67% compressive strain. The left top-view SEM image clearly shows that out-of-plane wrinkles formed after the strain was transferred from the prestretched elastomer to the SWNT electronic foil. The right cross-section SEM image shows the active channel region of one SWNT TFT with a bending radius of ~40 μm, which would lead to ~1.7% local tensile strain (Supporting Information, S0). We note that the local tensile strain depends on the local bending radius and can be different from the number 67% due to the wrinkles formed on the electronic foil. However, the use of 67% compressive strain is better to clearly describe our experiment. We measured the electrical performance of the SWNT TFT under different compressive strains. Figure 4c shows the transfer characteristics of a representative SWNT TFT with L = 50 μm and W = 100 μm undergoing various compressive strains. There is no apparent degradation of the SWNT TFT even under 67% compressive strain. The small change in the off-current can be attributed to the variations of the gate leakage current under different compressive strains (Figure S3 in the Supporting Information, S3). Figure 4d depicts normalized values of mobility, threshold voltage, and current on−off ratio under various compressive strains for the same device. For various compressive strains up to 67%, the change in mobility is less than 5%, the change in threshold voltage is less than 7%, and the change in logarithmic on/off ratio is less than 4%. While devices with local bending radius down to 40 μm showed good stretch compatibility and mechanical robustness (*e.g.*, Figure 4b−d), we note that finer wrinkles with even smaller bending radius did lead to failure of the devices, and the overall yield of the devices on the stretch-released sample was ~10%.

Besides SWNT TFTs, we also evaluated the stretch compatibility and mechanical robustness of the fabricated SWNT circuits to demonstrate that our platform is also suitable for complex circuits and systems. For proof of this concept, the fabricated basic logic blocks such as inverters, NAND gates, and NOR gates were configured with diode-load since SWNT transistors usually show p-type transistor behavior. To evaluate the flexibility of the circuits, we applied 33% compressive strain to the SWNT electronic foil to form tiny wrinkles (Supporting Information, S4). The wrinkles typically had a bending radius of ~50−60 μm. The fabricated SWNT circuits were tested in ambient air with and without 33% compressive strain, and the results are shown in Figure 4e−m. Figure 4e shows the schematic diagram of diode-load inverters, and Figure 4f,g shows the voltage transfer curves (VTCs) of diode-load inverters with and without compressive strain. The inset of Figure 4f shows a photograph of an SWNT diode-load inverter. Inverters still functioned properly after 33% compressive strain with a slight decrease in the inverter gain. Figure 4h shows the schematic diagram of diode-load NAND gates, and Figure 4i,j shows the output characteristics of diode-load NAND gates before and after 33% compressive strain. The inset of Figure 4i shows a photograph of an SWNT diode-load NAND gate. NAND gates also functioned correctly after a 33% compressive strain with a slight decrease in both output high voltage level (V_{OH}) and output low voltage level (V_{OL}). The schematic diagram of SWNT diode-load NOR gates is shown in Figure 4k, and the inset of Figure 4l shows a photograph of a diode-load NOR gate. SWNT diode-load NOR gates showed similar behaviors to the SWNT diode-load NAND gates (Figure 4l,m). We note that the 67% compressive strain we used for single transistor measurement and 33% compressive strain we used for SWNT circuits are by no means limits of our transistor operation. With further optimization of the transistor/circuit design, we believe that even better performance can be achieved. The above results confirm that, besides fabricated SWNT TFTs, the fabricated SWNT circuits on ultrathin substrates also have outstanding stretch compatibility and mechanical robustness.

CONCLUSION

In conclusion, we have developed a reliable approach for realizing high-performance and ultraflexible SWNT TFTs and circuits on a 1.4 μm PET substrate. The fabricated SWNT electronic foil is ultrathin, is ultralightweight, and exhibits excellent electrical performance and mechanical flexibility due to the properties of carbon nanotubes and the ultrathin substrates, which help to reduce tensile strains. The fabricated SWNT TFTs can be bent with a bending radius down to ~40 μm and even severely crumpled without discernible degradation of their electrical performance. Moreover, the SWNT TFTs can also sustain up to 67% compressive strain without apparent change compared with their performance without any strain. Besides the SWNT TFTs, the SWNT circuits also show good performance with up to 33% compressive strain. Another important advantage of our platform is that it is compatible with the standard semiconductor manufacturing process, which enables large-scale low-cost fabrication of our SWNT electronic foil. Our platform can be further improved by incorporating n-type materials (*e.g.*, IGZO) to achieve complementary circuits that can reduce the circuit power consumption and improve the reliability of circuit operation. On the basis of all the aforementioned advantages, our platform shows great potential for next-generation electronics such as ultraflexible digital electronics, artificial skins, active-matrix-based displays, and sensors.

METHODS

Substrate Preparation. A silicon wafer with 300 nm SiO_2 was used as supporting substrate for easy handling of the 1.4 μm PET film (DuPont Teijin Films, Japan) during device fabrication. After spin-coating PDMS onto the silicon wafer, the sample was baked at 65 °C for 1 h. Then the ultrathin PET film was attached onto the PDMS by van der Waals force.

Device Fabrication. First, 1 nm titanium and 50 nm palladium were deposited by e-beam evaporator as gate electrodes. Second, 20 nm Al_2O_3 was deposited by atomic layer deposition (Savannah atomic layer deposition system) at 90 °C, followed by depositing 5 nm SiO_2 with an e-beam evaporator (CHA Mark 40) to form the stacked dielectric layer for SWNT TFTs and circuits. After that, the substrate was immersed in poly-L-lysine aqueous solution (0.1% w/v (mass concentration), TED PELLA, Inc.) for 8 min to functionalize the surface. After rinsing with DI water, an SWNT solution (IsoSol-S100, #23-081, NanoIntegris Inc.) was dropped onto the substrate and washed away after 40 min of incubation. This step is followed by baking the silicon wafer at 90 °C for 30 min to evaporate the solvent. After depositing SWNT thin-film networks, channels were opened using buffer oxide etchant, and 1 nm titanium and 50 nm palladium were e-beam evaporated as source/drain electrodes and interconnection metals. Last, unwanted SWNTs were removed with oxygen plasma (100 W, 150 mTorr, 80s).

Device Characterization. All electrical characteristics of the fabricated SWNT TFTs and circuits were measured with an Agilent 4156B Precision semiconductor parameter analyzer in ambient

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environment. All the SEM images were taken with a Hitachi S-4800 field emission scanning electron microscope.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b02847.

Tensile strain calculation (S0); scanning electron microscope images of a crumpled electronic foil (S1); gate leakage current and electrical parameters of the representative device under three conditions (S2); gate leakage current for the representative SWNT TFT under different compressive strains (S3); scanning electron microscope images of SWNT circuits with 33% compressive strain (S4) (PDF)

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Author Contributions

§X. Cao and Y. Cao contributed equally to this work.

Notes

The authors declare no competing financial interest.

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