Supporting Information for

High Performance WSe_2 Field-Effect Transistors *via* Controlled Formation of In-Plane Heterojunctions

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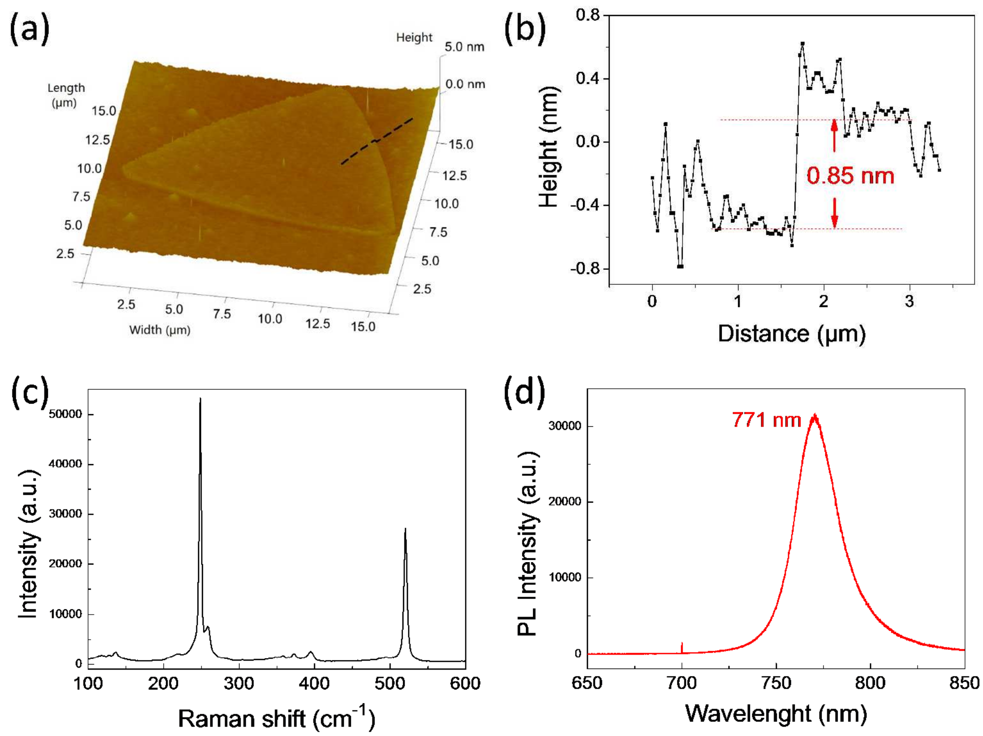
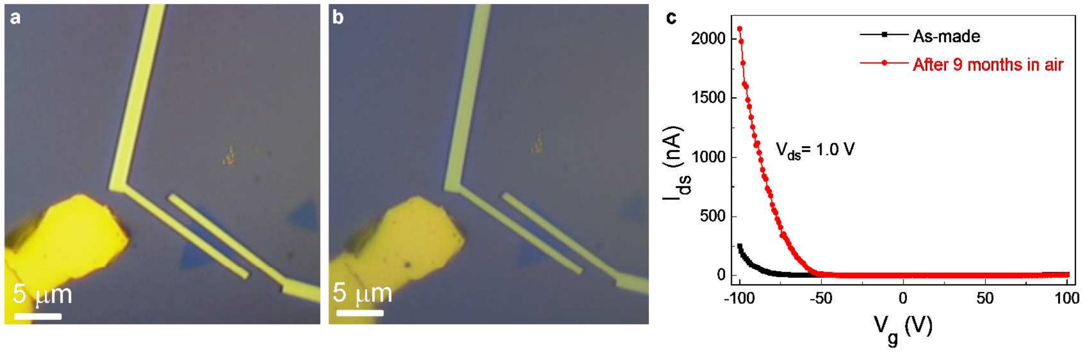
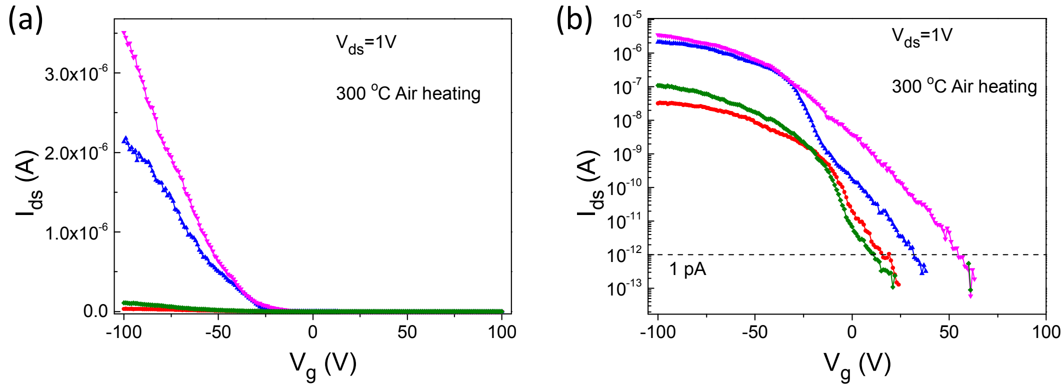


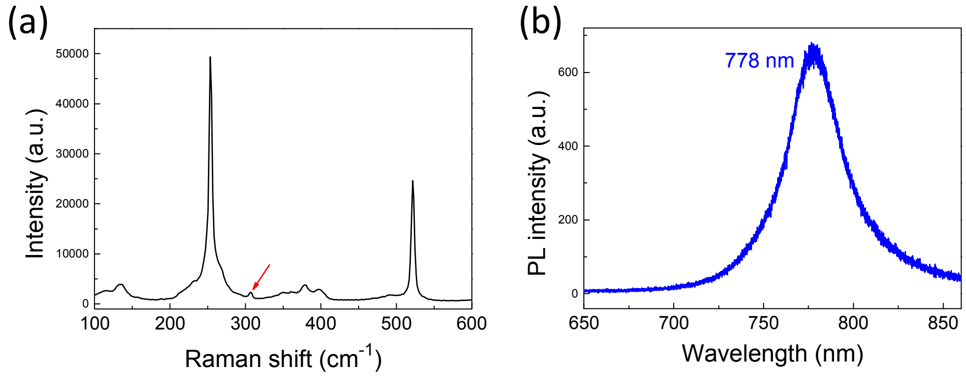
Supplementary Figure S1. Characterization of CVD-grown monolayer WSe_2. (a) An AFM image of a CVD-grown WSe_2 flake. (b) Height profile along the black curve in image a, indicating this flake is a monolayer WSe_2 with a thickness of 0.85 nm. (c), (d) Typical Raman and PL spectra of CVD-grown monolayer WSe_2 flakes. The absence of the peak at ~303 cm^{-1} (which is a fingerprint of few-layer WSe_2) and strong PL intensity indicate the samples are monolayer WSe_2 flakes.



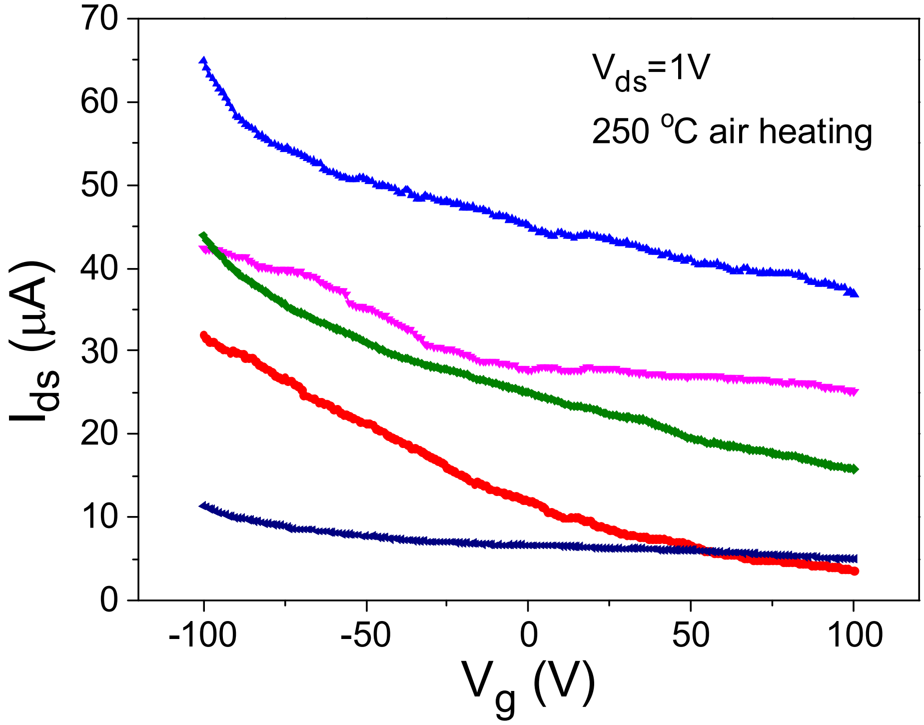
Supplementary Figure S2. Optical microscopy characterization and electrical performance of a monolayer WSe_2 FET. (a), (b) Optical images of an as-fabricated CVD-grown monolayer WSe_2 FET (a) and the same device after leaving in air for 9 months (b). The flakes became less visible in the right image. (c) Comparisons of the transfer characteristics (I_{ds}-V_g curves) of the devices shown in (a) and (b).



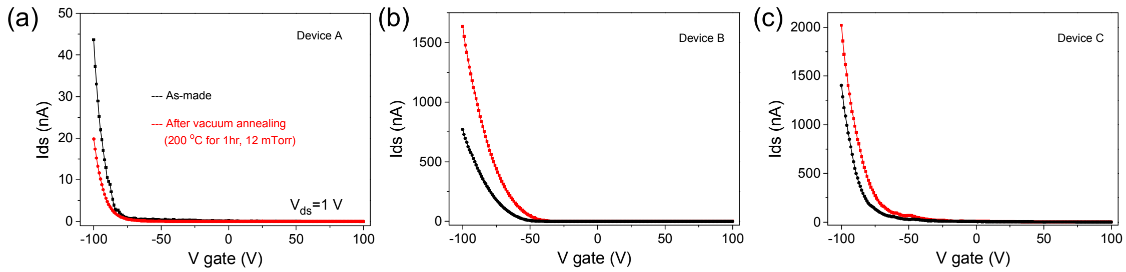
Supplementary Figure S3. I_{ds}-V_{ds} characteristics of monolayer WSe_2 devices after 300 °C treatment. Linear (a) and semi-log (b) scale I_{ds}-V_g curves of CVD-grown monolayer WSe_2 transistors after 300 °C treatments. Different colors indicate different devices. Compared with 250 °C treated devices, the on-state current of all these devices decreased significantly (>10 fold). We noted that the devices still showed high on/off ratios of 10^4-10^7. After further air heating at 400 °C, all devices became open circuits.



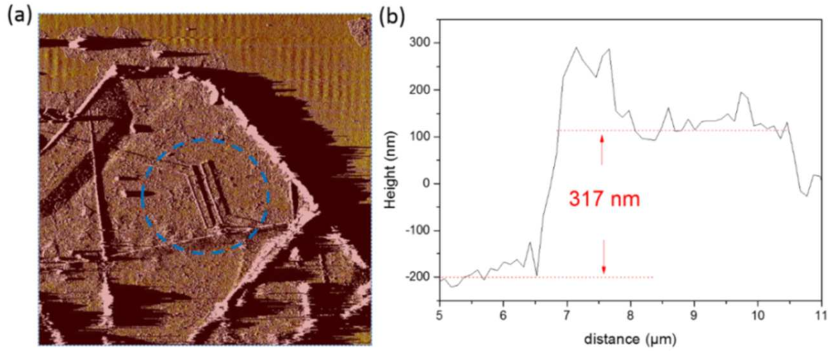
Supplementary Figure S4. Raman and PL characterization of PVD-grown few-layer WSe_2. Typical Raman (a) and PL (b) spectra of PVD-grown few-layer WSe_2 flakes. The existence of the small peak at ~303 cm^{-1} (which is a fingerprint of few-layer WSe_2) and weak PL intensity indicate that these samples are few-layer WSe_2 flakes. The Raman and PL spectra were taken at the same laser power as shown in Figure S1 for CVD-grown monolayer samples.



Supplementary Figure S5. I_{ds}-V_g curves of few-layer WSe_2 FETs after 250 °C air heating. Different colors indicate different devices. The devices show increased on-state current compared to 200 °C heated few-layer WSe_2 FETs, but with low on/off ratio of less than 10.



Supplementary Figure S6. Effects of vacuum annealing on device performance of WSe_2 FETs. (a), (b), (c) show three typical devices after vacuum annealing. The black curves and red curves corresponding to as-made and vacuum annealed devices, respectively. The V_{ds} was 1V for all measurements. The vacuum annealing was done at 200 ^{o}C for 1hr in a tube furnace, and the pressure was 12 mTorr. After annealing, the devices show slight change (either increase or decrease) of on-state current. The magnitude of device current change by heating devices in vacuum (<5x) is significantly smaller that heating in air (1000x).



Supplementary Figure S7. A FET based on CVD monolayer WSe_2 flake grown on BN. (a) A phase mode AFM image showing the FET structure. The blue dash line circles out the position of this WSe_2 flake. (b) Height profile across the edge of BN showing its thickness is 317 nm.