Electronic Supplementary Material (ESI) for Nanoscale.

Supporting information for

Facile and low-cost length sorting of single-wall carbon nanotubes by precipitation and applications for thin-film transistors

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1. Absorption spectra of PMAA and PSS precipitated SWCNTs.

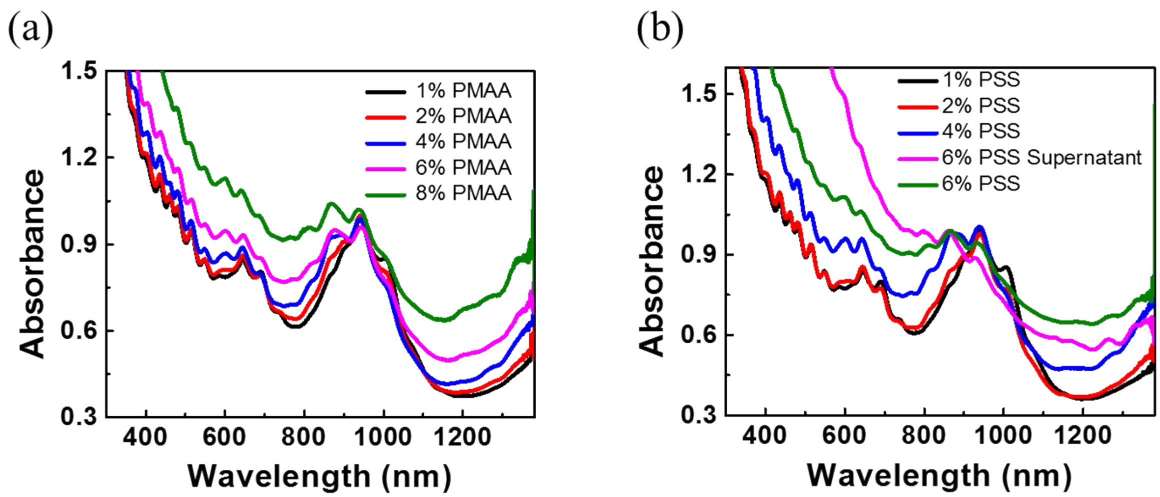

Figure S1. UV-vis-NIR absorption spectra of (a) 1% to 6% PMAA and (b) PSS precipitated nanotubes.

2. PSS Molecular weight effect

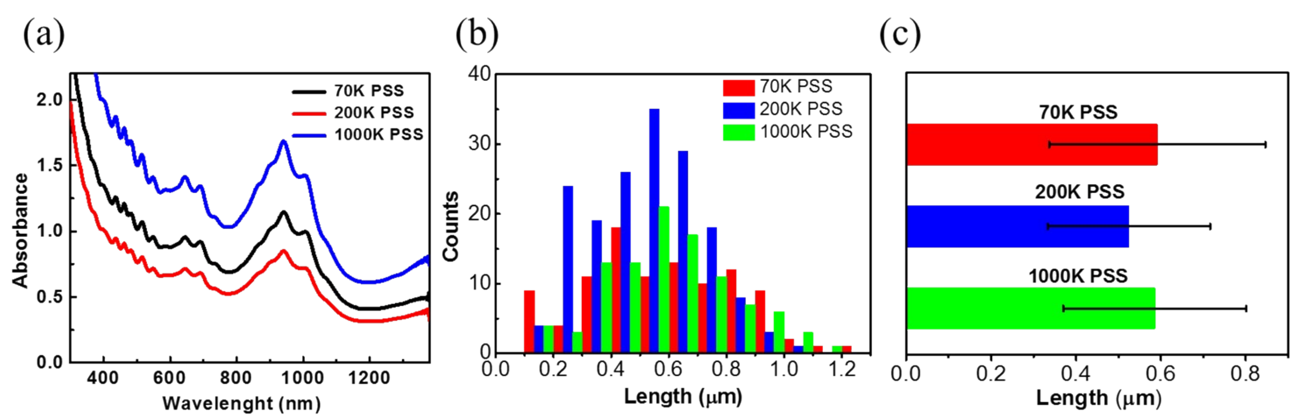

Figure S2. (a) UV-vis-NIR absorption spectra of nanotubes precipitated by 1% PSS with molecular weight of 70 KDa, 200 KDa and 1000 KDa respectively. (b) The histogram of the three kinds of nanotube precipitates from 1% PSS with molecular of 70 KDa, 200 KDa and 1000 KDa, respectively. (c) Average length and deviation of the three kinds of nanotubes precipitated by 1% PSS with molecular weight of 70K, 200K and 1000K, respectively.

3. Semiconducting tubes from the shortest length fraction

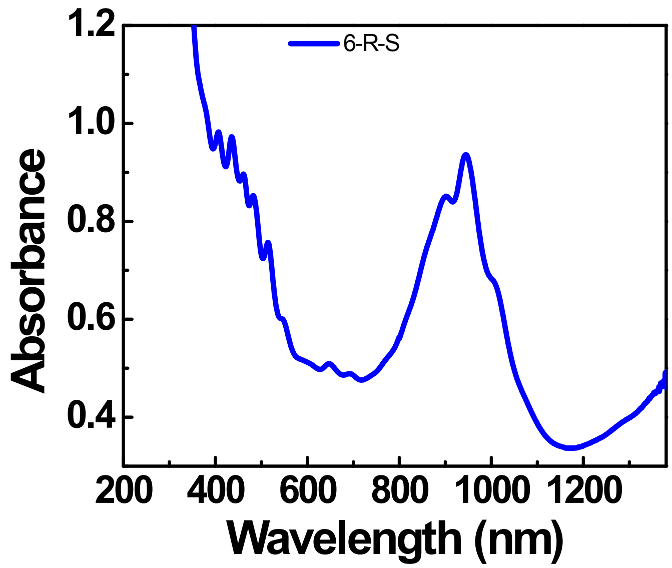

Figure S3. Absorption spectrum of the semiconducting fraction 6R from the 6% PMAA length fraction.

4. TFT output characterization

The output characteristics of TFTs made of the 1-R fraction is shown below. When voltage is between -0.1 V and 0.1 V, the drain current and drain voltage show linear relationship under different gate voltage. When drain voltage is increased to -5V, the drain current starts to saturate.

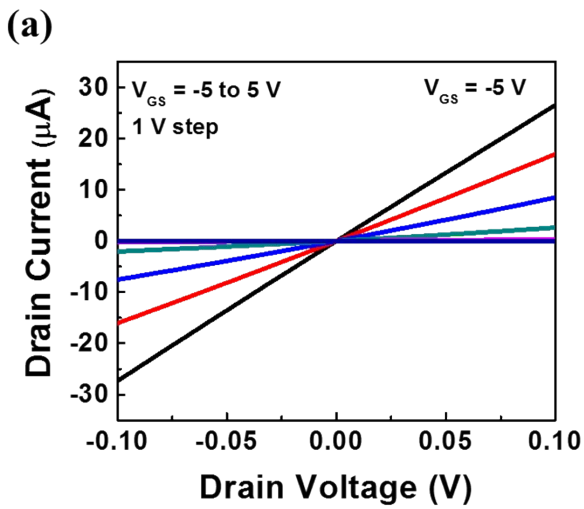

Figure S4. Output characteristics of devices (L = 4 μm, W = 400 μm) made of the 1-R fraction.

(a) linear regime; and (b) saturation region .

5. TFT performance of 6-R

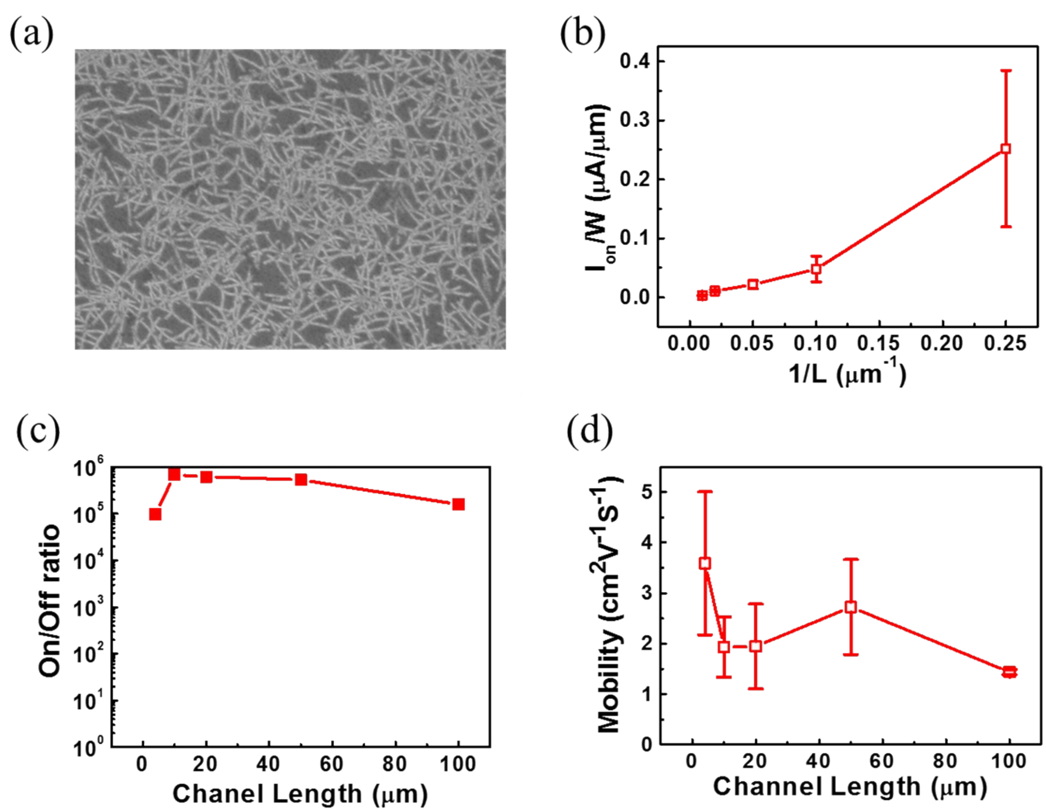

Figure S5. (a) SEM image of the 6-R nanotube thin-film network on a Si/SiO2 substrate. (b) On-current density versus inverted channel length of TFTs fabricated with the 6-R fraction. (c) on/off ratio versus channel length of TFTs fabricated with 6-R fraction. (d) Relationship of mobility and channel length of TFTs made with the 6-R fraction.

6. Mobility calculation method

The mobility is calculated using the parallel plate model, with the following equation:

$$\mu_{device} = \frac{L}{V_d C_{ox} W} \frac{dI_d}{dV_g} = \frac{L}{V_d C_{ox}} \frac{g_m}{W},$$

where W represents the width of the device channel, ε is the dielectric constant of SiO_2, L is the length of the channel, g_m is the transconductance, that is, the maximum slop of the Vg-Id curve. C_{ox} is the gate capacitance. C_{ox} is calculated using a parallel plate model as ε/t_{ox}, where t_{ox} and ε are the thickness and dielectric constant of SiO_2 layer, respectively.