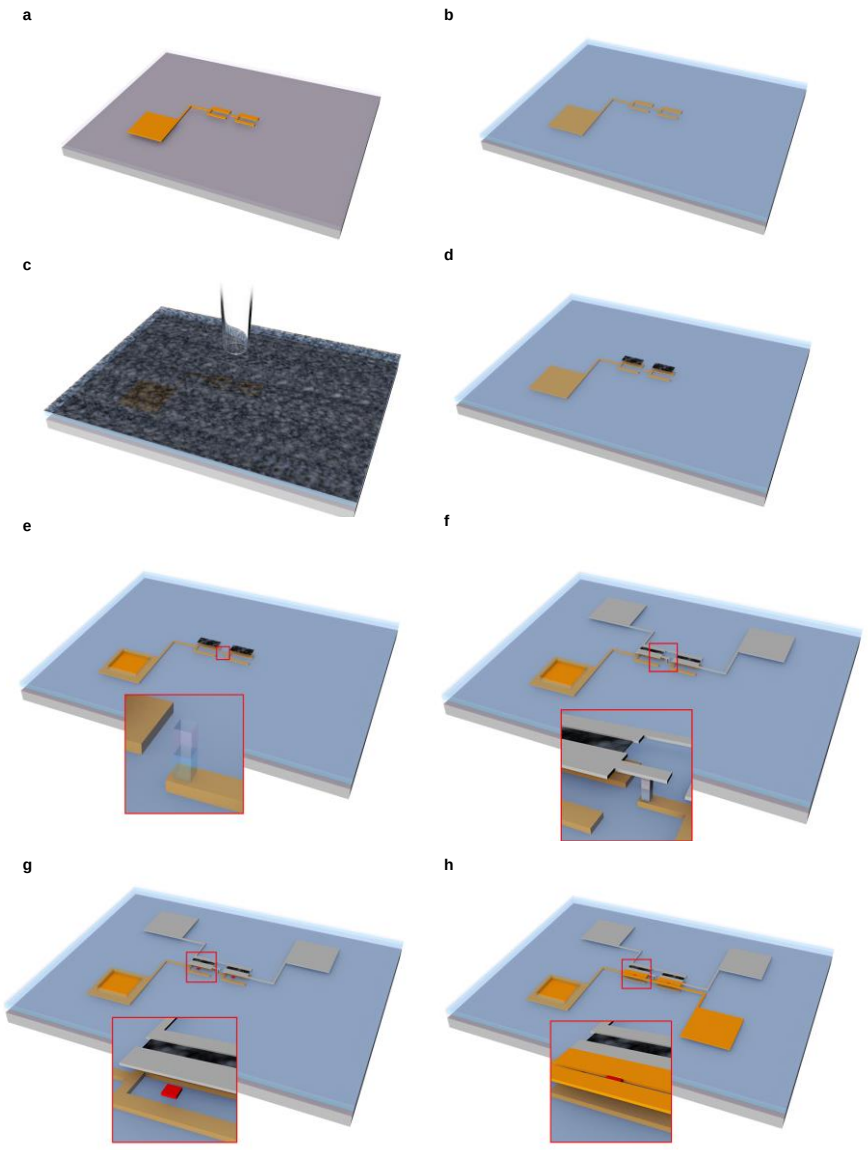

Supplementary Figure 1| Fabrication procedure of hybrid CNT/IGZO complementary integrated circuits. a, Individual bottom-gate electrodes are patterned by photolithography on a highly doped p-Si substrate with a layer of thermally grown oxide (300 nm). E-beam evaporation is used to deposit Ti/Au (5 nm/50 nm) to form the electrodes. **b,** A layer of 40 nm of Al_2O_3 is deposited on the electrodes by ALD at 250 ˚C, which is then followed by deposition of 5 nm of SiO_x by E-beam evaporation to form the dielectric layer for the circuits. **c,** Incubation of 98% semiconducting enriched CNT solution on the surface of the sample. **d,** CNT channels are then defined by photolithography and are followed by O_2 plasma etching at 100 W/150 mTorr for 1 minute and 15 seconds. **e,** Vias or interconnects between devices and probing window on testing pads for gate electrodes are patterned by photolithography and the dielectric material at the vias and on the testing pads is etched by buffered oxide etchant (buffered HF 7:1) for 1 minute and 20 seconds. **f,** Electrodes for the p-type CNT TFTs are defined by photolithography and then formed by E-beam evaporation with Ti/Pd (1 nm/50 nm). **g,** A layer of 50 nm of IGZO thin film is deposited by DC magnetron sputtering at 180 W. **h,** The circuit is completed by patterning the electrodes for the n-type IGZO TFTs and metallization of Ti/Au (1 nm/50 nm) with E-beam evaporator.