GaAs nanowire array solar cells with axial p-i-n junctions

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Supporting Information

Simulation. We use the finite-difference time-domain method to get the absorption spectra and the generation profile throughout the nanowires under the AM1.5G solar illumination, by integrating from which we can get the maximum achievable short circuit current from a certain nanowire structure. Then we use coupled electromagnetic and carrier transport simulations to solve both absorption properties and J-V response of the nanowire array with different structure parameters and junction designs. Simulation details can be found somewhere else[37].

GaAs nanowire growth. 20nm thick silicon nitride layer is deposited by plasma enhanced chemical vapor deposition (PECVD) followed by patterning of 1mm^2 array of holes using electron beam lithography (EBL) and reactive ion etching (RIE). Nanowires are then grown in a vertical Thomas Swan MOCVD with shower head at temperature of 760 ℃ and 0.1 atm pressure. Trimethylgallium (TMG) and arsine (AsH_3) are used as the precursors for Ga and As. Disilane and Diethylzinc are choosen as the precursors for n-type and p-type dopants. The total flow rate of carrier gas is 7 standard liter per minute (SLM) and partial pressure for TMG and AsH_3 are 7.56×10^{-7} atm and 2.14×10^{-4} atm.

Solar cells fabrication. Transparent insulating polymer BCB (Cyclotene, Dow) is drop-casted on the as grown samples and let infiltrate for about 12 minutes for complete penetration to the root of nanowires. The polymer is then spun at 6000 rpm to achieve a film thickness around 2.5 μm. The polymer is cured at 250 ℃in vacuum furnace and etched by CF_4/O_2 RIE to expose the tip consisting p-type emitter. Subsequently front electrode is formed by depositing a 300nm thick Indium-Tin-Oxide (ITO) using RF sputtering at 300W power and 5mT chamber pressure. AuGe alloy is deposit at the back of substrate and annealed at 400℃ to form backside ohmic contact.

Challenges in nanowire based multi-junction solar cells. The idea of tandem solar cells involving nanowires have been proposed for years and systematic simulations were carried out and predicted optimal device architectures by several groups[1-3]. However the experimental implementation of such devices is facing several technological challenges. Well-controlled nanowire growth on heterogeneous substrate, especially those with mismatched lattice, is the most critical issue. Some encouraging progress has been demonstrated recently on the growth of GaAs nanowires on Si substrate using SAG[4], VLS[5] or self-catalyzed[6] techniques. However the size of the nanowires is often limited to the critical diameter[7-9] in order to avoid mis-fit dislocations and abnormal growth orientation which exerts constrain on the optimization at device level, such as to mitigate

over overwhelming surface recombination encountered by thin nanowires. Secondly, tunnel junctions between the nanowire sub-cells and the bottom planar sub-cells have not been explicitly demonstrated yet mostly due to the difficulties in the precise characterization of spatial doping concentration within the nanowires. Recently several groups reported III-V nanowire/Si hetero-structured tunneling junction[10-13] which might provide an alternative interconnecting scheme.

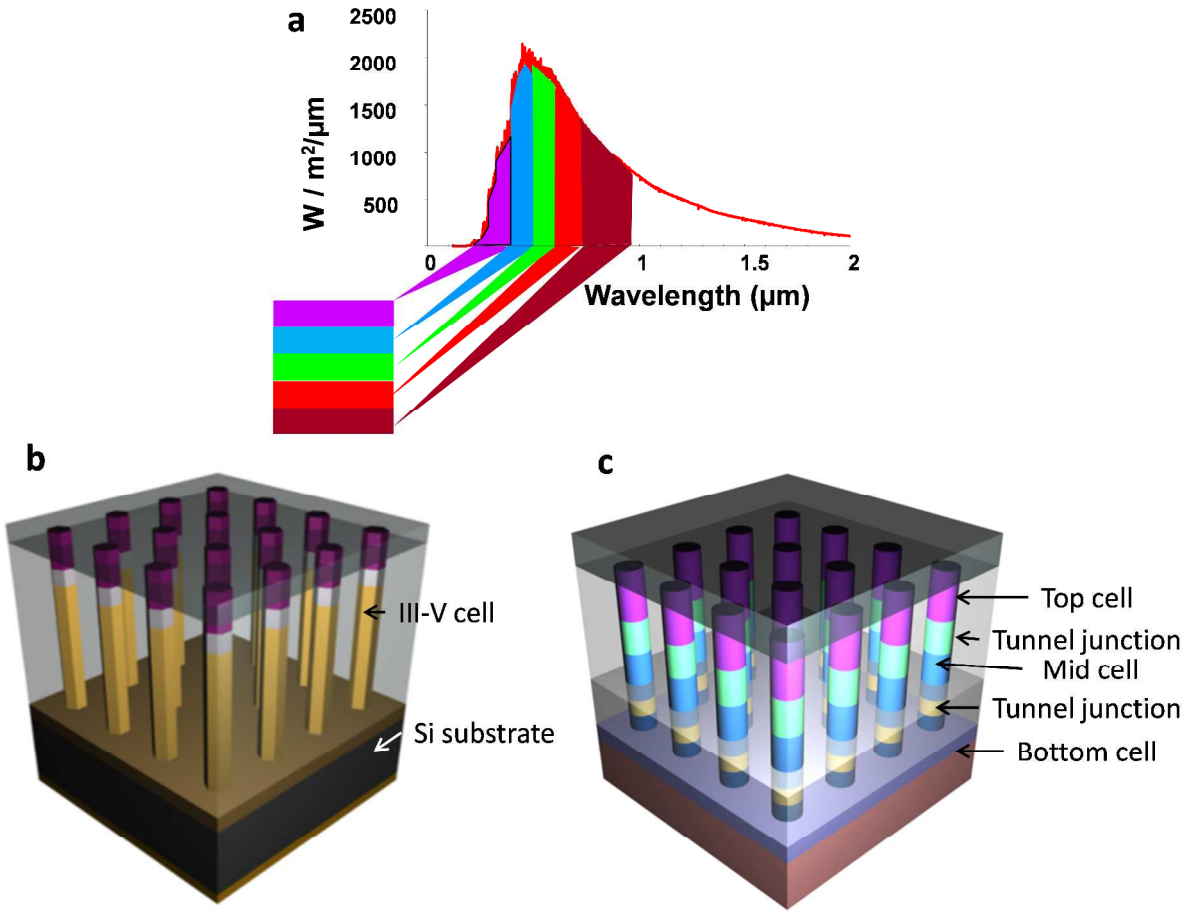

Figure S1. Multi-junction solar cells. (a) Multi-junction solar cells consist of materials with different band-gaps. Materials with larger band-gaps stack on top so different parts of the solar spectrum can be preferentially absorbed at different depths from the surface. (b) A solar cell made from III-V nanowire p-n junctions grown on Si substrate. (c) A

three-junction solar cell made from heterogeneous III-V nanowires grown on Si solar cells.

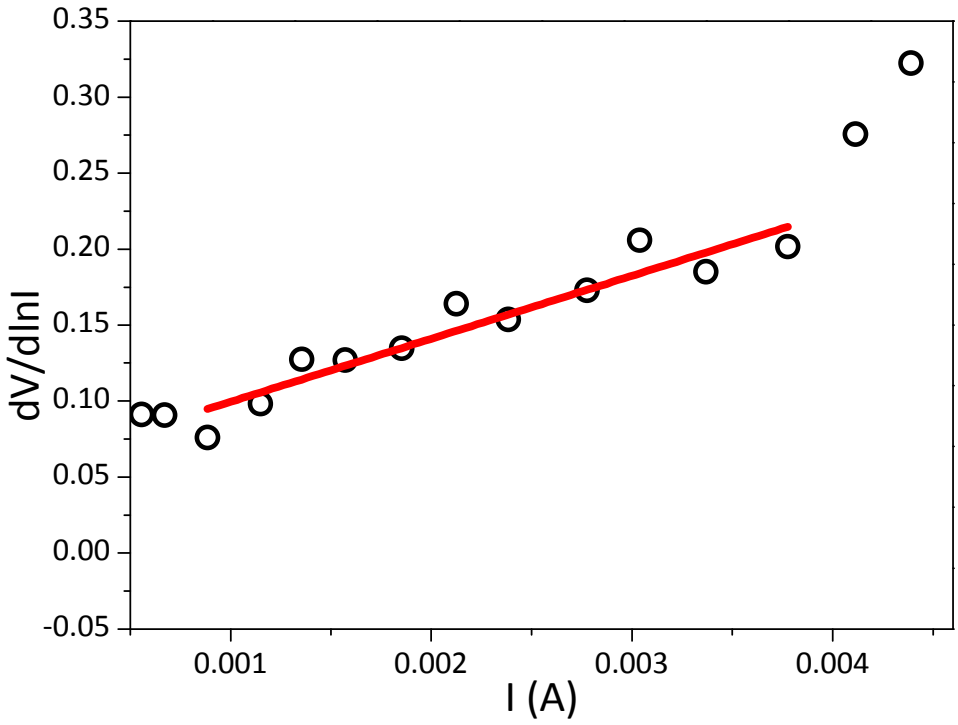

Figure S2. *dV/d(lnI)* versus *I* curve of the device showing the highest efficiency. Based on Cheung's method, R_s is the slope and *nkT/q* is the y-axis intercept. The extracted values of ideality factor and series resistance are 2.2 and 41 Ω, respectively.

Fig. S3 shows the performance of a sample (referred to as Sample G in Table 1) with 320 nm diameter and 300 nm junction depth, so it differs from Sample D only in diameter and differs from Sample F only in junction depth. We can find that the Sample G performance is closer to Sample F performance and farther away from Sample D performance, which tells us that the nanowire diameter affects the solar performance more significantly than the junction depth.

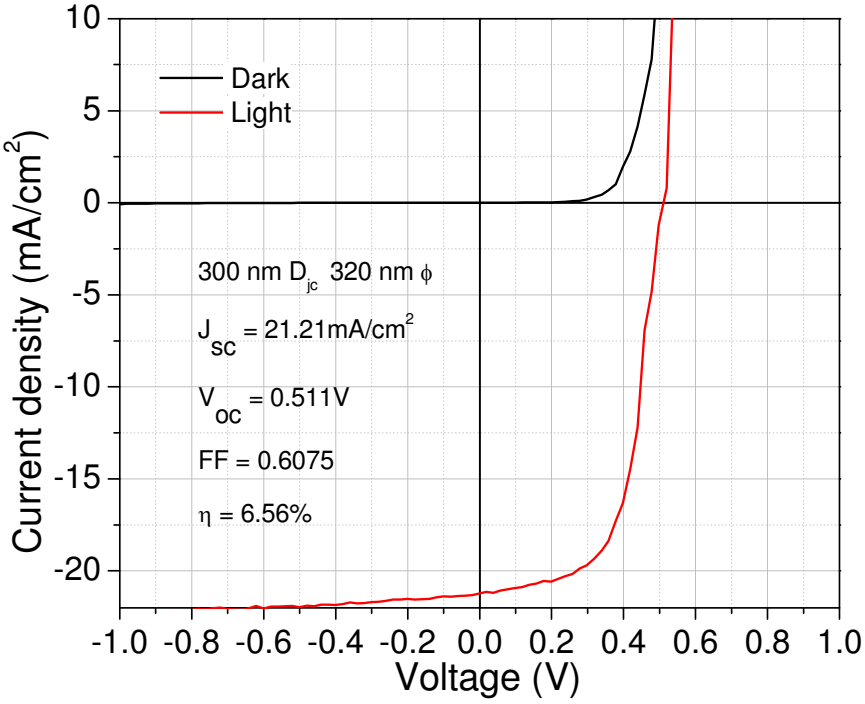

Figure S3. Dark and light I-V curves of device with 320 nm diameter and 300 nm junction depth (referred to as sample G in the paper) .

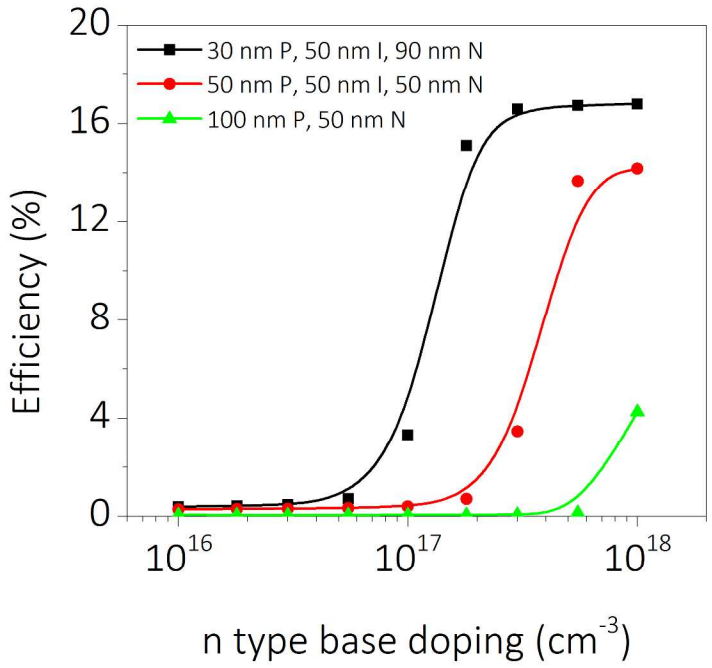

Figure S4. Efficiency as a function of n-type base doping for three radial junction structures: 30 nm p-shell/50 nm intrinsic/90 nm n-core (black), 50 nm p-shell/50 nm intrinsic/50 nm n-core (red), and 100 nm p-shell /50 nm n-core (green)

J_{sc} depends on the broadband absorption spectrum of the nanowire structure as well as the incident solar flux spectrum. The following figure shows the spectral current density for nanowire arrays with 150 nm, 200 nm and 300 nm diameters; J_{sc} is found by integrating the area under the curve up to a wavelength of 867 nm, corresponding to the GaAs band gap. The lattice constant is fixed to be 600 nm. For the 150 nm case, there are two peaks at 450 nm and 800 nm, which correspond to TM12 and TM11 modes (Hu et al., Energy Environ. Sci. 2013). For the 200 nm case, the modes shift to longer wavelengths; the higher wavelength mode lies above 867nm. The integrated area under the curve decreases,

resulting in a local minimum in J_{sc}. As we further increase the diameter of the nanowires, the TM12 mode overlaps better with the solar spectrum, leading to higher current.

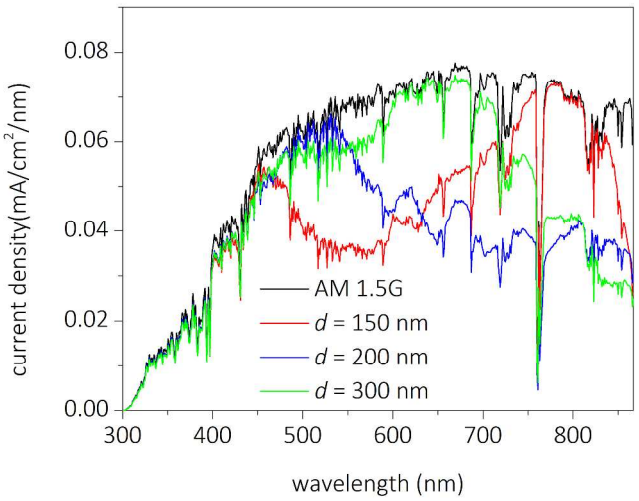

Figure S5. Current density spectra for nanowire arrays with 150 nm (red), 200 nm (green) and 300 nm (blue) under AM 1.5G solar spectrum (black). Pitch is fixed at 600 nm and height is fixed at 3μm.

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