Giant random telegraph signals in the carbon nanotubes as a single defect probe

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Giant random telegraph signals (RTSs) are observed in *p*-type semiconducting single-wall carbon nanotube (SWNT) field-effect transistors (FETs). The RTSs are attributed to the trapping and detrapping of the two defects inside SiO_2 or in the interface between SWNT and SiO_2. The amplitude of the RTSs is up to 60% of total current. The giant switching amplitude of RTSs is believed to be caused by the strong mobility modulation originated from the charging of the defects in the one-dimensional carbon nanotube channels with an ultrasmall channel width on the order of 1–3 nm. The potential application of RTSs in SWNT as a sensitive probe to study single defects is discussed. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1901822]

The random jumps of the conductance due to the capture and emission of carriers by trapping centers at Si/SiO_2 interface in the submicron metal-oxide-semiconductor field effect transistors (MOSFETs), referred to as random telegraph signals (RTSs), have been extensively studied.[1–4] RTSs have been observed in various types of devices, such as, conventional metal oxide semiconductor field effect transistors (MOSFETs), junction field effect transistors (JFETs), quasi-one-dimensional GaAs/AlGaAs high electron mobility transistors made by split-gate technique,[5] and single electron transistors (SETs).[6,7] The studies of RTSs have mainly focused on the understanding of noise performance of devices. It is believed that individual charge trapping has a Lorentzian noise power spectrum. Because of a large number of defects in large devices within a few *kT* range of the Fermi energy, the superposition of many Lorentzians with a broad range of time constants yields low frequency $1/f$ noise in relatively large devices.[1,2] With the continuing scaling down of CMOS and the development of nanotechnology,[8–11] atomic level interface imperfection and single defect in the self-assembled nanowires and carbon nanotubes (CNTs) can dramatically affect device performance. At the same time, the understanding of materials, such as high-*k* material, and the interface will further help CMOS scaling. However, conventional capacitance-based defect characterization methods, such as deep level transient spectroscopy (DLTS), cannot be applied to nanodevices because of the lack of sensitivity due to small capacitance of nanodevices. Hence, nanometrology is needed for characterizing nanodevices. In this sense, the noise becomes the signal. RTSs have been used as sensitive probes to investigate tunneling phenomena in the atomic level.[12] Recently the spin properties of defects in the MOSFETs were studied.[13,14] In this work, RTSs in the self-assembled one-dimensional (1D) *p*-type CNT FETs are investigated. The characteristics of the RTSs are analyzed under different gate biases (V_g) and source-drain biases (V_{ds}). The mechanism of the giant RTSs in the CNT FET is discussed. It will be shown that the giant RTSs in the CNTs yield a high signal-to-noise ratio for probing single defects. Hence, the RTSs in nanoscale devices are proposed as a sensitive nanometrology tool to study defects or interface states of nanodevices and material properties.

CNT FETs were fabricated using chemical vapor deposition (CVD) grown SWNTs[15] on silicon substrate covered with a 500 nm thermal oxide as the gate dielectric layer. Catalyst islands of $Fe(NO_3)_3$ mixed with Al_2O_3 were deposited onto the substrate and then heated up to 900 °C in the flow of a gas mixture of CH_4, H_2, and C_2H_4. The processes produced nanotubes with diameters of 1–3 nm. The length of the SWNT is 4 μm. After the synthesis, photolithography was applied to define the electrodes on top of the nanotubes, followed by Ti/Au deposition as the contacts. The scanning electron microscopy (SEM) image is shown in Fig. 1(a); the schematic drawing and the band structure of the measured devices are shown in Figs. 1(b) and 1(c), respectively. The device measured shows a typical *p*-type transistor characteristic, suggesting only semiconducting carbon nanotubes bridged the source and drain electrodes. The following measurements were carried without electrically stressing on the device.

The RTSs at 4.2 K taken as a function of V_g for $V_{ds}=0.1$ V, and $V_{ds}=0.5$ V are shown in Fig. 2. Current (I–V) was measured after amplification of the signals using a standard operational amplifier through a sampling resistor. Instead of the monotonic increasing of the current with respect to V_g, the giant current switching happens near $V_g=-8.5$ and -10.5 V. Strong gate bias dependencies of the shape and the up–down ratio (capture-emission ratio) of the RTSs indicate that the filling and unfilling of the defects by holes are under the gate control. These experimental observations indicate that the RTSs result from the trapping and detrapping of holes by the defects inside the SiO_2 or in the CNT/SiO_2 interface. As shown in Fig. 1(c), the CNT FET Fermi energy aligns with the first defect (A) at approximating $V_g=-9$ V so that the carriers in the two transport channels hop into or out of the trap level as indicated in region I of Fig. 2(b). As V_g

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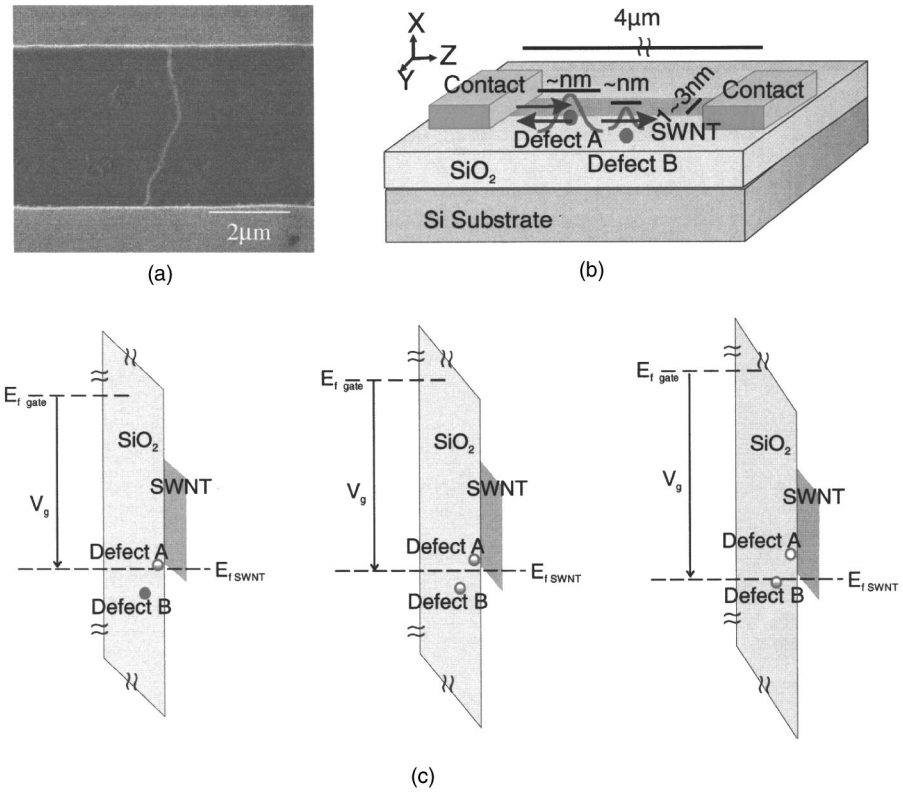

FIG. 1. (Color online) (a) SEM image of a CNT FET device; (b) Schematic drawing showing the CNT FET with two defects inside the SiO_2 or at the SWNT/SiO_2 interface. The Coulomb potential produced by the charged defect extends further than the diameter of the SWNT. The potential extension pinches off parts of the conducting channels, resulting in the giant RTSs. (c) The band diagram explains the alignment of the Fermi energy with the defects under different V_g, giving rise to the four level switching of the drain current (RTSs). The band diagram is used for the explanation of the observed RTS data.

decreases further to about -12 V, the Fermi level of the CNT FET moves toward a second defect (B). The observed four levels of RTSs agree with the switching effects due to the two defects, A and B.[5] These two defects may be either spatially located differently or have a different energy or a combination of both. At last, when $V_g < -14$ V (region III), only defect B is near the Fermi energy of CNT FET so that two level switching is observed again.

Figure 3 shows typical switching of the source–drain current as a function of time, using 0.4 s for taking each data point with a total time interval of 200 s. It is worth noting that the RTS amplitude as shown in Fig. 3(a) may be up to 60% of the total source-drain current of 5×10^{-8} A. In contrast, the amplitude of RTSs observed in the past is normally no more than 5% in MOSFETs. In some special cases, even though as large as 70% amplitude of RTSs was observed in MOSFETs at room temperature, these RTSs were only occasionally seen at particular bias conditions. Defect interaction and quantum tunneling were used to explain these giant RTSs.[16–18] In our case, the amplitude of the RTSs is significantly large ($>10\%$) for both single defect and two defects cases in a broad V_g range for small V_{ds} biases ($V_{ds} < 0.2$ V). From the first order analysis, the change of current resulting from the defect charging/discharging can be expressed as:

$$\frac{\Delta I}{I} = \frac{\Delta n}{n} + \frac{\Delta \mu}{\mu},$$

where I, n, and μ represent current, mobile carrier density, and mobility in the devices, respectively. On one hand, the number of carriers in the two conducting channels of the CNT fluctuates because of the hopping/tunneling of one hole from the transport channels into the defect states. However, in our case, the CNT FET works in the strong inversion region. The total number of holes in the two conducting channels is quite large on the order of several thousands, thus, the change of current due to one hole in the channels gives little effect on the total current in the FET. It is also shown that the transport in SWNTs is nearly ballistic of two conducting channels with a mean free path of several microns.[19] Positive Coulomb potential by trapping a hole of the near defects can significantly perturb the conduction of the holes in the channels and decrease the mobility, conductance, and current. As shown in Fig. 1(b), the potential perturbation caused by defects in the strong inversion is roughly on the order of several nanometers because of the charge screening of the channel holes,[20] but the SWNT has an even smaller diameter of about 1–3 nm. This fact explains that the defect potential completely blocks the carriers in the 1D transport channels, which is a clear contrast to the lateral current transport in the 2D case for most of previous works. Moreover the scattering only occurs in forward and backward directions in the 1D CNT. Together with the nearly 1D ballistic transport, the amplitude of the switching of the current becomes large. These facts explain the giant fluctuations observed due to the single defects charging in the 1D transport in the time domain. Schottky contacts,[21] 1D density of states and hole–hole interactions need to be taken into consideration for detailed analysis.

From our previous discussions, it is clear that there is a considerably large signal (RTS switching amplitude)-to-noise (background noise)-ratio due to the small channel width in the SWNT. Comparing to a capacitance-based measurement, such as DLTS for studying defects/interfaces in the nanoscale devices, our current-based measurement technique

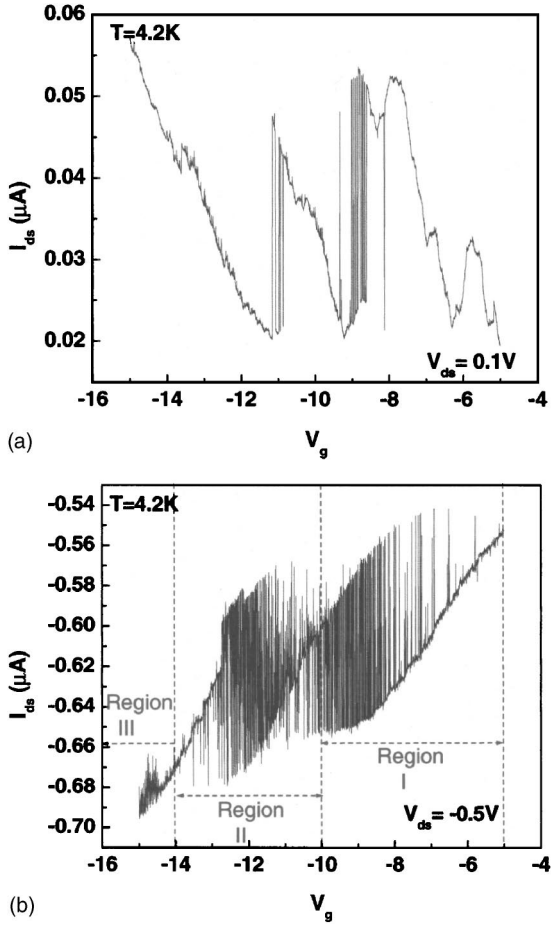

FIG. 2. (Color online) Current as a function of V_g at $T=4.2$ K with a V_g scanning rate of 5 mV/s for $V_{ds}=0.1$ V (a) and $V_{ds}=-0.5$ V (b). The energy band diagram [Fig. 1(c)] suggests that the CNT FET Fermi energy is approximately aligned with one defect (defect A) in region I from -8 to -10 V. At a large negative V_g, the Fermi energy aligns towards the second defect (B) so that the presence of the two defects A and B illustrates a four level switching characteristics at large gate bias. With further decreasing V_g (region III), defect B aligns with the CNT FET Fermi level.

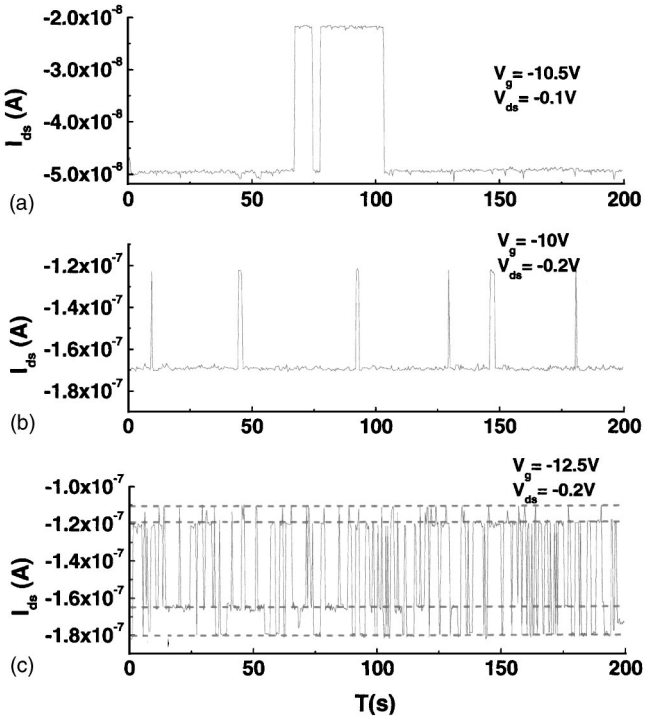

FIG. 3. (Color online) Typical switching of the source-drain current observed for a total time period of 200 s. (a) up to 60% switching amplitude of the total current is observed at $V_g=-10.5$ and $V_{ds}=-0.1$ V; (b) switching due to defect A; (c) four level switching due to defects A and B, when V_g is varied from -10.5 to -12.5 V, while V_{ds} is kept at -0.2 V.

has a much higher sensitivity. The sensitivity of the current-based RTSs probe does not decrease as device areas is scaled down, and in fact, a narrow channel width will make single defect detection realizable with a high sensitivity. Hence, the RTSs in the CNT FET can be used as a sensitive probe for studies of single defects/interface states, material properties, and other physical phenomena.

In summary, the giant RTSs originating from the trapping and detrapping of the two defects in the SiO_2 or the CNT/SiO_2 interface are observed in the *p*-type semiconducting CNT FETs. The amplitude of the RTSs is up to 60% of total current. The switching of the current is attributed to the mobility modulation due to the charged defect Coulomb scattering potential. Because of the small diameter of 1D transport channels in the SWNT, the amplitude of the switches is quite large. These results demonstrate that the RTSs in the 1D nanodevices can be used a valuable probe for characterizing material and nanodevices.

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