Nanowire transistors with ferroelectric gate dielectrics: Enhanced performance and memory effects

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Integration of ferroelectric materials into nanoscale field-effect transistors offers enormous promise for superior transistor performance and also intriguing memory effects. In this study, we have incorporated lead zirconate titanate (PZT) into In_2O_3 nanowire transistors to replace the commonly used SiO_2 as the gate dielectric. These transistors exhibited substantially enhanced performance as a result of the high dielectric constant of PZT, as revealed by a 30-fold increase in the transconductance and a 10-fold reduction in the subthreshold swing when compared to similar SiO_2-gated devices. Furthermore, memory effects were observed with our devices, as characterized by a counter-clockwise loop in current-versus-gate-bias curves that can be attributed to the switchable remnant polarization of PZT. Our method can be easily generalized to other nanomaterials systems and may prove to be a viable way to obtain nanoscale memories. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1759069]

Nanoelectronics based on nanowires and nanotubes is considered to be a promising alternative solution to break the scaling limit the silicon industry may soon have to face. The past few years have witnessed tremendous growth in this direction, and various nanowire and nanotube devices have been designed and evaluated.[1–5] Recently, In_2O_3 nanowires have been successfully synthesized and tailored to work as interesting nanoelectronic building blocks such as nanoscale transistors,[6,7] photodetectors,[8] and chemical and bio-sensors.[9,10] These devices typically utilize SiO_2 as the gate dielectric, and its relatively low dielectric constant imposes a severe constraint on the device performance. In contrast, ferroelectric materials have steadily emerged as important candidates to work as gate insulators for their ultrahigh dielectric constants and intriguing remnant polarization.[11–14] As a result, integrating ferroelectric gate insulators into nanowire FETs is expected to deliver substantially enhanced performance and also nonvolatile memory effects for data storage. In this study, we have incorporated lead zirconate titanate (PZT), a ferroelectric material, into In_2O_3 nanowire field effect transistors to replace the commonly used SiO_2 as the gate dielectric. These transistors exhibited very strong gate dependence, significantly reduced subthreshold swing and substantially enhanced transconductance as a result of the high dielectric constant of PZT. Furthermore, pronounced memory effects were also observed, as revealed by the hysteresis in current-versus-gate-bias curves that can be attributed to the switchable remnant polarization of PZT.

Our fabrication starts with preparing high-quality PZT films on top of platinized silicon substrates using a sol-gel approach, and the detail of process and study can be found in our previous publications.[15,16] Figure 1(a) shows the x-ray diffraction pattern of 400 nm PZT thin films used in our study. A strong peak corresponding to PZT (111) can be seen together with two weak peaks (001) and (002), indicating that (111) is the highly preferred orientation for our PZT films. A strong peak corresponding to Pt(111) can also be observed. This is because there is a good match of lattice constants between the PZT films and the underlying Pt electrode. Figure 1(b) inset depicts an atomic force microscope image of the PZT film showing a mean roughness of 1.089 nm, indicating good film quality. The ferroelectric hysteresis loop of the PZT film is shown in Fig. 1(b). The remnant polarization (P_r) is determined to be ~14 $\mu C/cm^2$, and the coercive field is about 13 kV/cm. The PZT dielectric constant is determined to be ~500 by measuring a capacitor made by depositing Pt top electrode to a $PZT/Pt/SiO_2/Si$ substrate.

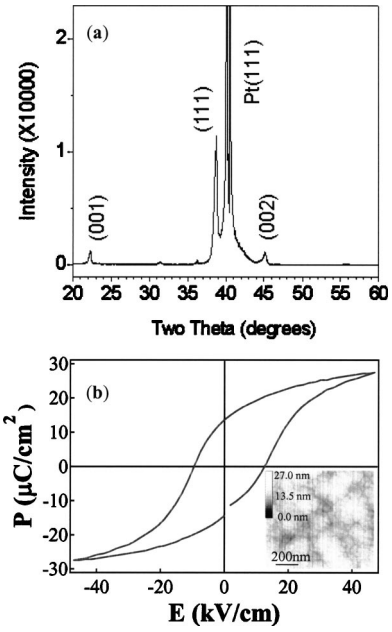

FIG. 1. (a) X-ray diffraction pattern of the PZT film on a $Pt/SiO_2/Si$ substrate. (b) $P-E$ hysteresis loop measured on a $Pt/PZT/Pt/SiO_2/Si$ device. Inset: an atomic force microscope image of the PZT film showing a mean roughness of 1.089 nm.

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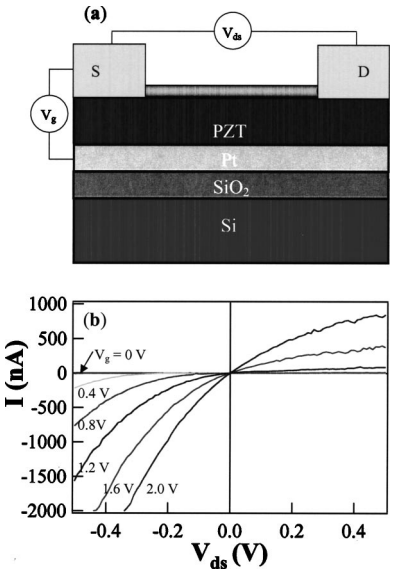

FIG. 2. (a) Schematic circuit diagram of an In_2O_3 nanowire FEFETs. (b) $I-V_{ds}$ curves recorded under various gate biases.

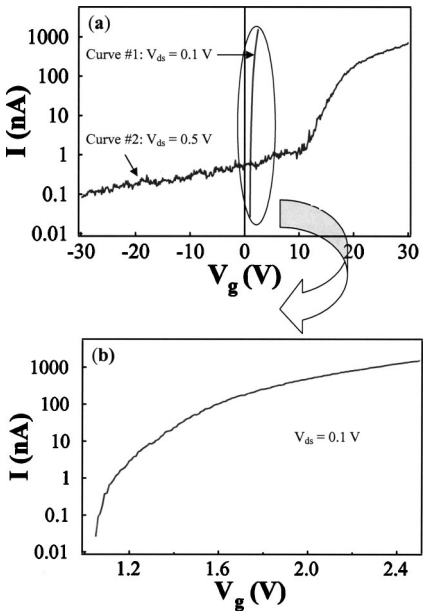

FIG. 3. (a) $I-V_g$ curves recorded under $V_{ds}=0.1$ V for the In_2O_3 nanowire FEFET (curve 1) and under $V_{ds}=0.5$ V for the conventional In_2O_3 nanowire FET (curve 2). (b) The zoom-in diagram of curve 1.

The schematic structure of our In_2O_3 nanowire FETs is depicted in Fig. 2(a). Single-crystalline In_2O_3 nanowires of 10 nm in diameter were synthesized by using a laser ablation process described before.[7] Two kinds of substrates were used in our study for direct comparison: Si substrates coated with 500 nm SiO_2 for conventional nanowire transistors and also PZT(400 nm)/Pt(120 nm)/SiO_2(200 nm)/Si substrates for ferroelectric gated nanowire field effect transistors (FEFET). The In_2O_3 nanowires were first sonicated into a suspension in isopropanol and then deposited onto the substrates using a spin-on technique. Photolithography and Ti/Au deposition were employed to pattern the drain and source electrodes to contact both ends of individual nanowires. The degenerated doped silicon substrate was used as a back gate for conventional In_2O_3 nanowire FETs, while the Pt layer was used as a back gate for In_2O_3 nanowire FEFETs. Our nanowire field effect transistors typically have channel width $\sim$10 nm (defined by the nanowire diameter) and channel length $\sim$2–3 μm. In this study, all the electronic measurements were conducted at room temperature with the devices residing in a high-vacuum chamber to eliminate the effect of moisture.

For In_2O_3 nanowire FEFETs, altogether eight devices were carefully examined. Figure 2(b) shows a family of current versus drain-source voltage ($I-V_{ds}$) curves from a typical In_2O_3 nanowire FEFET under different gate biases (V_g). Six curves at $V_g=0$ V, 0.4, 0.8, 1.2, 1.6, and 2.0 V are displayed in this figure. As the gate bias varied from 0 to 2.0 V, the conductance of the nanowire increased substantially. Detailed calculation revealed that the differential conductance at $V_{ds}=0$ V increased from 6.01×10^{-11} S at $V_g=0$ V to 2.85×10^{-6} S at $V_g=2.0$ V. This increase in conductance driven by such a small change of V_g is generally hard to achieve with conventional In_2O_3 nanowire FETs with 500 nm SiO_2 gate insulator. It can be clearly seen that all the six $I-V_{ds}$ curves are asymmetric with respect to V_{ds}. Such an asymmetric behavior can be attributed to the local gating effect induced by the drain-source bias. Similar results were observed in conventional In_2O_3 nanowire transistors.[6] In addition, Figure 3(a) shows the $I-V_g$ curve of this typical In_2O_3 nanowire FEFET with 400-nm-thick PZT (curve 1). As a comparison, the $I-V_g$ curve of a typical conventional In_2O_3 nanowire FET with 500-nm-thick SiO_2 layer is also shown in Fig. 3(a) (curve 2). A drastic difference lies in the subthreshold swing (S), defined as $S=\ln(10)[dV_g/d(\ln I)]$.[17] With 500 nm SiO_2 gate dielectric (curve 2), the conventional In_2O_3 nanowire device exhibited a swing of $S\sim4$ V per decade. In contrast, with 400 nm PZT dielectric (curve 1), the In_2O_3 nanowire FEFET showed $S\sim300$ mV per decade, and the current at $V_{ds}=0.1$ V was observed to vary by more than four orders of magnitude when the gate bias was tuned from 1.1 to 2.5 V [Fig. 3(b)], indicating an on/off ratio exceeding 10^4. The subthreshold swing is a key parameter for scaling of field effect transistors. Low threshold voltage and low power operation for miniaturized transistors require a small subthreshold swing. In this regard, the In_2O_3 nanowire transistor with the PZT dielectric instead of SiO_2 has been improved considerably.

To further demonstrate the performance of our In_2O_3 nanowire FEFETs, we have calculated the capacitance, the transconductance, and the electron mobility based on data shown in Figs. 3(a) and 3(b). The nanowire capacitance is given by $C=2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$,[18] where ε is the dielectric constant of PZT, ε_0 the vacuum dielectric constant, L and r the length and radius of the nanowire, h the thickness of the PZT layer. The electrostatic capacitance C is $\sim1.095\times10^{-2}$ pF with $\varepsilon\sim500$, $L\sim2$ μm, $r\sim5$ nm, and $h\sim400$ nm. In contrast, for the conventional nanowire transistors with 500 nm SiO_2 as the gate dielectric, we obtain a gate capacitance of $C\sim8.19\times10^{-5}$ pF with the same nanowire radius and length. This difference in the gate capacitance lies in the heart of the dramatically different gate dependence we observed in Fig. 3. The transconductance characterizing the gate dependence, which was calculated from the slope of the $I-V_g$ curves following $g_m=dI/dV_g$, take values of 2.04×10^{-6} A/V for the FEFET and 6.01×10^{-8} A/V for the conventional nanowire FET. Such a 30-

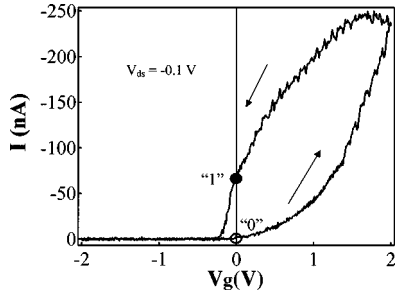

FIG. 4. $I-V_g$ characteristics of the PZT-gated In_2O_3 nanowire transistor with $V_{ds}=-0.1$ V showing pronounced hysteresis. "1" and "0" denote two states at $V_g=0$ for the memory operation.

fold improvement in transconductance has significant implications for the FEFETs to be used for high-frequency applications. Using the equation $dI/dV_g=\mu CV_{ds}/L^2$ for field effect transistors in the linear regime, we get mobility values of $\mu=74.6$ cm^2/V s for the FEFET and 59 cm^2/V s for the conventional transistor shown in Fig. 3. Detailed measurements over other devices revealed a mobility distribution from 10 to 500 cm^2/V s, presumably as a result of the variation in the distribution and concentration of scattering centers. Overall, the performance of In_2O_3 nanowire transistors with PZT has been improved significantly compared with conventional ones.

Besides the enhanced performance originating from the high dielectric constant of PZT, all these devices also showed a similar memory effect correctly mirroring the fact of the switchable polarization of the PZT layer. This memory behavior is characterized by a pronounced counter-clockwise hysteresis loop in the $I-V_g$ curves taken with another device, as shown in Fig. 4. When the gate bias was swept from -2 to 2 V, the device exhibited little conduction at $V_g=0$ V; whereas when the gate bias was swept back from 2 to -2 V, the current was significantly higher than that obtained from the previous sweep. This counter-clockwise loop is in agreement with the memory effect we expect out of the ferroelectric PZT gate insulator, as the gate bias of ± 2 V applied across the 400-nm-thick PZT exceeds the coercive field of 13 kV/cm, and hence remnant polarization is expected at $V_g=0$ V. When V_g was swept from -2 to 0 V, the remnant polarization caused a build-up of negative charges in the upper-side of PZT, which depleted electrons out of the *n*-type In_2O_3 nanowire and thus left the device in a highly resistive state. Conversely, when the gate bias was swept from 2 to 0 V, the remnant polarization led to an enrichment of electrons in the nanowire and hence kept the device in a rather conductive state at $V_g=0$ V. This hysteresis in the $I-V_g$ curve allows us to define two states (denoted State "1" and "0") at $V_g=0$ for the memory operation, as shown in Fig. 4. The current difference (ΔI) between state "1" and state "0" can be derived from the corresponding remnant polarization difference at $V_g=0$, estimated to be $\Delta P=28\ \mu$C/cm^2 from Fig. 1(b). The remnant polarization induces equal amount of charge per unit area in the semiconductor nanowire,[19] and hence the difference in the charge density between state "1" and "0" is given as $\Delta Q_s=\Delta P=28\ \mu$C/cm^2. ΔI can be estimated as $\Delta I=W\Delta Q_s\mu E$, where W is the effective channel width[20] (7.85 nm) and E is the channel electric field (500 V/cm). The mobility derived for this device is around 10 cm^2/V s, with only a slightly difference between different branches of $I-V_g$ loop. ΔI is therefore calculated to be 109.9 nA. As an order-of-magnitude estimate, this is in satisfactory agreement with the experimental value of 66.6 nA determined from Fig. 4. Control experiments were also done with conventional In_2O_3 nanowire FETs with SiO_2 as the gate dielectric, and no such memory effect was observed.

In summary, we have demonstrated the integration of ferroelectric dielectrics into nanowire transistors based on our high quality single-crystalline In_2O_3 nanowires and PZT thin films. Compared to conventional SiO_2-gated transistors, the PZT-gated In_2O_3 nanowire transistors exhibited high transconductance $\sim 2.04\times 10^{-6}$ A/V and small subthreshold swing $\sim$300 mV per decade. Memory effects originating from the switchable remanent polarization of the PZT films have also been successfully observed. Our method can be easily generalized to other nanomaterials systems and may prove to be a viable way to obtain nanoscale memories.

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