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Polymer thin-film transistors with high dielectric constant gate insulators

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ABSTRACT Field-effect transistors consisting of poly(3-hexylthiophene) have been fabricated with high dielectric constant $SrBi_2Ta_2O_9$ films working as the gate insulator. Significantly enhanced gate effects were observed in these devices compared to similar transistors with conventional SiO_2 gate dielectric. Our devices exhibited operating voltages around 10 V, as compared to about 100 V for devices employing SiO_2 as the gate dielectric. Moreover, inverters based on such polymer transistors were demonstrated with nice input–output characteristics.

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The research on organic thin-film semiconductor devices has attracted a lot of attention since early reports on organic field-effect transistors [1, 2]. These transistors can be prepared at low cost and provide large-area coverage even on plastic substrates, thus having great potential to be used in flat-panel displays, integrated flexible logic circuits [3] and sensor arrays [4]. The core of the fabrication approach lies in the preparation of the organic thin films, which typically involves evaporation of small organic molecules [5] such as pentacene, self-assembling of functionalized molecular wires [6] or spin coating of a desired organic semiconductor from its solution [7]. Of particular interest is the spin coating of poly(3-hexylthiophene) (P-3HT), which has been shown to form highly ordered films and render field-effect transistors with high mobilities [7]. Despite the utmost importance of such polymer thin-film transistors, their practical applications for flat-panel displays and flexible logic circuits have been hindered by the high operating voltages involved (typically ~ 100 V in [7]) due to the inefficiency of the SiO_2 gate dielectric. High-κ dielectrics have been pursued to replace SiO_2 as gate insulators [8]. In this paper we report our approach toward polymer transistors with low operating voltages (~ 10 V) by employing high gate dielectric $SrBi_2Ta_2O_9$ (SBT) [5, 9, 10]. SBT films are known to possess high dielectric constants and hence can generate significantly more gate capacitance per unit area than the conventional SiO_2 gate. Our experiments convincingly demonstrate substantially improved performance in transistors with SBT gates, as manifested by the reduction in the operating voltages. Furthermore, we have demonstrated a logic inverter based on our transistors with operating voltages as low as 10 V.

The device fabrication started with preparation of high-quality SBT films. Degenerately doped silicon wafers were chosen as the substrates, on which a layer of silicon nitride (SiN) film, ~ 3 nm in thickness, was deposited to work as a buffer layer. A SBT film, approximately 200 nm in thickness, was then deposited atop the SiN buffer layer by a spin-on method using a presynthesized solution, and subsequently annealed at $\sim 900\,^{\circ}$C in oxygen for one hour. Details of this preparation method can be found in [9]. The SiN buffer layer was included to form a good interface with the silicon substrate and is sufficiently thin so as not to take up a significant portion of the gate voltage. The quality of the SBT film has been confirmed with X-ray diffraction and a dielectric constant of ~ 50 has been derived from previous capacitance–voltage measurements [9].

We defined the source and drain electrodes of our transistors on top of the SBT films using the standard photolithography and lift-off techniques. These Ti/Au electrodes were 200 nm in thickness and yielded device structures with a channel width of 500 μm and three different channel lengths: 12 μm, 4 μm and 2 μm. The final step of our fabrication was the deposition of the active polymer layer. Poly (3-hexylthiophene) with 98.5% head-to-tail (HT) regio-specific conformation (shown in Fig. 1a) was purchased from Sigma Aldrich. Chloroform was used as the solvent to dissolve P-3HT and yield P-3HT solutions with concentrations ∼0.4%. A P-3HT thin film was subsequently deposited by spin coating the P-3HT solution onto the substrates with prefabricated Ti/Au electrodes. The thickness of the P-3HT film was about 200 nm with the 3000-rpm spin speed used. Thus our transistor structure consisted of the active polymer layer contacted by the source/drain gold electrodes with the silicon substrate as a back gate and the SBT film as the gate dielectric, as shown in Fig. 1b. The electrical characterization of these devices was carried out in vacuum (10^{-6} Torr)

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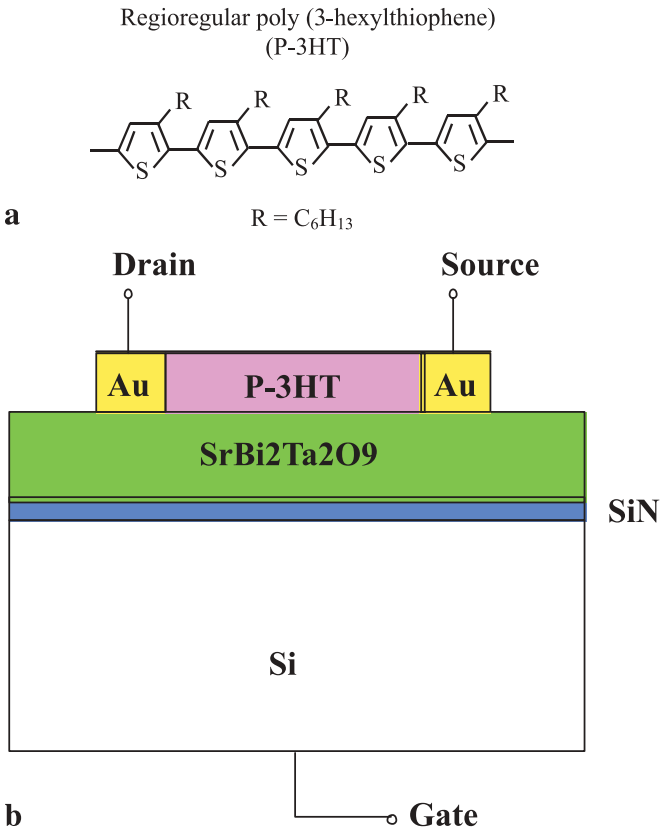

FIGURE 1 **a** Formula of regio-regular poly(3-hexylthiophene) (P-3HT). **b** Schematic diagram of the polymer field-effect transistor with high-dielectric SBT film as the gate dielectric

and at room temperature. The current–voltage characteristics were obtained with an Agilent 4156B semiconductor parameter analyzer.

Figure 2 displays the drain current–drain voltage ($I_d - V_d$) curves for a typical polymer transistor with a channel length of 2 μm and SBT as the gate dielectric, where the gate bias was varied from −4 V to +4 V with 1-V increment from the top curve to the bottom curve. This device exhibited strong conduction with gate bias $V_g = -4$ V, and displayed a monotonic decrease in conduction as V_g increased positively, ending up with almost no current flowing at $V_g = +4$ V. Both the linear regime at low V_d and the saturation regime at high V_d are clearly present in Fig. 2, consistent with the characteristics of a typical *p*-type field-effect transistor. The relation between the drain current and the gate bias for a field-effect transistor in the saturation regime can be described by (1), where μ is the field-effect mobility, Z (500 μm) is the channel width, L (2 μm) is the channel length, C_i is the capacitance per unit area of the gate dielectric and V_{th} is the threshold voltage.

$$I_d = \mu C_i Z/2L(V_g - V_{th})^2 \,. \qquad (1)$$

By sweeping the gate bias with V_d fixed in the saturation regime, an $I_d - V_g$ curve can be obtained, shown as the red curve in Fig. 3. A plot of $(-I_d)^{1/2}$ vs. V_g is shown as the blue line in Fig. 3 and can be fitted with a straight line for $V_g > 0$ V, consistent with (1). This leads to an extrapolated threshold voltage of 0.64 V and a mobility of 7.47×10^{-3} cm^2/V s. This mobility value is consistent with previously reported values [7], indicating that the ordering and crystallinity of the active polymer layer were not compromised by the polymer/SBT interface. Similar threshold-voltage and mobility values were also obtained for devices with 4-μm and 12-μm channel lengths.

Overall, our data indicate significantly improved performance for transistors with SBT gate dielectric as compared to transistors with SiO_2 gates [7]. For example, our transistors exhibited an on/off ratio of around 10^4 with a V_g sweep from −4 V to +4 V, whereas similar devices with SiO_2 gates utilized gate voltages as high as −100 V and 40 V [7]. Furthermore, our transistors possess threshold voltages of around 0.64 V, as compared to 5.8 V for transistors with SiO_2 gates [7]. Such an enhancement in gate effect can be explained by the fact that SBT films have a much higher dielectric constant ($\varepsilon = 50$) than SiO_2 ($\varepsilon = 3.9$), which leads to a ten-fold difference in the gate dielectric capacitance C_i and results in much stronger gate effects for devices employing SBT gates. A similar reduction in V_d is also present: −10 V for our devices, as compared to −100 V for devices with SiO_2, partly due to a small channel length (2 μm) used in our transistors.

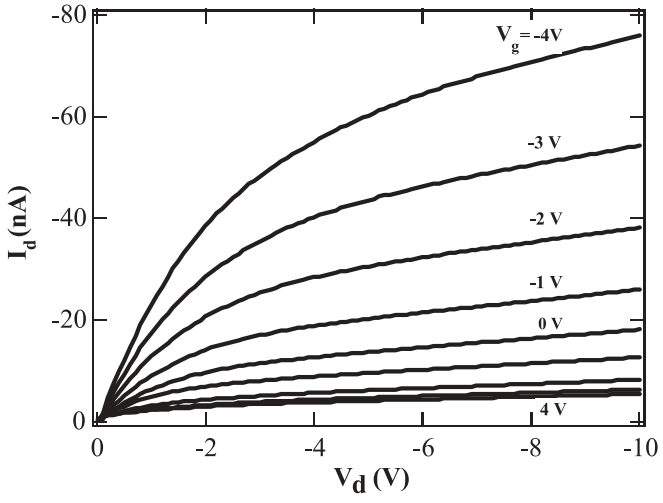

FIGURE 2 $I_d - V_d$ characteristics of the polymer transistor exhibiting low operation voltages. The gate bias varies from −4 V to +4 V with 1-V increment from the *top curve* to the *bottom curve*. The channel width is 500 μm and the channel length is 2 μm for this device

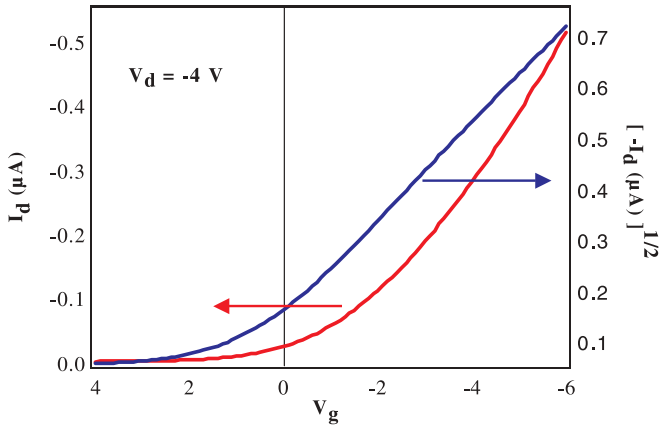

FIGURE 3 Transfer characteristics of the polymer transistor: $I_d - V_g$ shown as the *red line* and $(-I_d)^{1/2} - V_g$ shown as the *blue line*. The threshold voltage and the mobility can be derived

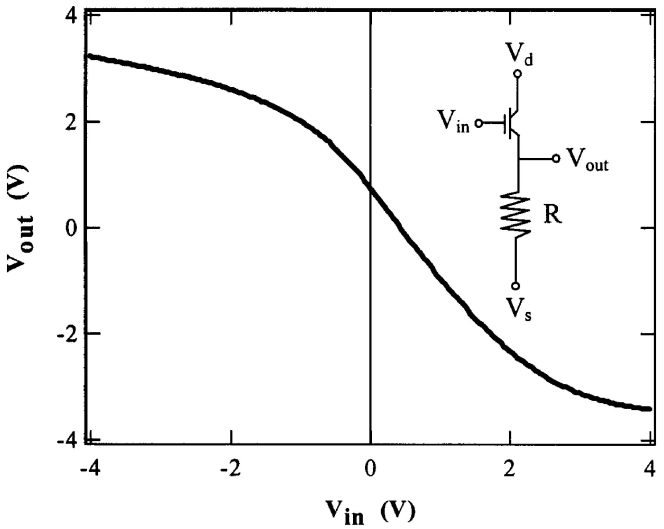

FIGURE 4 Input–output characteristics of the polymer-based inverter with the circuit diagram shown in the *inset*

Such low operating voltages for both V_g and V_d render our transistors particularly useful for a wide range of applications such as active-matrix flat-panel displays, smart cards, sensor arrays and even flexible microelectronic logic circuits, where low voltage supply, sometimes powered by batteries, is highly desirable. Based on this *p*-type field-effect transistor we have demonstrated a *p*-type field-effect inverter with low operating voltages. As shown in Fig. 4, a resistor was used as the load for the *p*-type transistor, the gate bias was used as the input and the voltage drop across the resistor was used as the output. When the input was low (−4 V, logic '0'), the *p*-type transistor was turned on and the output was high (logic '1'). On the other hand, when the input was high (4 V, logic '1'), the *p*-type transistor was turned off and the output was low (logic '0'). A detailed input–output transfer curve is shown in Fig. 4, clearly demonstrating the inverter operation with voltages as low as 4 V. A voltage gain of ∼ 1.5 was observed when the input voltage is around 0 V. Work toward demonstrating other types of logic gates with low operating voltages is currently under way.

In summary, due to the high dielectric constant of SBT films, our polymer transistors employing SBT as the gate insulator showed much stronger gate effects than devices made with SiO_2. Our devices exhibited low operating voltages, high on/off ratios and good mobility values, leading to the successful demonstration of polymer-based inverters with operation voltages around a few volts. Our technique can also be used to yield low operating voltages for other organic field-effect devices.

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