Carbon nanotube field-effect inverters

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This letter presents *p*-type metal–oxide–semiconductor (PMOS) and complementary metal–oxide–semiconductor (CMOS) inverters based on single-walled carbon nanotube field-effect transistors. The device structures consist of carbon nanotubes grown via a chemical-vapor deposition method and contacted by two metallic source/drain electrodes. Electrical properties of both *p*-type (without doping) and *n*-type nanotube transistors with potassium doping have been measured. By utilizing a resistor as the load for a *p*-type nanotube field-effect transistor, a PMOS inverter is demonstrated. Furthermore, by connecting a *p*-type nanotube transistor and an *n*-type nanotube transistor, a CMOS inverter is demonstrated. Both types of inverters exhibit nice transfer characteristics at room temperature. Our work represents one step forward toward integrated circuits based on nanoelectronic devices. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1417516]

The electronic properties of single-walled carbon nanotubes (SWNTs) have been extensively studied throughout the last decade.[1–8] Various fabrication approaches have been developed to address individual single-walled carbon nanotubes, such as depositing SWNTs from liquid suspensions onto prefabricated nanoelectrodes[4,5,8] or onto flat substrates followed by patterning electrodes.[6,7] These techniques have resulted in remarkable success in producing individual isolated devices such as single-electron transistors[4–6] and field-effect transistors (FETs);[5–8] however, there is a lack of control over the location and orientation of deposited nanotubes, and hence, producing integrated systems is almost impossible with these techniques. In contrast, the recently developed chemical-vapor deposition (CVD) technique[9–11] has great potential in producing integrated systems because of its control on the position and orientation of as-grown nanotubes. Recent effort with this technique has yielded a lot of interesting devices such as chemical sensors,[12] mechanical switches,[13] and $p-n$ junctions.[14]

Inspired by the above-mentioned success, we have decided to exploit the unique advantage of the CVD technique to demonstrate small integrated nanotube systems, i.e., logic gates. This letter reports our effort on building nanoscale inverters, a basic unit of digital circuits, by using SWNTs. A *p*-type metal–oxide–semiconductor (PMOS) inverter is demonstrated by connecting a load resistor to a *p*-type nanotube FET, which consists of a CVD-grown individual single-walled nanotube with metallic source/drain electrodes and the silicon substrate backgate. Further integration of this *p*-type nanotube FET with an *n*-type nanotube FET produced by potassium-vapor doping[15–17] leads to the demonstration of a more sophisticated complementary metal–oxide–semiconductor (CMOS) inverter.

All the SWNT devices used in this study were prepared with patterned chemical-vapor deposition and microfabrication for the source/drain contacts.[9,10] The core of this fabrication approach involves depositing catalytic nanoscale iron particles onto a patterned Si/SiO_2 substrate, followed by growth of SWNTs out of these iron particles at 900 °C with CH_4 as the feeding gas. Therefore, the location of the as-grown carbon nanotubes is determined by the location of the catalyst islands. As the last fabrication step, e-beam lithography and metallization are utilized to deposit two Ni/Au electrodes, each covering one end of the nanotube and serving as the source/drain electrodes, while the degenerately *p*-doped silicon substrate is used as the gate electrode. A diagram of a finished device and an atomic-force microscopy (AFM) image are shown in Fig. 1. The dimensions of the SWNTs used in this study are about 500 nm in length and 2 nm in diameter, derived from topographic atomic-force microscope images.

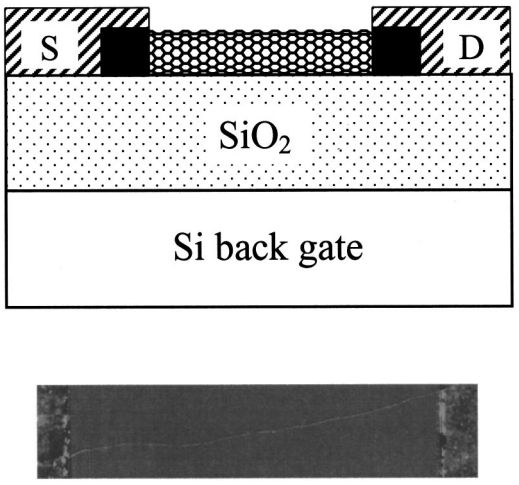

FIG. 1. (a) Schematic diagram of the carbon nanotube transistors used in this study. The nanotube is grown bridging the catalyst islands (black squares) via a CVD technique. (b) AFM image of a typical device. The transistor channel length is 500 nm, as defined by the distance between the left and right metallic electrodes.

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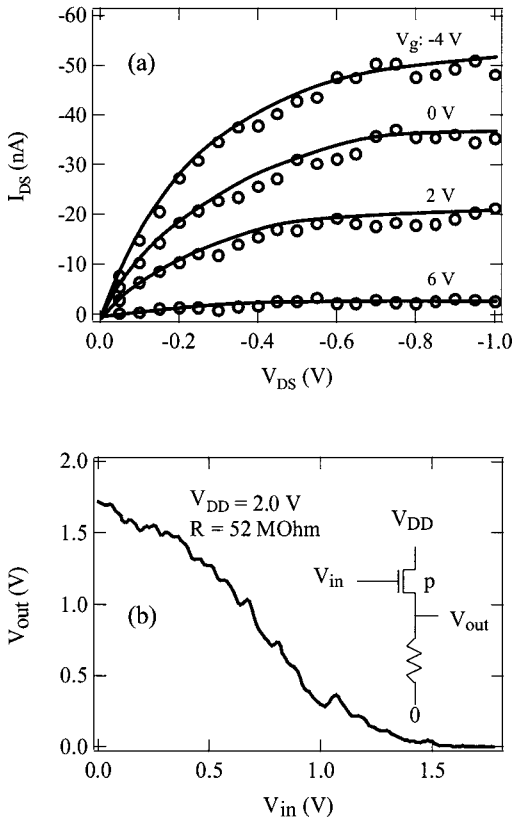

FIG. 2. (a) $I-V$ characteristics of a typical *p*-type nanotube field-effect transistor showing both linear and saturation regimes. (b) Transfer characteristics of a PMOS inverter. Inset: schematic diagram of the PMOS inverter.

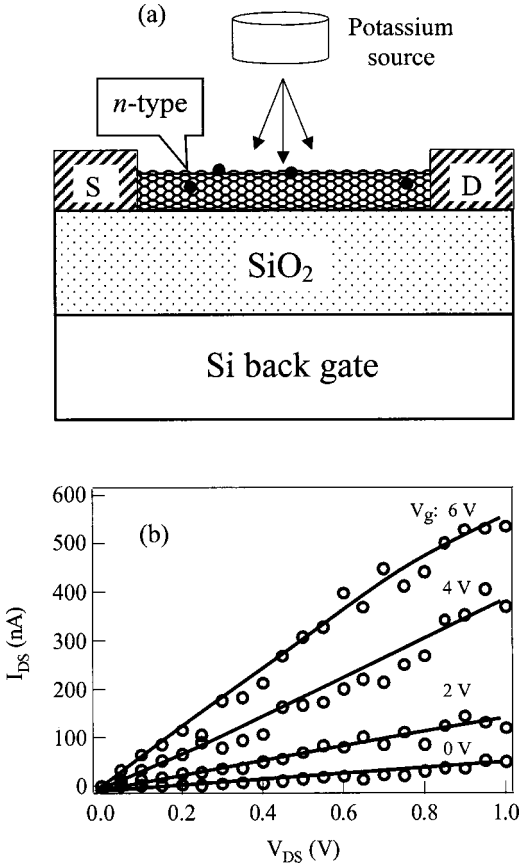

FIG. 3. (a) Schematic diagram of the potassium doping setup. (b) $I-V$ characteristics of a potassium-doped nanotube transistor showing *n*-type behavior.

$I-V$ characteristics of a typical device made this way are shown in Fig. 2(a). This device shows high conductance under negative gate bias and displays almost no conduction with a gate bias of 6 V, indicating a *p*-type doped nanotube, consistent with previous observations.[5,8,11] The $I-V$ curves are similar to those of the conventional silicon MOSFET, with a well-defined linear regime under small source–drain bias and a saturation regime at high bias. This is also consistent with our previous observation,[11] and a detailed explanation can be found there. By comparing the data with the standard metal–oxide–semiconductor field-effect transistor model, we find the transconductance of this device to be in a range of 3.7–5.0 nS at 1.0 V source–drain.

Based on this nanotube transistor, an inverter can be readily constructed to output logic ''1'' when the input is ''0'' and the output ''0'' when the input is ''1.'' As shown in the Fig. 2(b) inset, a resistor is connected between ground and the source of this nanotube device, while a bias of 2.0 V is supplied to the drain. The silicon gate is used as the input while the potential of the output electrode is monitored. As shown in Fig. 2(b), when the input voltage is swept from 0 to 2 V, the output varies from 1.7 to almost 0 V, working just like an inverter. When the input is low, i.e., logic 0, the *p*-type transistor is on, and hence, most of V_{DD} is dropped across the resistor, leading to a high output, i.e., logic 1. On the other hand, as we increase the gate bias from 0 to 2.0 V, the nanotube transistor is gradually turned off and becomes increasingly resistive. Consequently, more and more voltage is dropped across the nanotube instead of the load resistor and eventually the output voltage is almost 0, fulfilling the function of an inverter. In our experiment, the inverter turns on (logic 1) at 0 V and turns off at 1.5 V and a gain of about 1 has been measured. Furthermore, since the voltage ranges of input and output are almost the same, these inverters can be integrated in a cascade manner without malfunctioning.

Despite the proper functioning of the above-mentioned system, it does not stand as an integrated system since an external resistor is used. In addition, PMOS inverters are inferior to CMOS inverters when power consumption, stability, and noise suppression are considered.[18] Therefore, we decided to pursue complementary inverters by integrating a *p*-type nanotube transistor with an *n*-type nanotube transistor. *N*-type nanotube transistors are obtained by doping a nanotube with potassium vapor, following previous effort.[17] The underlying mechanism is that electron transfer from adsorbed potassium atoms to the nanotube can shift the Fermi level of the tube from the valence-band edge to the conduction-band edge, thus reverting the doping from *p* to *n* type. The schematic of our setup is shown as Fig. 3(a). The doping is carried out by heating up a Saes-getter potassium source placed 2 cm away underneath the sample in a vacuum of 1×10^{-5} Torr. The duration of this doping process is about 3 h, and details can be found in earlier publications.[17] Figure 3(b) shows $I-V$ characteristics of a typical *n*-type nanotube transistor obtained this way. The conductance is found to increase under positively increasing gate bias, going from 34 nS at $V_g=0$ V to 600 nS at $V_g=6$ V. This kind of behavior is the signature of *n*-type field-effect transistors. Interestingly, $I-V$ curves of this device are rather linear as

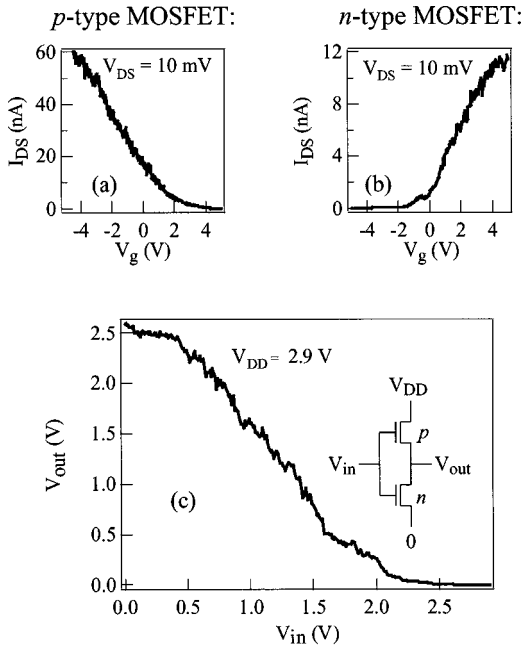

FIG. 4. (a) $I-V_g$ curve for a *p*-type nanotube transistor. (b) $I-V_g$ curve for an *n*-type nanotube transistor. (c) Transfer characteristics of a CMOS nanotube inverter constructed by connecting the *p*-type transistor with the *n*-type transistor.

compared to the saturated $I-V$ curves in Fig. 2. The origin of such a difference is not fully understood at this moment.

Combining *p*- and *n*-type transistors, complementary field-effect inverters can be easily demonstrated. We utilize two separate nanotube transistors connected in series with an electric lead about 2 mm in length. One nanotube transistor is exposed to the potassium vapor and hence doped into *n* type, while the other is hidden from the potassium vapor and remains *p* type. Details of this process can be found in our previous publications.[14] Figures 4(a) and 4(b) display the $I-V_g$ characteristics of *p*- and *n*-type nanotube transistors, respectively. Under a source–drain bias of 10 mV, the *p*-type nanotube exhibits substantial conduction (17 nA) at $V_g=0$ V and little conduction with V_g beyond 2.5 V, the signature of a depletion-mode *p*-type transistor. On the contrary, the *n*-type nanotube transistor displays little conduction around $V_g=0$ V and significant conduction with $V_g>2.5$ V, indicating an enhancement-mode *n*-type transistor. These two devices are then biased in the configuration depicted in the Fig. 4(c) inset. We applied a 2.9 V bias to the V_{DD} terminal and swept the gate electrode (input) from 0 V (defined as logic 0) to 2.5 V (defined as logic 1), and the transfer characteristic curve is shown in Fig. 4(c). When the input voltage is low (logic 0), the *p*-type transistor is on, meaning the conductance is high, and the *n*-type transistor is off, meaning the conductance is low. As a result, the output of this inverter is close to V_{DD}, thereby producing an output of logic 1. As the input voltage is increased, the conductance of the *p*-type nanotube increases and the conductance of the *n*-type nanotube decreases, leading to a decreasing output voltage. With sufficiently high input, the *p*-type nanotube is turned off, whereas the *n*-type nanotube is on. The combined effect is an output voltage close to the ground, i.e., logic 0, as clearly demonstrated in our experiment. Our results show that the output starts to decrease at $V_{in}=0.4$ V and is cutoff at $V_{in}=2.0$ V, leading to a gain as high as 1.7. Thus far, the operation of a CMOS nanotube inverter is fully demonstrated, though an ideal inverter should exhibit a stepwise V_{out} vs V_{in} behavior, whereas our results in Figs. 2 and 4 show a small flat region at low and high values of V_{in} with almost a linear variation in between. The observed behavior may be due to the *p*-MOS tube transistor being somewhat leaky, and the threshold control for both transistors not being perfect, all of which reflects the fabrication difficulties in nanoelectronics at this early stage. An additional drawback is that the system must be kept in vacuum because of the potassium doping used. Further advances should involve development of doping methods that are stable in ambient atmosphere.

In summary, we have demonstrated both PMOS and CMOS inverters based on carbon nanotubes. Although the PMOS inverter requires an external load resistor, the CMOS inverter represents a rudimental integrated system by connecting a *p*-type nanotube transistor with an *n*-type nanotube transistor. Both types of inverters can function at room temperature and possess gains equivalent to or greater than 1. Our work demonstrates the advantage of the CVD growth technique and should stimulate more effort toward integrated nanoelectronic systems.

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