

Electrical measurements of individual semiconducting single-walled carbon nanotubes of various diameters

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(Received 28 October 1999; accepted for publication 28 January 2000)

Individual semiconducting single-walled carbon nanotubes (SWNTs) of various diameters are studied by electrical measurements. Transport through a semiconducting SWNT involves thermal activation at high temperatures, and tunneling through a reverse biased metal–tube junction at low temperatures. Under high bias voltages, current–voltage (I – V) characteristics of semiconducting SWNTs exhibit pronounced asymmetry with respect to the bias polarity, as a result of local gating. SWNT transistors that mimic conventional p -metal-oxide-semiconductor field-effect transistor with similar I – V characteristics and high transconductance are enabled. © 2000 American Institute of Physics. [S0003-6951(00)04612-X]

Carbon nanotubes are molecular wires exhibiting intriguing electrical, mechanical, and chemical properties.^{1–3} Single-walled nanotubes (SWNT) are ideal systems for studying the physics in quasi-one-dimension.^{1,4–6} Previous approaches to addressable SWNT electrical architectures include depositing SWNTs from liquid suspensions onto pre-defined electrodes,^{7–9} or onto a flat substrate followed by locating nanotubes and patterning electrodes.^{10,11} Results obtained with individual single-walled tubes and ropes include Coulomb charging^{7,10,11} and Luttinger liquid behavior¹² in metallic tubes. Semiconducting SWNTs were found to exhibit field-effect transistor-like characteristics at room temperature.^{8,9}

A recently developed SWNT synthetic method allowed the growth of individual tubes at controlled sites on surfaces,¹³ and led to a new approach to obtain large numbers addressable SWNTs for systematic studies of various classes of nanotubes.^{14,15} The current work focuses on elucidating the electrical properties of individual SWNTs that are semiconducting in nature. We present temperature dependent transport characteristics of individual semiconducting SWNTs of various tube diameters. Transport mechanisms through semiconducting SWNTs at various temperatures are elucidated. SWNT transistors exhibiting current–voltage (I – V) characteristics resembling that of silicon based p -metal-oxide-semiconductor field-effect transistor (MOSFET) are obtained, with transconductance two orders of magnitude higher than previous nanotube transistors.

Sample preparation for metal/individual SWNT/metal samples involved patterned chemical vapor deposition growth and microfabrication for metal-tube electrical contacts.^{13–15} Results presented in this letter were obtained with SWNTs contacted by 20-nm-thick nickel electrodes with 60-nm-thick gold on top. The lengths of the SWNTs between electrodes were $\geq 3 \mu\text{m}$. Degenerately doped silicon wafers with 500-nm-thick thermally grown oxide on the surface were used as the substrates. The heavily doped substrate is conducting at low temperatures and was used as a back gate. Figure 1 shows tapping mode atomic force mi-

croscopy (AFM) images of individual SWNTs in two samples. The diameters of SWNTs were determined from AFM topographic height data.

I – V curves obtained at room temperature with sample No. 1 are shown in Fig. 2(a). The nanotube has a relatively large diameter of $2.8 \pm 0.1 \text{ nm}$ and exhibits a highly linear I – V curve with resistance $\sim 340 \text{ k}\Omega$ measured at zero gate voltage (V_g). Positive gate voltages progressively reduce the linear conductance of the sample [Fig. 2(a)]. At $V_g > 3 \text{ V}$, the conductance is suppressed by four orders of magnitude from that at $V_g = 0$. These I – V characteristics are signatures of hole-doped semiconducting SWNTs acting as p -type “transistors” as reported by previous work.^{8,9,14,15} When the gate voltage is further increased, the conductance of the sample remains suppressed until the gate voltage reaches $\sim 40 \text{ V}$ where appreciable recovery in the conductance is observed [Fig. 2(a) inset].

The zero-gate linear resistance versus temperature curve for the $d = 2.8 \text{ nm}$ semiconducting tube is shown in Fig. 2(b) inset. The resistance increases from $340 \text{ k}\Omega$ to $1 \text{ M}\Omega$ as temperature is lowered from 300 to 25 K . Below 25 K , the temperature dependent resistance can be fitted into $\sim \exp(-E_a/K_B T)$ with $E_a \sim 4.6 \text{ meV}$ [solid line in Fig. 2(b) inset]. At 4 K , a gap $\sim 20 \text{ mV}$ is observed in the I – V curve and the sample is insulating in the bias range $|V| < \sim 10 \text{ mV}$ under zero gate voltage [Fig. 2(b)]. The insulating region is found to be significantly suppressed by applying a -1.5 V gate voltage. Applying a positive gate voltage [e.g., $V_g = +1 \text{ V}$ in Fig. 2(b)] leads to a larger insulating region in the I – V curve.

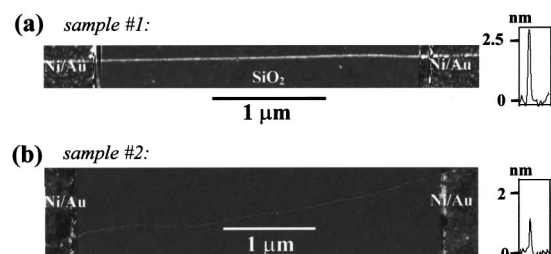


FIG. 1. (a) AFM image of sample No. 1 consisting of a $d \approx 2.8 \text{ nm}$ SWNT. (b) AFM image of sample No. 2, the SWNT diameter $\approx 1.3 \text{ nm}$.

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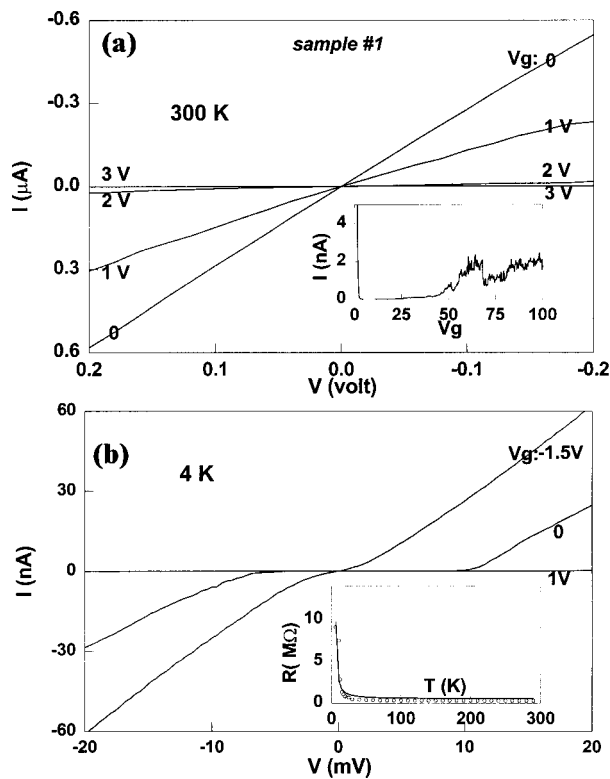


FIG. 2. (a) Room temperature I - V curves of sample No. 1. Inset: current vs gate voltage recorded at 300 K under a 10 mV bias voltage. (b) I - V curves under $V_g = -1.5, 0,$ and $+1$ V at 4 K. Inset: R vs T . Solid line shows the $\exp(-E_a/K_B T)$ fit.

The results obtained with sample No. 1 are interpreted as the following. First, the nanotube is suggested to be hole doped along its entire length. Second, each contact is suggested to consist of a serial resistance and a junction formed with the p -type nanotube bridge. The junction formation arises from the separation between the nanotube Fermi level and the valence band $E_{FV} = E_F - E_V$ and sets a barrier to electron transport.

The junction barrier is responsible for the observed thermally activated transport shown in Fig. 2(b), and is determined to be $E_a \sim 4.6$ meV for sample No. 1 from the temperature dependent linear resistance data. Positive gate voltages cause the valence band shifting down away from the Fermi level, leading to higher barriers and thus less conducting states as seen in Fig. 2(a). At 4 K where $K_B T \ll E_a \sim 4.6$ meV, thermally activated transport through the system is quenched. The sample is in an insulating state near zero bias as seen in Fig. 2(b). For bias voltages $|V| > \sim 10$ mV, the sample is turned into a conducting state. Analyses of the I - V curve after the turn-on find that current increases by approximately three orders of magnitude in the bias range of 7–14 mV, and can be fitted into $I \sim \exp(-c/V)$ where c is a constant. These results suggest that electron transport at 4 K is via a tunneling mechanism. Under a sufficiently high bias voltage V , electron tunneling occurs through a reverse biased junction. Similar transport mechanisms were reported in conventional metal–semiconductor–metal systems by Lepselter and Sze.¹⁶

The observed conductance recovery suggests that high positive gate voltages convert the sample into an n -type system from p type, with further increase in gate voltage en-

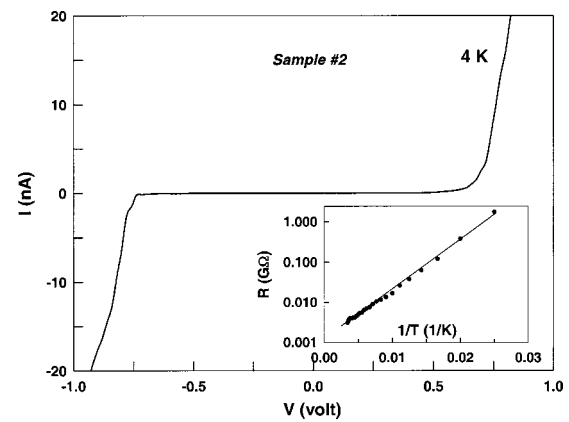


FIG. 3. I - V curve recorded at 4 K with sample No. 2 ($V_g = 0$). Inset: R (in log scale) vs $1/T$.

hances the conductance of the n -type system. The band gap can be estimated to be on the order of $E_g \sim 150$ meV,¹⁷ compared to the theoretically expected $E_g \approx 200$ meV for the $d = 2.8$ nm semiconducting tube.¹

Figure 3 shows the results obtained with sample No. 2 consisting of a semiconducting SWNT with $d = 1.3 \pm 0.1$ nm and length $\sim 5 \mu\text{m}$. Linear resistance of the sample is ~ 3.4 M Ω at room temperature, and increases upon cooling according to $\sim \exp(-E_a/K_B T)$ with $E_a \approx 25$ meV (Fig. 3 inset). At 4 K, an insulating gap is observed within $\sim \pm 0.6$ V in the I - V curve shown in Fig. 3. Within our model, the junction barrier height is $E_a = E_{FV} \sim 25$ meV, which is comparable to the room temperature thermal energy. Note the expected energy gap for the $d \sim 1.3$ nm tube $E_g \sim 0.6$ eV.¹ Beyond the insulating gap in I - V , the current is found to increase by three orders of magnitude when the bias is increased from 0.5 to 0.9 V, which points to the tunneling transport mechanism described earlier. Because of a higher junction barrier than that in sample No. 1, the small diameter tube sample requires much higher bias voltage to establish significant tunneling currents through the reverse biased junction.

We found that at room temperature and zero gate voltage, the resistance of semiconducting SWNTs were typically in the range of 160–500 k Ω for tube diameters > 2.0 nm. The resistance of smaller diameter SWNTs with $d \leq 1.5$ nm were typically on the order of megahms or higher. Hole doping to larger diameter tubes led to smaller E_{FV} and thermal activation barriers, as found by temperature dependent measurements. The lower resistance for larger diameter semiconducting SWNTs can be attributed to the lower transport barrier at the metal–tube junctions, and better electrical coupling may have been made with larger diameter tubes and contributed to their low resistance. For small diameter tubes, we observed no conductance recovery under gate voltages up to $+100$ V. This can be attributed to the large energy gaps (≥ 0.6 eV) relative to the gate efficiency and large band bending effects at the junctions.

All of our semiconducting nanotube samples exhibit an interesting feature in the I - V curves under high bias voltages. The I - V curves show remarkable asymmetry with respect to the polarity of the bias voltage when $|V| > \sim 1$ V. I - V curves obtained at room temperature with sample No. 1 over a bias range of 3 to -3 V are shown in Fig. 4. In the

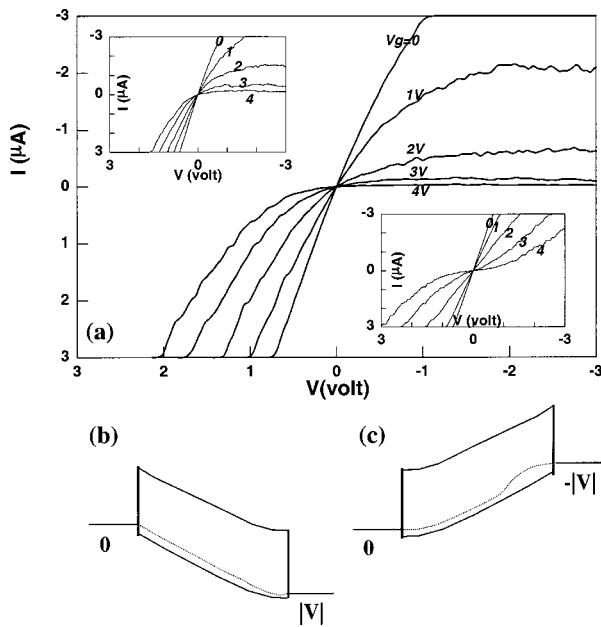


FIG. 4. (a) I - V curves recorded at 300 K with sample No. 1 for $V = 3$ to -3 V. Left inset: I - V curves recorded after exchanging the source-drain electrodes. Right inset: symmetrical I - V curves obtained under symmetrical bias. (b), (c) Band diagrams for positive and negative drain bias, respectively.

negative bias side, the current initially scales linearly as $|V|$ but reaches saturation and stays constant under large negative biases. In the positive bias side, the current increases continuously as the bias voltage increases. The asymmetry in I - V is found to be independent of which metal electrode is ground (source) or biased (drain). Data recorded after exchanging the source and drain electrodes show nearly unchanged asymmetry in I - V (Fig. 4 left inset). Symmetrical I - V curves can be obtained (Fig. 4 right inset) under symmetrical bias by scanning V in the range of -3 to 3 V while biasing the two electrodes at $-V/2$ and $+V/2$ respectively. These results suggest that the observed asymmetrical I - V curves are not caused by asymmetrical parameters such as different contact resistances at the two metal-tube interfaces, but are inherent to the metal/tube/metal system.

The I - V asymmetry in bias polarity was consistently observed in all of the six independent semiconducting SWNT samples studied. We suggest that the origin of this asymmetry is local gating of the biased drain electrode. Under a given positive gate voltage (e.g., $V_g = 2$ V), the nanotube can be considered to have a constant hole density along its length. In a negative bias configuration $[0, |V|]$ (e.g., $|V| = 3$ V), the quasi-Fermi level¹⁸ shown as dotted line in Fig. 4(c) of the nanotube is further away from the valence band near the drain where the local gating voltage is more positive relative to the drain. This results in a reduced hole density in the tube section near the drain and thus reduced conductance. Saturation occurs for large $|V|$ because of the competing roles of driving and gating of the drain bias voltage. This phenomenon can be related to local carrier depletion and channel pinch-off by negative drain bias in a conventional p -type MOSFET.¹⁸ In a positive bias configuration $[0, |V|]$, local hole enrichment is induced in the nanotube section near the drain where the quasi-Fermi level is closer to the valence

band as shown in Fig. 4(b), which results in a more conducting system.

The results presented in this letter are significant in terms of enabling high performance nanotube transistors. First, the I - V curves of our samples resemble those of conventional p -MOSFET.¹⁸ Second high voltage gain and transconductance are obtained with our devices. Sample No. 1 shown in Fig. 2 exhibits positive voltage gain of $\Delta V_{ds}/\Delta V_g|_{I=3\mu A} \sim 3$ compared to the maximum gain of ~ 0.35 obtained previously.⁸ A transconductance of $\partial I_{ds}/\partial V_g|_{V=100\text{ mV}} \sim 200$ nA/V is obtained with this sample, which is two orders of magnitude higher than previous results with SWNTs.⁹ Transconductance normalized by the tube width is ~ 0.1 mS/ μm , which is comparable to silicon based p -MOSFETs. Three independent SWNTs with diameters in the range of 2.5–3 nm are found to exhibit high transconductance between 100 and 200 nA/V. The high transconductance is a direct result of the low linear resistance of these samples (hundreds of k Ω). Samples consisting of small diameter tubes ($d < 1.5$ nm) exhibit lower transconductance in the range of 1–10 nA/V because of their high resistance ($>$ several M Ω).

In summary, we presented detailed results of electron transport measurements of individual semiconducting SWNTs. Transport in semiconducting SWNT samples involves thermal activation at high temperatures and tunneling through a reverse biased metal-tube junction at low temperatures. Electrical properties of SWNTs with various diameters are elucidated. Local gating effects lead to a bias polarity associated transport phenomenon and high transconductance SWNT transistors.

H. D. acknowledges support by NSF, LAM at Stanford, DAPRA/ONR, SRC, ACS, and the Camille Henry-Dreyfus Foundation.

¹M. S. Dresselhaus, G. Dresselhaus, and P. C. Eklund, *Science of Fullerenes and Carbon Nanotubes* (Academic, San Diego, 1996).

²B. I. Yakobson and R. E. Smalley, *Am. Sci.* **85**, 324 (1997).

³C. Dekker, *Phys. Today* **52**, 22 (1999).

⁴C. Kane, L. Balents, and M. P. A. Fisher, *Phys. Rev. Lett.* **79**, 5086 (1997).

⁵C. L. Kane, E. J. Mele, R. S. Lee, J. E. Fischer, P. Petit, H. Dai, A. Thess, R. E. Smalley, A. R. M. Verschuere, S. J. Tans, and C. Dekker, *Europhys. Lett.* **6**, 683 (1998).

⁶C. L. Kane and E. J. Mele, *Phys. Rev. Lett.* **78**, 1932 (1997).

⁷S. J. Tans, M. H. Devoret, H. J. Dai, A. Thess, R. E. Smalley, L. J. Geerligs, and C. Dekker, *Nature (London)* **386**, 474 (1997).

⁸S. Tans, A. Verschuere, and C. Dekker, *Nature (London)* **393**, 49 (1998).

⁹R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, *Appl. Phys. Lett.* **73**, 2447 (1998).

¹⁰M. Bockrath, D. H. Cobden, and P. L. McEuen, *Science* **275**, 1922 (1997).

¹¹D. H. Cobden, M. Bockrath, P. L. McEuen, A. G. Rinzler, and R. E. Smalley, *Phys. Rev. Lett.* **81**, 681 (1998).

¹²M. Bockrath, D. H. Cobden, J. Lu, A. G. Rinzler, R. E. Smalley, T. Balents, and P. L. McEuen, *Nature (London)* **397**, 598 (1999).

¹³J. Kong, H. Soh, A. Cassell, C. F. Quate, and H. Dai, *Nature (London)* **395**, 878 (1998).

¹⁴H. T. Soh, C. F. Quate, A. F. Morpurgo, C. M. Marcus, J. Kong, and H. J. Dai, *Appl. Phys. Lett.* **75**, 627 (1999).

¹⁵J. Kong, C. Zhou, A. Morpurgo, H. T. Soh, C. F. Quate, C. Marcus, and H. Dai, *Appl. Phys. A: Solids Surf.* **69**, 305 (1999).

¹⁶M. P. Lepselter and S. M. Sze, *Proc. IEEE* **56**, 1400 (1968).

¹⁷A conversion factor between the band energy shift ΔE and the gate voltage ΔV_g is estimated to be ~ 3 meV/V using a method described in Ref. 10.

¹⁸S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).