Fabrication of fully transparent nanowire transistors for transparent and flexible electronics

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The development of optically transparent and mechanically flexible electronic circuitry is an essential step in the effort to develop next-generation display technologies, including 'see-through' and conformable products. Nanowire transistors (NWTs) are of particular interest for future display devices because of their high carrier mobilities compared with bulk or thin-film transistors made from the same materials, the prospect of processing at low temperatures compatible with plastic substrates, as well as their optical transparency and inherent mechanical flexibility. Here we report fully transparent In_2O_3 and ZnO NWTs fabricated on both glass and flexible plastic substrates, exhibiting high-performance n-type transistor characteristics with ~82% optical transparency. These NWTs should be attractive as pixel-switching and driving transistors in active-matrix organic light-emitting diode (AMOLED) displays. The transparency of the entire pixel area should significantly enhance aperture ratio efficiency in active-matrix arrays and thus substantially decrease power consumption.

In view of the inherent limitations of silicon-based electronic circuits and the demand for portable display/communication/computational/identification products, the development of high-performance transparent devices is the focus of much activity. The availability of optically transparent and mechanically flexible electronic circuitry could open the door to next-generation display technologies, including 'see-through' and conformable products.

Poly-silicon thin-film transistors (poly-Si TFTs) and amorphous-silicon thin-film transistors (α-Si TFTs) are widely used to fabricate commercial displays[1–3], but their lack of transparency limits their utility in transparent device applications. In this regard, recent transparent transistor research efforts have focused on enhancing transparency and flexibility while maintaining or enhancing key TFT performance metrics. There have been several recent reports of transparent transistors fabricated with ZnO, SnO_2, In_2O_3 or other semiconducting oxide thin films, or with carbon nanotube networks as the active channel layers and opaque source and drain metals, or with carbon nanotube films and transparent source/drain electrodes[4–11]. However, there have been no reports of fully transparent oxide nanowire transistors (NWTs) fabricated with all-transparent gate and source/drain electrodes and displaying high transistor performance.

In_2O_3 and ZnO nanowires are particularly promising candidates for transistor active channels satisfying these requirements because they are both transparent and mechanically robust/flexible. Furthermore, indium-tin oxide (ITO) and indium-zinc oxide (IZO) are attractive transparent conductors for gate and source/drain electrodes[12–14]. In addition to transparency, transistor performance metrics such as high on-current (I_{on}), high on/off current ratio (I_{on}/I_{off}), high field-effect mobility (μ_{eff}), steep subthreshold slope (S) and small threshold voltage (V_T) variation during transistor operation are required to realize commercially viable logic circuits and display devices.

Recent studies of NWTs have reported stable, high-performance transistor characteristics rivalling or surpassing those of α-Si and poly-Si TFTs, especially for μ_{eff} and S (refs 15–18). The mobility observed in the present study exceeds the typical bulk mobility[19] reported for In_2O_3 as well as the reported mobility[9] in transparent In_2O_3 thin-film transistors. Similar phenomena, that is, nanowire mobilities exceeding bulk mobilities, have been reported in a number of materials[16–18]. Although the exact mechanisms for this are not completely clear, the quasi-one-dimensional nature of nanowires may play a significant role in terms of reducing low-angle carrier scattering[20–24]. The use of preformed nanowires allows low-temperature device processing, which is essential for applications such as circuits fabricated on plastic substrates.

The present results build on recent NWT studies indicating that the desired semiconductor properties can be achieved and that post-treatments such as ozone and electrical stressing further enhance device performance[25]. Here, we report fully transparent NWTs fabricated using all-transparent In_2O_3 and ZnO nanowire active channels, Al_2O_3 gate insulators, ITO source/drain electrodes and IZO gate electrodes. The representative In_2O_3

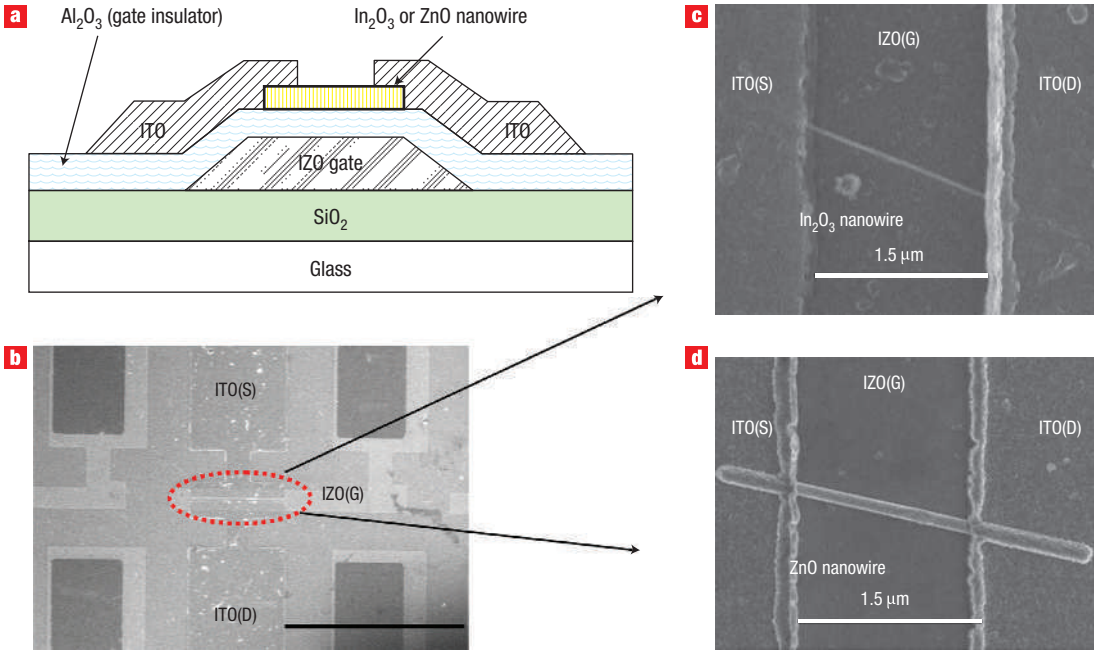

Figure 1 Fully transparent NWTs. a, Cross-sectional view of fully transparent NWT device structures consisting of a SiO_2 buffer layer (500 nm), patterned IZO gate electrode (120 nm), ALD-deposited Al_2O_3 gate insulator (18 nm), a single In_2O_3 nanowire ($D \sim 20$ nm) or ZnO nanowire ($D \sim 120$ nm) for the active channel, and ITO for the source/drain electrodes (120 nm). **b**, Top-view FE-SEM images of the devices. The IZO gate overlaps with the ITO source/drain electrodes to improve transistor performance with coverage all nanowire channel. Scale bar represents 100 μm. **c**, Top-view SEM of a single In_2O_3 nanowire region ($D/L \sim 20$ nm/1.80 μm). Scale bar represents 1.5 μm. **d**, Top-view SEM of a single ZnO nanowire region ($D/L \sim 120$ nm/1.66 μm). Scale bar represents 1.5 μm.

NWTs on glass substrates exhibit n-type transistor characteristics with ~82% visible transparency, and μ_{eff} varies from approximately 514 to 300 $cm^2\,V^{-1}\,s^{-1}$ as the gate bias is increased from 0 V to 2 V. The representative ZnO NWTs on glass substrates exhibit ~83% visible transparency, with μ_{eff} varying from ~96 to 70 $cm^2\,V^{-1}\,s^{-1}$ over the gate bias range of 0–3 V. Fully transparent and mechanically flexible In_2O_3 NWTs with optical transmission of ~81% are also fabricated on PET plastic substrates, with $\mu_{eff} \approx 120$–167 $cm^2\,V^{-1}\,s^{-1}$ over the reported gate bias range. We show here that the excellent transparency and semiconducting properties of In_2O_3 and ZnO nanowires combined with Al_2O_3 as the gate insulator, and with ITO and IZO contacts, affords high-performance NWTs that are attractive candidates for future flexible transparent display applications.

EXPERIMENTAL RESULTS AND DISCUSSION

A cross-sectional view of the fully transparent NWT structure with an individually addressed bottom gate is shown in Fig. 1a. The structure consists of a SiO_2 buffer layer, a patterned IZO gate electrode, an atomic layer deposition (ALD)-derived high-κ Al_2O_3 gate insulator, a single-crystal semiconducting In_2O_3 (ref. 26) or ZnO (ref. 27) nanowire for the active channel, and ITO for the source/drain electrodes. No further passivation layers are used, so the dielectric above the nanowire is air. Figure 1b shows a top view of an NWT device, including all transparent components. Field-emission scanning electron microscope (FE-SEM) images of single In_2O_3 and ZnO nanowires between source and drain electrodes are shown in Fig. 1c,d, respectively. The corresponding nanowire diameters and lengths (D/L) of single In_2O_3 or ZnO nanowires addressed between source and drain on the glass substrates are 20 nm/1.80 μm and 120 nm/1.66 μm, respectively.

Figure 2a shows the gate and drain leakage currents of a representative In_2O_3 NWT device for the bias configurations shown in the inset. Note that the drain leakage current here is the summation of the body current leakage of the In_2O_3 nanowire (~40 pA at 2 V) and the leakage current through the gate dielectric (~1 pA at 2 V). The Al_2O_3 gate dielectric exhibits excellent insulating properties, with an electrical breakdown field of >8 MV cm^{-1} (ref. 28) and a dielectric constant of ~9. The thin Al_2O_3 gate dielectric allows the channel potential to be modulated at a relatively low gate voltage without significant gate leakage, resulting in a steep S and a high I_{on}/I_{off}. Figure 2b shows linear-scale and log-scale drain current versus gate–source voltage (I_{ds}–V_{gs}) characteristics for the same In_2O_3 NWT at $V_d = 0.5$ V before 2 min of ozone treatment (black squares) and after 2 min of ozone treatment (red solid line). Ozone treatments for 2 min resulted in significant device performance enhancement in terms of S, V_T and I_{on}. Compared with as-fabricated devices, S was reduced from 600 mV dec^{-1} to 160 mV dec^{-1}, along with improvement in I_{on}/I_{off} (~1×10^6), and a shift in V_T from −1.16 V to −0.27 V. The improvement in S is due to change in terms of a reduction in the interfacial trap states and in fixed surface charge states[25]. Ozone treatment not only removes defects and contamination from the nanowire surface, but also changes the work function[29,30]. Ozone is also expected to increase the density of oxygen vacancies near the nanowire surface. Because oxygen vacancies act as donor states[31,32], this should increase nanowire conductivity. Although the ITO and IZO microstructures and chemical bonding states

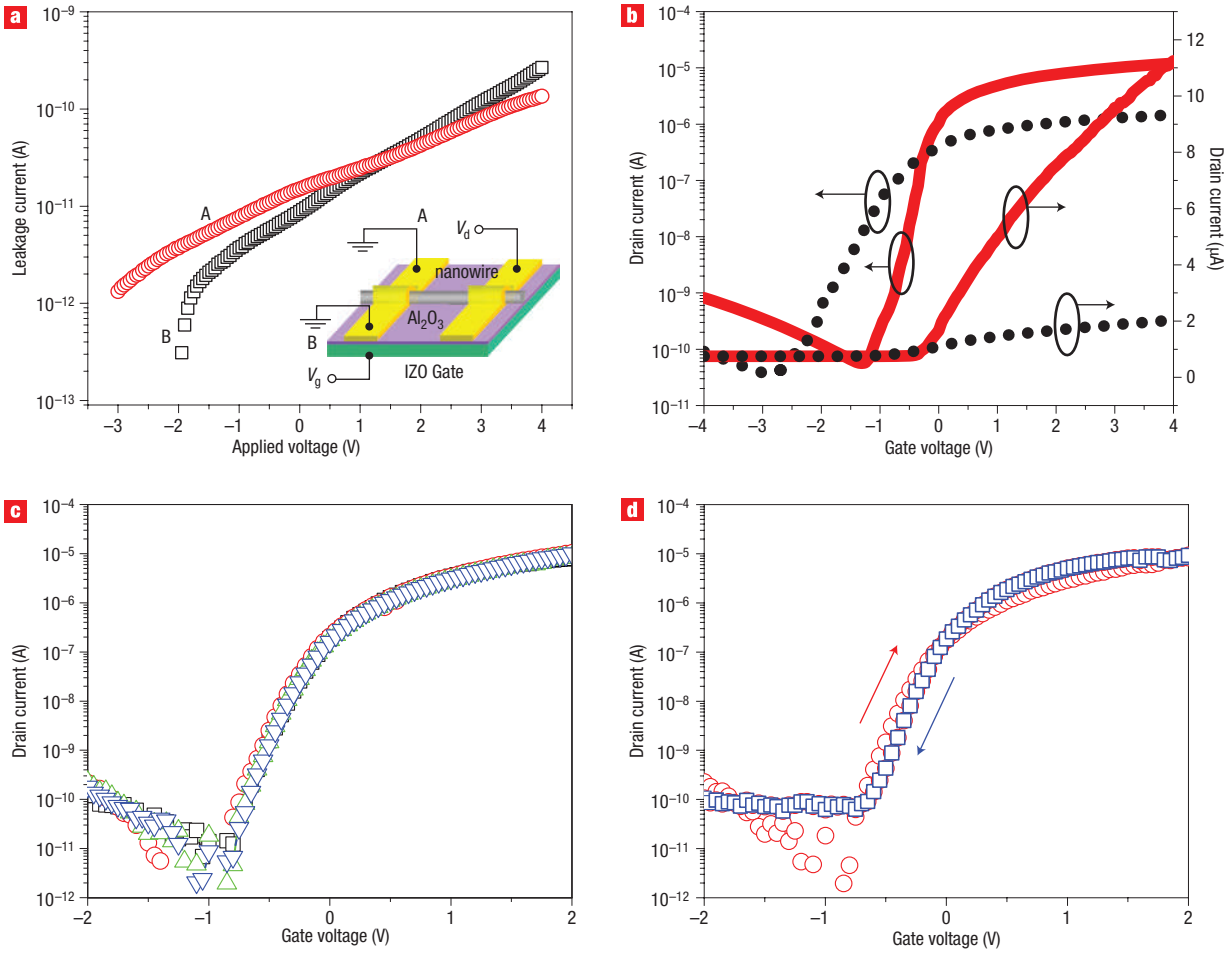

Figure 2 Characteristics of fully transparent In_2O_3 NWTs. a, Gate leakage (B, black open squares) and drain leakage (A, red open circles) of the device (shown in inset). **b**, The linear-scale and log-scale $I_{ds}-V_{gs}$ characteristics of an In_2O_3 NWT at $V_d = 0.5$ V. Arrows indicate appropriate axis. Data points are shown for the device before (black squares) and after (red solid line) 2-min ozone treatment. **c**, The log-scale $I_{ds}-V_{gs}$ characteristics during ten successive sweeps from -4 V to $+4$ V ($V_d = 0.5$ V). Black, red, green and blue data points correspond to first, second, third and fourth sweeps, respectively. The time between sweeps is ~1 s. **d**, Measured $I_{ds}-V_{gs}$ characteristics showing sweeps from -2 V_g to $+2$ V_g (red circles) and from $+2$ V_g to -2 V_g (blue squares), as indicated by arrows ($V_d = 0.5$ V). The bias sweep rate (dV_g/dt) is 2 V s^{-1}.

are more complex, the basic crystal structures are sufficiently similar to those of In_2O_3 and ZnO to reasonably expect that the In_2O_3 and ZnO nanowire work functions will increase similarly upon ozone treatment[30,33]. Thus, the source/drain–nanowire contact should not significantly change with ozone treatment. However, because the ozone treatment plausibly reduces nanowire surface dangling bonds and carbon contamination, and forms an oxygen vacancy-rich surface, the transistor characteristics including I_{on}/I_{off}, S and V_T should be enhanced[34]. Figure 2c shows $I_{ds}-V_{gs}$ curves for another device during four successive sweeps from -2 V to $+2$ V, illustrating the excellent stability of the In_2O_3 NWT. The $I_{ds}-V_{gs}$ curves are comparable following bias sweeps, with consistent I_{on}/I_{off}, S and V_T values. Furthermore, for the same device, $I_{ds}-V_{gs}$ curves were swept from negative gate voltage ($V_g(-)$) to positive gate voltage ($V_g(+)$) and back to $V_g(-)$ as shown in Fig. 2d. Over this bias range, the hysteresis is modest, which illustrates the excellent quality of the Al_2O_3 gate insulator and indicates negligible charge trapping and detrapping in the gate insulator. Note that the nanowire channel active regions are not passivated in these devices.

Figure 3a,c shows the $I_{ds}-V_{gs}$ characteristics for representative single In_2O_3 and ZnO NWTs. The In_2O_3 device (the same device as in Fig. 2a,b) exhibits $S = 160$ mV dec^{-1}, $I_{on}/I_{off} = 1 \times 10^6$ and $V_T = -0.27$ V. The μ_{eff} of the representative In_2O_3 NWT, deduced from transconductance ($g_m = dI_d/dV_g$), varies from ~514 to 300 cm^2 V^{-1} s^{-1} as the gate bias is increased from 0 V to 2 V, following a trend that is observed in NWTs, TFTs and MOSFETs. The ZnO NWT device exhibits $S = 0.3$ V dec^{-1}, $I_{on}/I_{off} \approx 1 \times 10^6$ and $V_T = -0.07$ V, and μ_{eff} varies from ~96 to 70 cm^2 V^{-1} s^{-1} over the gate bias range of 0 V to 3 V. One important device performance metric for high-speed and low-power operation is the $S = dV_{gs}/d\log I_{ds}$ (mV dec^{-1}). A small S value is required for switching transistors, ideally approaching the theoretical limit of ~60 mV dec^{-1}. The present S values were extracted from the linear portion of the $\log I_{ds}$ versus V_{gs} plot (Fig. 3a,c). The very small S values in In_2O_3 and ZnO devices are comparable to other reports[35,36]. The drain current versus drain–source voltage ($I_{ds}-V_{ds}$) characteristics of fully transparent single In_2O_3 and ZnO NWTs are shown in Fig. 3b,d. These devices exhibit typical enhancement mode long-channel FET

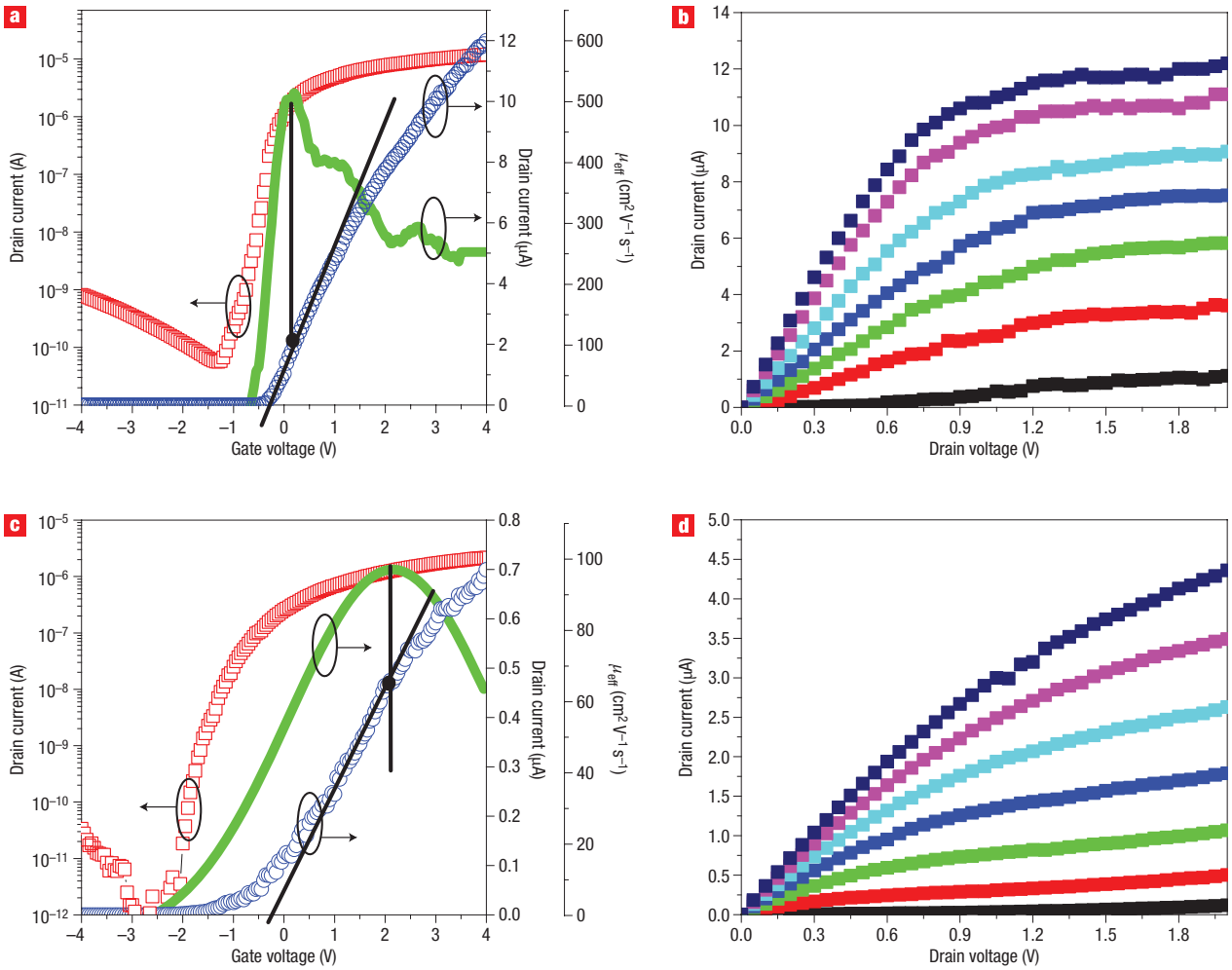

Figure 3 Characteristics of fully transparent In_2O_3 and ZnO NWTs. a, The $I_{ds}-V_{gs}$ characteristic of an In_2O_3 NWT ($D/L \sim 20$ nm/1.80 μm) at $V_d = 0.5$ V. Blue, red and green data points correspond to linear-scale $I_{ds}-V_{gs}$, log-scale $I_{ds}-V_{gs}$ and μ_{eff}, respectively. Arrows indicate appropriate axis. **b**, The $I_{ds}-V_{ds}$ characteristic of fully transparent In_2O_3 NWTs. V_g ranges from -0.5 V to 2.5 V in 0.5 V steps, with the maximum current observed at $V_g = 2.5$ V. **c**, The $I_{ds}-V_{gs}$ characteristic of ZnO NWTs ($D/L \sim 120$ nm/1.66 μm) at $V_d = 0.5$ V. Blue, red and green data points correspond to linear-scale $I_{ds}-V_{gs}$, log-scale $I_{ds}-V_{gs}$ and μ_{eff}, respectively. Arrows indicate appropriate axis. **d**, The $I_{ds}-V_{ds}$ characteristic of fully transparent ZnO NWTs. V_g ranges from 0.0 V to 3.0 V in 0.5 V steps, with the maximum current observed at $V_g = 3.0$ V.

behaviour. For the fully transparent In_2O_3 single NWT device, I_{on} is $\sim 1 \times 10^{-5}$ μA at $V_{ds} = 1.0$ V and $V_{gs} = 2.0$ V. The I_{on} of a ZnO single NWT device is ~2 μA at $V_{ds} = 1.0$ V and $V_{gs} = 2.0$ V. The performance of In_2O_3 and ZnO NWT devices is comparable to that of previously reported non-transparent In_2O_3 and ZnO NWT devices[35–40]. Because the extraction procedure for μ_{eff} involves uncertainties due to the required capacitance estimation (see Methods), NWTs can be compared with planar transistors by comparing the I_{on} and g_m per unit width (g_m/W), using the nanowire diameter as the device width. The In_2O_3 nanowire on glass exhibits an I_{on} density of ~600 mA mm^{-1} and a g_m/W of ~212 mS mm^{-1}. Both values are more than five times higher than those obtained in previous studies on transparent transistors using In_2O_3 thin films, even after adjusting for the differences in gate lengths and gate capacitance. The single-crystal nature of the nanowires and the formation of relatively high-quality interfaces are believed to play key roles in achieving this performance.

The optical transmission spectra through the In_2O_3 and ZnO NWT structures, with the substrate absorption removed, are shown in Fig. 4, showing the optical transmissions to be about 90% for both transistor types. With the substrate included, the optical transmissions are ~82% (In_2O_3 NWT + glass substrate) and ~83% (ZnO NWT + glass substrate) in the 350–1,350 nm wavelength range. The NWT array regions are 1.0 × 0.5 inch (the glass substrate is 1.5 × 1.0 inch), contain 23,000 NWT device patterns, and the substrates are entirely covered by the SiO_2 buffer layer and the Al_2O_3 gate insulator. The source/drain regions and the gate regions cover ~45% and ~25% of the total NWT array region, respectively. The optical absorption of the In_2O_3 and ZnO nanowires should thus be negligible because the diameter of the nanowires is small and the area covered by the nanowires is relatively small compared with the entire NWT array. The observation of >90% optical transmission indicates that the transmission losses due to the various layers, including the nanowires, are negligible, and that visible light can readily penetrate the dense NWTs. The image in the inset of Fig. 4 shows a transparent In_2O_3 NWT device structure, with text on an underlying opaque layer clearly visible.

Fully transparent and flexible In_2O_3 NWT devices using a polyethylene terephthalate (PET) plastic substrate (Melinex,

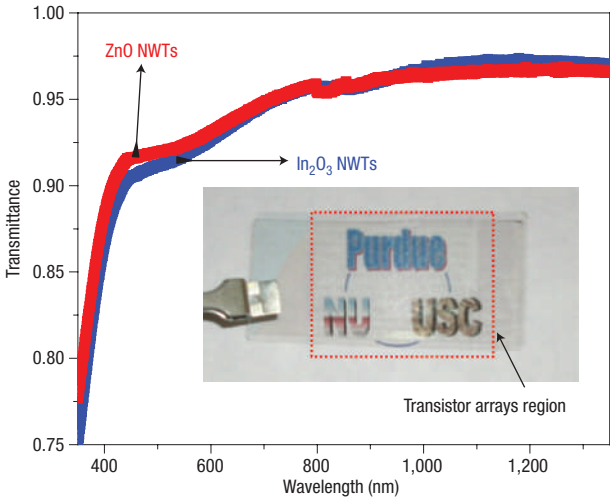

Figure 4 Optical transmission spectra through entire NWT structures. Blue and red lines correspond to In_2O_3 and ZnO NWTs, respectively. The inset shows the image of a transparent In_2O_3 NWT substrate having 23,000 devices, showing that text on the layer behind the substrate is clearly visible.

DuPont) were also fabricated. A cross-sectional view of the present fully transparent and flexible In_2O_3 NWT device structure with an individually addressed bottom gate is shown in Fig. 5a. D and L for the single In_2O_3 nanowires addressed between source and drain on the plastic substrate are 20 nm and 1.79 μm, respectively. In order to suppress the leakage current due to tensile/compressive stress of the plastic substrate during photolithographic processing (up to 130 °C) and gate insulator deposition (up to 200°C), a relatively thick Al_2O_3 gate insulator (50 nm) is used. A fully transparent and flexible In_2O_3 NWT using In_2O_3 nanowires as the active material, ITO as the bottom gate electrodes and ITO as source/drain electrodes is shown in Fig. 5b. The optical transmission through the NWT structure and substrate, with spectra shown in Fig. 5c, is ~81% in the 350–1,350 nm wavelength range. Figure 5d shows the I_{ds}–V_{gs} characteristic of a representative single In_2O_3 NWT on the plastic substrate. Here $S = 0.9$ V dec^{-1}, $I_{on}/I_{off} \approx 1 \times 10^5$, $V_T = -0.6$ V, and μ_{eff} varies from ~167 to 120 cm^2 V^{-1} s^{-1} over the gate bias range of 1–3.5 V. The lower but respectable response characteristics on the plastic substrate may reflect the effects of high-temperature deposition (300 °C) and post rapid thermal annealing (500 °C for 30 s in N_2). Further optimization efforts are presently in progress.

Possible applications of the present transparent NWTs include pixel drivers for AMOLED displays. For AMOLEDs, increasing the

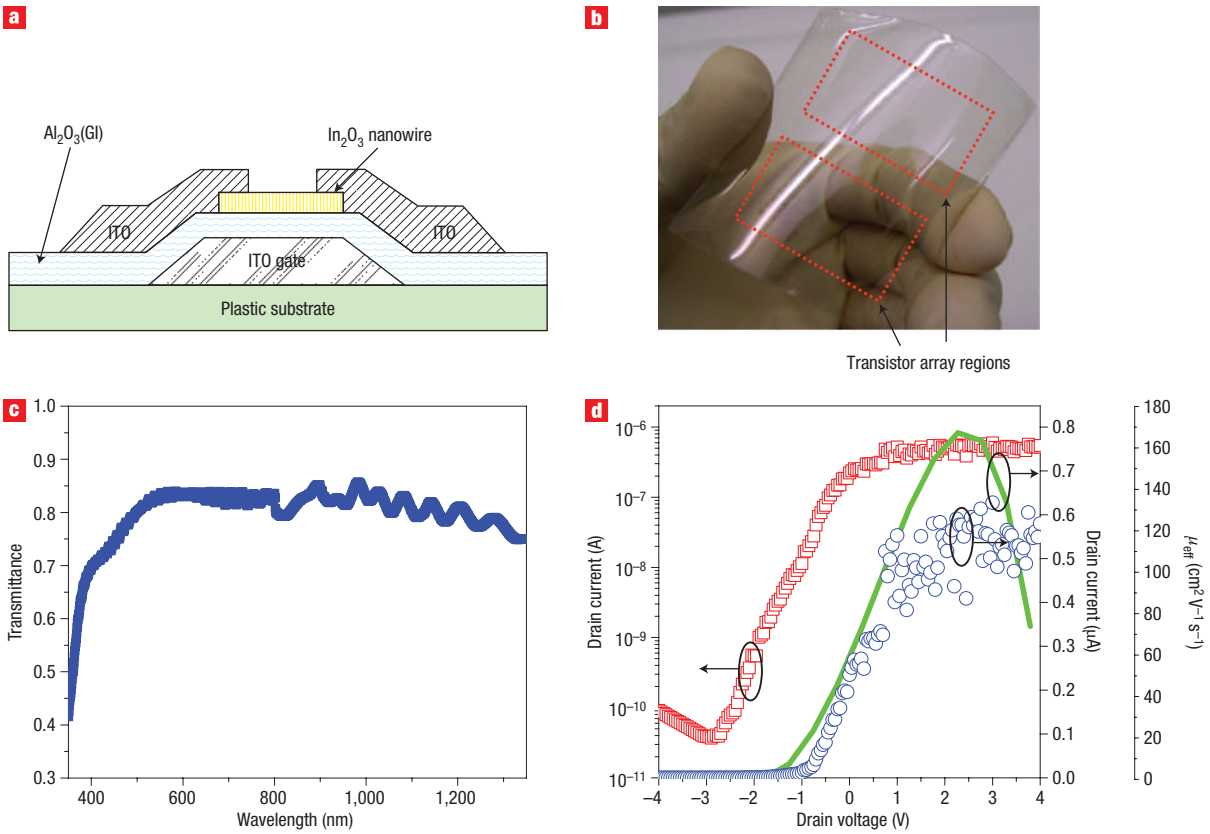

Figure 5 Fully transparent and flexible In_2O_3 NWTs. a, Cross-sectional view of fully transparent and flexible NWT device structure consisting of a plastic substrate, patterned ITO gate electrode (120 nm), ALD-deposited Al_2O_3 gate insulator (50 nm), a single In_2O_3 nanowire ($D/L \sim 20$ nm/1.79 μm) for the active channel, and ITO for the source/drain electrodes (120 nm). **b**, Image of In_2O_3 NWTs on the plastic substrate, showing the optical clarity and mechanical flexibility. **c**, Optical transmission spectrum of region containing In_2O_3 NWTs on the plastic substrate (ITO(S/D)/In_2O_3 nanowires/Al_2O_3 /ITO(G)/plastic substrates). **d**, The I_{ds}–V_{gs} characteristic of In_2O_3 NWTs at $V_d = 0.5$ V. Blue, red and green data points correspond to linear-scale I_{ds}–V_{gs}, log-scale I_{ds}–V_{gs} and μ_{eff}, respectively. Arrows indicate appropriate axis.

aperture ratio is necessary to increase efficiency and reduce power consumption. For non-transparent transistors, maximizing the aperture ratio corresponds to minimizing the transistor and capacitor physical sizes. Transparent transistors would allow stacking of the drive transistors with the OLEDs, which would allow a larger transistor size (width/length) and capacitor size (single or dual capacitors). Device geometries could then be optimized to improve metrics such as peak luminescence, Commission Internationale de L'Éclairage (CIE) coordinates and power consumption. Importantly, the present NWTs exhibit relatively high performance in comparison with typical TFTs for display applications, which should allow higher operating speeds and/or smaller device areas. For instance, in order to produce white peak luminance of $\sim$ 300 cd m^{-2} (71 $\times$ 213 μm pixel size, 40% aperture ratio, 40% polarizer transmission, 5.1 cd A^{-1} of red, 13 cd A^{-1} of green, 5.7 cd A^{-1} of blue, and (0.31, 0.32) of white CIE coordinates) using phosphorescent materials, driving transistors on RGB pixels must provide $\sim$2.44 μA (red), $\sim$1.01 μA (green), $\sim$1.46 μA (blue) and $\sim$3.9 μA (white), respectively[41]. Therefore, the present transparent NWTs would be suitable for switching and driving transistors on such pixels. It is also expected that the required current for AMOLED operation will decrease with increasing aperture ratio provided by all-transparent components. The realization of flexible and transparent NWTs could also enable high-resolution and low-power consumption products such as head-up displays. Although challenges remain in the precise control of nanowire positions and orientations on large-scale substrates for NWT integration, promising advances have recently been reported[42–45]. For example, one report has demonstrated greater than 90% yield for the assembly of single-walled carbon nanotubes in desired positions[42]. Moreover, nanowire/nanotube networks (nanomat/nanobundles) are also possible solutions[46–48]. We recently reported transistors consisting of up to 22 ZnO nanowires assembled in parallel and have shown that on-current levels scale with the number of nanowires and with negligible degradation in the subthreshold slope[49].

CONCLUSIONS

In summary, fully transparent NWTs are fabricated using In_2O_3 and ZnO nanowires as active channels, Al_2O_3 as the gate insulator, ITO as the source/drain electrodes and IZO as the gate electrodes. The optical transmission of these devices is $\sim$82%, and they exhibit transfer and current versus voltage (I–V) characteristics comparable to those observed in non-transparent devices using the same types of nanowires. Fully transparent and mechanically flexible NWTs are fabricated on plastic substrates and have an optical transmission of $\sim$81%. The combination of excellent optical transparency and mechanical flexibility of In_2O_3 and ZnO nanowires, as well as excellent device performance metrics, make these NWTs an attractive technology for realizing transparent and flexible circuits. Fully transparent NWTs will not only increase aperture ratio efficiency in active matrix arrays, but will also enable low-power consumption as well as transparency for future display technologies.

METHODS

FABRICATION OF In_2O_3 AND ZNO NWT DEVICES

The 500-nm-thick SiO_2 was deposited by plasma-enhanced chemical vapour deposition on Corning 1737 glass substrates and served as a buffer and planarization layer. Individual gate electrodes were formed by sputtering IZO (R_{sheet} = 40 ohms per square) and by ion-assisted deposition (IAD) at room temperature (R_{sheet} = 60 ohms per square) and subsequent patterning by photolithography and etching. An 18-nm-thick layer of Al_2O_3 was then deposited using atomic layer deposition at 300 °C in an ASM Microchemistry F-120 ALCVD system using trimethyl aluminium ($Al(CH_3)_3$) (TMA) and water as precursors. Following Al_2O_3 deposition, the substrates were annealed at 500 °C for 30 s under N_2 to improve the film quality. Next, a suspension of In_2O_3 or ZnO nanowires in VLSI-grade 2-propanol solution was disbursed on the gate patterned substrates. Single-crystal semiconducting In_2O_3 nanowires were synthesized by a pulsed laser ablation process[26], with average diameter and length of 20 nm and 5 μm, respectively. Powdered ZnO nanowires synthesized by thermal evaporation and condensation were purchased from Nanolab. The average diameter and length were 120 nm and 5 μm, respectively, and microstructural characterization indicated that they were highly crystalline[27]. Finally, ITO source/drain electrodes were deposited by IAD at room temperature and patterned by photolithography. Following source/drain electrode patterning, the NWTs were subjected to an ozone treatment (UV-Ozone cleaner, UVO 42-220, Jelight) for 2 min to achieve optimum transistor performance in terms of I_{on}, I_{on}:I_{off} ratio, S and μ_{eff}. The ozone environment was obtained by setting the oxygen content to 50 p.p.m., the ultraviolet (UV) wavelength to 184.9 nm and UV lamp power to 28 mW cm^{-2} at 254 nm. Note that the devices were shielded from UV light. Fully transparent and flexible In_2O_3 NWT devices using PET (Melinex, DuPont) were also fabricated with a PET/ITO(G)/Al_2O_3/In_2O_3 nanowire/ITO(S/D) structure (Fig. 5a). The 50-nm-thick Al_2O_3 layer was deposited at 200 °C. The ITO for the gate and source/drain electrodes was deposited using IAD. The nanowire lengths of given transistors between source and drain were obtained from the FE-SEM image, and account for the angle between the nanowire and the electrode edges.

CHARACTERIZATION METHODOLOGY

The work function of an as-grown ITO thin film was measured using an AC-2, RKI Instruments photoelectron spectrometer. The UV-Vis spectra were recorded with a Varian Cary 1E spectrophotometer. Electrical I–V measurements were performed using a Keithley 4200 semiconductor characterization system. The nanowires within a device were imaged with a Hitachi S-4800 FE-SEM following electrical characterization.

CALCULATION OF MOBILITY AND THRESHOLD VOLTAGE

In contrast with planar transistors in which carrier concentration and mobility can be determined independently, for example, through Hall effect and conductivity measurements, the lack of extended lateral geometries in NWTs dictates an alternative approach for determining mobility. Following the typical approach used in earlier NWT studies, we calculated a field-effect mobility (μ_{eff}) using a combination of the cylinder-on-plate (COP) capacitance model $C_i = 2\pi\varepsilon_0 k_{eff} L/\cosh^{-1}(1 + t_{ox}/r)$ and the relationship $\mu = dI_{ds}/dV_{gs} \times L^2/C_i \times 1/V_{ds}$ obtained from the MOSFET linear region model[50], where a k_{eff} value of $\sim$9.0 is the effective dielectric constant of Al_2O_3, L is the channel length of the NWTs ($\sim$1.80 μm for an In_2O_3 nanowire, $\sim$1.66 μm for a ZnO nanowire), r is the radius of the NWTs (10 nm for the In_2O_3 nanowire, 60 nm for the ZnO nanowire), $t_{ox} \sim$ 18 nm is the thickness of the gate insulator, dI_{ds}/dV_{gs} is the transconductance and V_{ds} is drain voltage. In the case of flexible and transparent In_2O_3 NWTs, $L \sim$ 1.79 μm and $r \sim$ 10 nm are used. Our device geometry consists of the gate dielectric ($k_{eff} \sim$ 9) below and air ($k_{eff} \sim$ 1) above the nanowire. A previous comparision[51] between electrostatic simulations and an analytic formula for capacitance (a form of the COP equation valid for $t_{ox} \gg r$) for a comparable geometry to SiO_2/air showed good agreement between the two capacitances over a range of t_{ox}/r from 8 to 40, provided that a value of $k_{eff} = 0.5\varepsilon_{R1SiO2}$ was used. As our geometry uses a higher k dielectric constant and smaller t_{ox}/r ($\sim$1.8), the fringing fields are more tightly confined to the gate dielectric layer. We have therefore chosen to use $k_{eff} \sim \varepsilon_{R1Al2O3}$, which would tend to overestimate the capacitance (because the appropriate correction factor is greater than 0.5 but less than 1.0), and therefore underestimate the mobility. The transconductances shown in Fig. 3a,b and Fig. 4d have been smoothed by polynomial fit to three orders with 20 points fit to the curve. In order to extract V_T, here we used the extrapolated V_T ($V_T = V_G(g_{m\_max}) - (I_D(g_{m\_max})/g_{m\_max})$ where $g_m = \partial I_D/\partial V_G$ (at V_d = 0.5 V)), because it gives an accurate V_T. The gate voltage at the maximum g_m ($V_g(g_{m\_max})$), the drain current at the maximum g_m, $I_d(g_{m\_max})$, and the maximum $g_m(g_{m\_max})$ are obtained from Fig. 3a,c and Fig. 5d. These values are confirmed with V_T values obtained from the I_{ds}–V_{ds} curve at V_d = 0.1 V.

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Author contributions

All authors contributed equally to this work and all discussed the results and commented on the manuscript.

Competing financial interests

The authors declare no competing financial interests.