Device study, chemical doping, and logic circuits based on transferred aligned single-walled carbon nanotubes

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In this paper, high-performance back-gated carbon nanotube field-effect transistors based on transferred aligned carbon nanotubes were fabricated and studies found that the on/off ratio can reach 10^7 and the current density can reach 1.6 μA/μm after electrical breakdown. In addition, chemical doping with hydrazine was used to convert the *p*-type aligned nanotube devices into *n*-type. These devices were further utilized to demonstrate various logic circuits, including *p*-type metal-oxide-semiconductor inverters, diode-loaded inverters, complementary metal-oxide-semiconductor inverters, NAND, and NOR gates. This approach could work as the platform for future nanotube-based nanoelectronics. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2956677]

Since the discovery of carbon nanotubes (CNTs) by Iijima in 1991,[1] significant effort has been devoted to understanding their electronic properties.[2–6] Various logic circuits including inverters, NAND, NOR, and ring oscillators have been demonstrated with devices based on individual or a few single-walled CNT.[7–11] Recently, the growth of massively aligned nanotubes on sapphire or quartz substrates was also reported by several groups including our own.[12–16] Based on the aligned nanotube synthesis, a nanotube-on-insulator technology was proposed.[17] The advantages of devices based on massively aligned nanotubes include registration-free fabrication, high device yield, and high on-state current. Inspired by these advantages, we fabricated high-performance back-gated nanotube transistors using the transferred aligned nanotubes and systematically studied the device performance. In addition, hydrazine doping was utilized to convert the *p*-type devices into *n*-type. Furthermore, many kinds of logic circuits based on the aligned nanotube devices were also demonstrated, including *p*-type metal-oxide-semiconductor (PMOS) inverters, diode-loaded PMOS inverters, complementary metal-oxide-semiconductor (CMOS) inverters, NAND, and NOR gates.

Figures 1(a) and 1(b) are the schematic, optical micrograph, and scanning electron microscope (SEM) image of the back-gated CNT field-effect transistors (CNTFETs). The devices were fabricated by transferring aligned CNT from quartz substrates to Si/SiO_2 substrates followed by electrode patterning using a method adapted from our previous work.[17] Briefly, ferritin catalysts were defined by photolithography on the quartz substrates followed by calcination in air at 900 °C for 10 min. Then, conventional chemical vapor deposition approach was employed to grow perfectly aligned CNT between the catalyst islands with CH_4, C_2H_4, and H_2 as the feeding gases.[15] Typically, our nanotubes have a density of 3–10 nanotubes/μm as shown in Fig. 1(b), inset. After growth, 100 nm gold film was deposited onto the quartz substrate containing nanotubes, and the Revalpha tape (No. 3198M from Nitto Denko), the so-called thermal releasing tape, was used to peel off the gold film together with the grown nanotubes, which was then pressed with polydimethylsiloxane (PDMS) stamp against the targeting substrate (Si/SiO_2 as in our experiment) preheated on a hotplate at 140 °C for 20–30 s. After this process, the thermal tape was peeled off with the PDMS stamp. Finally, gold etchant

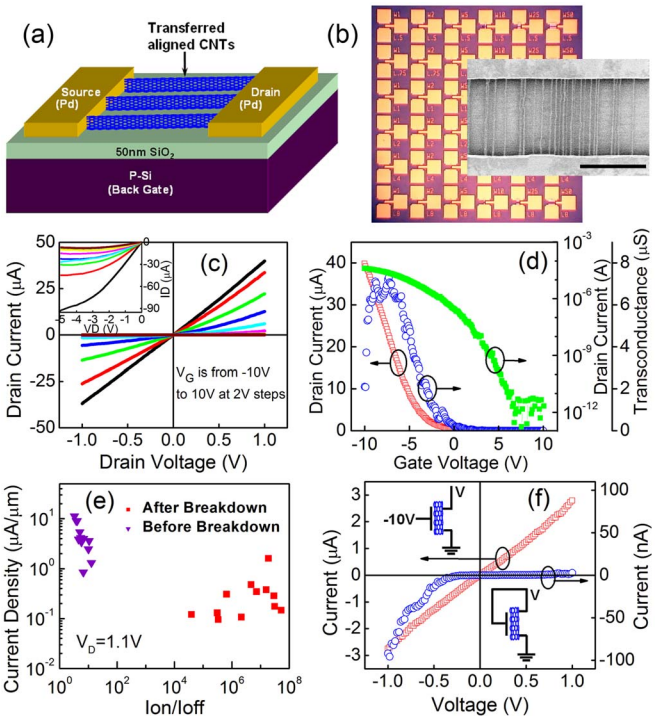

FIG. 1. (Color online) (a) Schematic of the device. (b) Optical micrograph of the back-gated transistors used in this study. Inset: SEM image of a typical device. The scale bar is 3 μm. (c) I_D-V_D curves of the device with inset showing the saturation behavior. (d) I_D-V_G curves (red: linear scale, green: log scale) and g_m-V_G curve (blue) of the device. (e) Statistics of devices before and after electrical breakdown. (f) Two-terminal behavior of the CNTFET showing Ohmic behavior with V_G=−10 V, and diode behavior with the gate and drain tied together.

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(KI/I_2) was used to remove the gold film, leaving only aligned nanotubes on the target substrate. SEM inspection revealed that our nanotube transfer technique can transfer almost all the as-grown nanotubes to the Si/SiO_2 substrate. Finally, the electrodes were patterned by photolithography, and 10 nm Ti and 100 nm Pd were deposited followed by the lift-off process. Such devices were made with channel widths (W) of 1, 2, 5, 10, 25, and 50 μm, and channel lengths (L) of 0.5, 0.75, 1, 2, 4, and 8 μm.

We carried out systematic study of the electrical performance of the devices. Figures 1(c) and 1(d) are the typical output characteristics (I_D-V_D curves) and transfer characteristics (I_D-V_G curves) for a transistor with $W=25$ μm and $L=0.75$ μm after proper electrical breakdown to remove metallic nanotubes. This device has around 75 CNT bridging the source and drain electrodes. The I_D-V_D curves appear to be very linear for V_D between −1 and 1 V, indicating that Ohmic contacts are formed between the electrodes and the nanotubes. These devices typically exhibit saturation behavior under higher negative V_D, as shown in Fig. 1(c), inset. The representative on current at $V_D=1$ V is measured to be around 40 μA, corresponding to a current density of 1.6 $\mu A/\mu m$, the on/off ratio exceeds 10^7 and the transconductance (g_m) is 7 μS, indicating the high performance of our devices.

Figure 1(e) is a statistical study of devices with various channel width and $L=0.75$ μm before and after electrical breakdown, where the on-state current density (on current I_{on} divided by the channel width) is plotted versus the on/off ratio. I_{on} is measured at $V_D=1.1$ V and $V_G=-10$ V, and I_{off} is measured at $V_D=1.1$ V and $V_G=10$ V. One can clearly see that the tuning of the device on/off ratios can be achieved with electrical breakdown. Before breakdown, the devices exhibit on/off ratios in the range of 1–10, due to the presence of metallic nanotubes. In contrast, after electrical breakdown, the on/off ratios undergo significant improvement to the range of 4×10^4–5×10^7, accompanied by a moderate degradation of the on current. The resulting devices exhibit rather narrow on-state current distribution and can be used as the platform for nanotube circuits. We nevertheless note that the electrical breakdown is time consuming, and thus one still needs to develop better ways to remove metallic nanotubes in a more scalable fashion.

Figure 1(f) shows that by tying the gate and drain together, the device that exhibits Ohmic behavior (red curve) can be easily converted into a diode (blue curve). When the applied voltage is negative, the upper terminal serves as drain, so that the gate and drain are tied together and the device will act as a diode. This kind of circuit configuration is similar to the concept of diode-connected transistor in silicon devices. The above-mentioned devices can be utilized to realize diode-loaded inverters as discussed below.

In order to convert devices in to n-type, many approaches have been reported in literature.[7,18–20] However, many of the doping methods have their relative advantages and disadvantages from different view points. For example, potassium doping usually requires high vacuum,[7] while polyethylene imine (PEI) doping normally gives small on-off ratios.[19]

Here we use hydrazine doping[20] to convert p-type devices into n-type while maintaining a reasonable device performance. Schematic of the doping process is shown in Fig. 2(a). The chip with p-type nanotube devices was immersed into hydrazine in isopropanol (volume ratio 1:10) for 1 h. Then the chip was taken out and blown dry without further cleaning with other organic solvents. Electrical measurements show that the p-type devices are indeed converted to n-type, as shown in Figures 2(b) and 2(c). The doping process, somehow, introduces slight degradation to the device performance in both on current, from 1.4 to 0.8 μA, and on/off ratio, from 10^5 to 10^3, respectively. However, the device performance after chemical doping is still better than those devices we get from other doping techniques such as PEI doping. The mechanism of the hydrazine doping process can be understood as the hydrazine molecules adsorb on the surface of CNT and act as dopants. The hydrazine doping method here is believed to be very promising for future complementary integrated circuits based on CNTFETs.

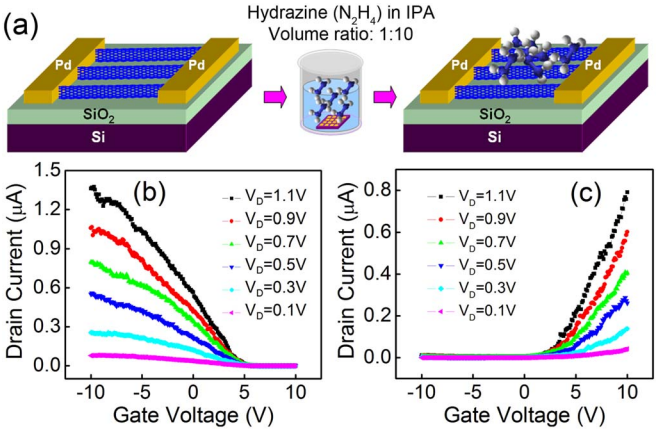

FIG. 2. (Color online) (a) Schematic drawing depicting the hydrazine doping process. (b) I_D-V_G curves of the device before hydrazine doping. (c) I_D-V_G curves of the device after hydrazine doping.

Based on the devices with transferred aligned nanotubes, three kinds of inverters were demonstrated, including PMOS inverters, diode-loaded PMOS inverters, and CMOS Inverters. Figures 3(a)–3(c) display the plots of the output voltage (V_{out}) and the current flow (I_{DD}) versus the input voltage (V_{in}) for the PMOS inverter, the diode-loaded PMOS inverter, and the CMOS inverter, respectively. Measurements

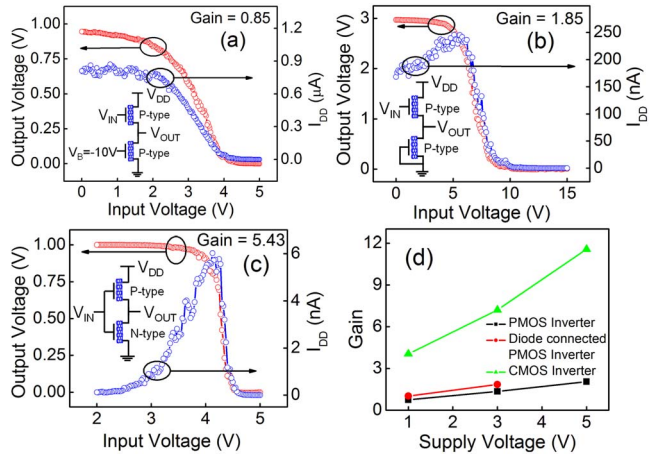

FIG. 3. (Color online) Voltage transfer characteristic (red curve) and power supply current (blue curve) of (a) the PMOS inverter, (b) the diode-loaded inverter, and (c) the CMOS inverter. Inset: schematic of the circuits. The supply voltage is $V_{DD}=1$ V for (a) and (c), and $V_{DD}=3$ V for (b). (d) Curves showing the dependence between the gain and supply voltage of different types of inverters.

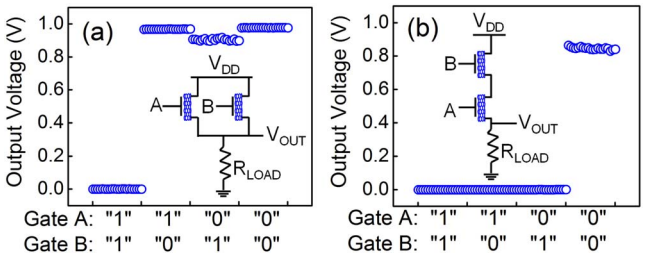

FIG. 4. (Color online) Output characteristics of (a) NAND and (b) NOR, with resistive load. Inset: schematic of the circuits. The supply voltage for both circuits is $V_{DD}=1$ V. Input voltages of 2 and −2 V are treated as logics 1 and 0, respectively.

reveal that our inverters can be operated with a V_{DD} as low as 1 V and an input voltage range of 0–5 V. Comparison between the PMOS inverter and the CMOS inverter reveals that the CMOS inverter has no static power consumption, as current flows only during the transition between different states, while the PMOS inverter has current flowing from V_{DD} to ground all the time. In addition, the CMOS inverter exhibits much smaller current and much higher gain than the PMOS inverter. This is because the *n*-type pull-down device of the CMOS inverter can actually be considered as a resistor with a variable resistance which can help the CMOS inverter to turn off much faster than the PMOS inverter. All those above observations are consistent with the theory of conventional inverters based on silicon devices.

The relationship between the gain of the inverters and the supply voltage was also studied. Figure 3(d) reveals that a larger power supply voltage (V_{DD}) can result in a larger gain. This is true for all three kinds of inverters. The reason is that as the drain voltage increases, the I_D tends to saturate [as shown in Fig. 1(c) inset], thus leading to increases in the output resistance $[r_{out}=1/(dI_D/dV_D)]$, and the voltage gain $(g_m r_{out})$. Figure 3(d) also shows that the CMOS inverter has the highest gain among all three types of inverters. This also agrees well with our expectation based on the theory of inverters made of silicon devices. We note that further improvement is still needed to produce nanotube inverters of even better performance. For instance, there is a mismatch of the V_{in} and V_{out} magnitude for our inverters. This is likely a consequence of the 50 nm SiO_2 used as the gate dielectric. Further reduction of the SiO_2 thickness or replacing SiO_2 with high-*k* materials can be solutions to achieve optimum inverter characteristics.

In addition to inverters, more sophisticated circuits have also been demonstrated. Figures 4(a) and 4(b) show the output characteristics of the NAND and NOR, respectively. Both logic blocks employ a 20 M Ω resistive load in the pull-down network, while two *p*-type aligned nanotube transistors are connected using external wires to serve as the pull-up network. The value of the resistive load is chosen so that it is between the on-state resistance and the off-state resistance of the transistors.

The NAND and NOR circuits are both operated with a V_{DD} of 1 V. 2 and −2 V applying on gates A and B are treated as logics "1" and "0," respectively. For the NAND, the output is 1 when either one of the two inputs is 0, while for the NOR, the output is 0 when either one of the two inputs is 1. These output characteristics confirm that our circuits are realizing the logic function correctly. Based on such aligned nanotube transistors, the construction of truly integrated circuits is currently ongoing and will be published in a separate publication.

As a conclusion, we have fabricated CNTFET devices based on transferred aligned nanotubes and systematically studied their electronic properties. Converting the *p*-type devices to *n*-type was fulfilled by the hydrazine doping technique. Combining the *p*-type, *n*-type, and diode devices we have, we have demonstrated many kinds of logic circuits, including PMOS inverters, diode-loaded PMOS inverters, CMOS inverters, and NAND/NOR gates with resistive load.

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