High-Performance Single-Crystalline Arsenic-Doped Indium Oxide Nanowires for Transparent Thin-Film Transistors and Active Matrix Organic Light-Emitting Diode Displays

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ABSTRACT We report high-performance arsenic (As)-doped indium oxide (In_2O_3) nanowires for transparent electronics, including their implementation in transparent thin-film transistors (TTFTs) and transparent active-matrix organic light-emitting diode (AMOLED) displays. The As-doped In_2O_3 nanowires were synthesized using a laser ablation process and then fabricated into TTFTs with indium−tin oxide (ITO) as the source, drain, and gate electrodes. The nanowire TTFTs on glass substrates exhibit very high device mobilities (~1490 $cm^2 V^{-1} s^{-1}$), current on/off ratios (5.7×10^6), steep subthreshold slopes (88 mV/dec), and a saturation current of 60 μA for a single nanowire. By using a self-assembled nanodielectric (SAND) as the gate dielectric, the device mobilities and saturation current can be further improved up to 2560 $cm^2 V^{-1} s^{-1}$ and 160 μA, respectively. All devices exhibit good optical transparency (~81% on average) in the visible spectral range. In addition, the nanowire TTFTs were utilized to control green OLEDs with varied intensities. Furthermore, a fully integrated seven-segment AMOLED display was fabricated with a good transparency of 40% and with each pixel controlled by two nanowire transistors. This work demonstrates that the performance enhancement possible by combining nanowire doping and self-assembled nanodielectrics enables silicon-free electronic circuitry for low power consumption, optically transparent, high-frequency devices assembled near room temperature.

KEYWORDS: transparent electronics · metal oxide nanowire synthesis · self-assembled gate dielectric (SAND) · AMOLED display

The concept of transparent electronics (also called invisible circuits) was first proposed in 1997[1] and offers the attraction of optical transparency and, in principle, low-temperature processing. There are currently numerous research efforts on transparent electronics, due to its great potential to make significant commercial impact, including in displays,[2−5] solar cells,[6,7] charge-coupled devices (CCDs),[8] and UV detectors.[9,10] The core technology to realize transparent electronics requires the development of high-performance transparent thin-film transistors (TTFTs), with high device mobilities, moderate carrier concentrations, low threshold voltages, and steep subthreshold slopes.[11] Currently, TTFTs fabricated with amorphous or polycrystalline transparent conducting oxide (TCO) thin films have been widely studied, including ZnO, SnO_2, $CuAlO_2$, and many other semiconductor oxides.[1,12−16] However, TTFTs made from these materials usually exhibit rather low mobilities (0.2−120 $cm^2 V^{-1} s^{-1}$) and high threshold voltages (V_{th} = 10−20 V).[14−17] For instance, TTFTs with amorphous indium gallium oxide (*a*-IGO) films display device mobility of 7 $cm^2 V^{-1} s^{-1}$, a current on−off ratio of 10^4, and an inverter gain of 1.5 on glass substrates.[18] These results clearly indicate that the performance of TCO thin-film-based TTFTs may limit their operation in high-frequency applications and has significant room for further improvement.

Recently, one-dimensional (1-D) nanostructured materials, including single-walled carbon nanotubes (SWNTs) and semiconductor metal oxide nanowires, have been considered as another material choice for TTFT fabrications.[19−22] In comparison to conventional TCO-based TTFTs, nanomaterials synthesized through a simple chemical vapor deposition (CVD) method can easily provide high-quality single-crystalline nanostructures, which are highly desirable in most electronic and optoelectronic devices.[23−25] In addition, nanostructured material-based TTFTs have added advantages, such as versatile

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compatibility with a variety of device substrates, which thereby extends their applicability to flexible electronics, due to the compatibility of nanostructured TTFTs with low-temperature processing. Among these nanomaterials, the In_2O_3 nanowire having a wide energy gap (~3.75 eV), a single-crystalline nanostructure, and high device mobility is one of the best candidates for high-performance TTFTs.[20,26] Our research group and Ju *et al.* have also demonstrated In_2O_3 nanowire TTFTs with a device mobility as high as 514 $cm^2 V^{-1} s^{-1}$. However, this performance is still low compared to nontransparent devices,[27] raising the question of whether further improvement might be possible through doping of the nanowires. While doping methods have been employed for controlling carrier concentration and transport properties in nanowires, their effects are not always predictable and remain a challenging issue in nanoelectronics science and technology, which constrains nanowire-based TTFT applications.[21,28]

In considering the enablers of next-generation displays, having good optical transparency and/or mechanical flexibility, high-performance transparent and/or flexible TFTs will be essential. For example, the circuitry of an AMOLED pixel usually contains one driving transistor and one switching transistor. The driving transistors must carry sufficient current to the OLED pixels, and the switching transistors must be able to operate at 60−120 Hz for the human eye to see an integrated image of successively presented patterns in a video display (so-called retinal persistence). Currently, polycrystalline silicon (*poly*-Si) and amorphous silicon (*a*-Si) are widely used as the "back-panel" electronics for AMOLED displays. However, these back-panels are usually optically opaque, not compatible with flexible substrates, and have drawbacks such as low mobilities, high threshold voltages, and, in the case of *a*-Si, poor current-carrying capacity.[11]

In this contribution, we first report the synthesis of arsenic (As)-doped In_2O_3 nanowires on Si/SiO_2 substrates and then fabricate TTFTs by transferring the doped nanowires to glass substrates with prepatterned indium−tin oxide (ITO) gate electrodes and an Al_2O_3 or a self-assembled nanodielectric (SAND) gate insulator, followed by patterning transparent ITO source and drain electrodes. It will be seen that the as-fabricated As-doped In_2O_3 nanowire TTFTs perform as typical n-type FETs with a high device mobility (1490 $cm^2 V^{-1} s^{-1}$) and optical transparency of near 81% in the visible wavelength regime. We further examine the AC gain of these nanowire TTFTs, to the best of our knowledge, the first AC gain study of nanowire TTFTs. The results indicate good frequency response, ~1.5 kHz with a unity-gain frequency of ~18.8 GHz. Moreover, we then show that As-doped In_2O_3 nanowire TTFTs can be used to drive organic light-emitting diodes (OLEDs) with tunable emitting intensities, including a seven-segment AMOLED display enabled by a nanowire TTFT "back-panel".

RESULTS AND DISCUSSION

Characterization of Arsenic-Doped Indium Oxide Nanowires. As-doped In_2O_3 nanowires used in this study were grown on a Si/SiO_2 substrate by a laser ablation process. In contrast to our previous work[29] using argon mixed with oxygen as the carrier gas, we intentionally added hydrogen to the carrying gas to suppress the oxidation processes and incorporate a small amount of As into the In_2O_3 nanowires. The surface morphology and crystal structure of the As-doped In_2O_3 nanowires was further characterized by field-emission scanning electron microscopy (FESEM), high-resolution transmission electron microscopy (HRTEM), selected area electron diffraction pattern (SAED), and energy dispersion X-ray spectrometry (EDS). Figure 1a shows a typical SEM image of as-grown As-doped In_2O_3 nanowires which are ~5−10 μm long with a diameter of 15−30 nm. A Au/In alloy particle, with a diameter of ~16 nm, can be clearly observed at the very tip of the nanowire, supporting growth *via* a so-called vapor−liquid−solid (VLS) growth mechanism (Figure 1a, inset). In addition, the As-doped In_2O_3 nanowires have perfectly smooth surfaces without any amorphous coating and have extremely uniform diameters. To further evaluate the composition of the As-doped In_2O_3 nanowires, EDS was performed during the TEM investigation. Figure 1b shows a typical EDS spectrum of an individual As-doped In_2O_3 nanowire, which indicates the presence of As elements in In_2O_3 nanowires. The atomic ratio of In/As is estimated to be 100:4. The atomic density of indium atoms in In_2O_3 is about 3.12×10^{22} $atom/cm^3$,[30] and the dopant density of 4% As dopants can be estimated to be 1.25×10^{21} $atom/cm^3$. However, the actual amount of As atoms incorporated into the crystal sites of In_2O_3 nanowires is not clear and required more detailed experiments.

The crystallography of these As-doped nanowires was also studied using HRTEM and SAED. HRTEM confirms that each As-doped In_2O_3 nanowire has a perfect single-crystalline structure without any noticeable dislocations or defects, and the corresponding SAED reveals that the phase of As-doped nanowires is body-centered cubic (bcc), as shown in Figure 1c. The interspacing between each plane is 0.506 nm, corresponding to the (200) plane in the bcc As-doped In_2O_3 nanowire crystal structure (shown in Figure 1d), with the lattice constant (*a*) of 1.012 nm slightly expanded *versus* that of undoped In_2O_3 nanowires ($a = 1.01$ nm).[29] The expanded lattice constant can be attributed to the incorporation of As into the In_2O_3 nanowires. Taken together, these results indicate that these nanowires grown using the present laser ablation process exhibit high crystalline quality, with the In_2O_3 nanowire structural integrity preserved after As dopant incorporation.

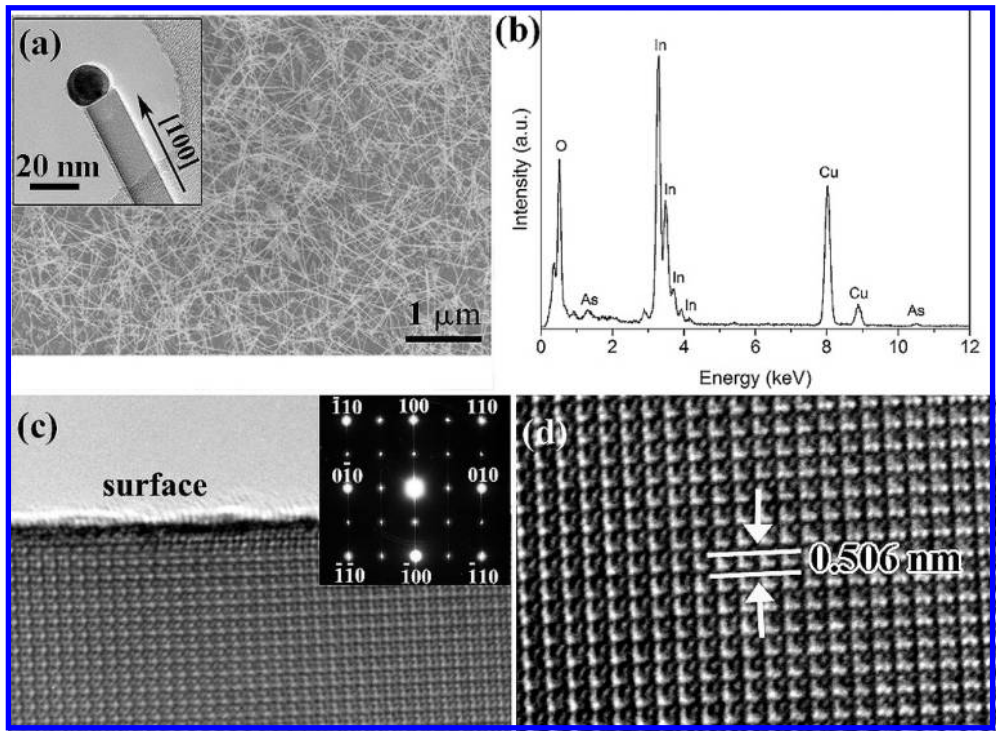

Figure 1. (a) SEM image of As-doped indium oxide nanowires. Inset figure shows an As-doped nanowire with a catalyst particle at the very tip (inset). (b) EDS spectrum showing the chemical composition of the As-doped indium oxide nanowires. (c) Corresponding HRTEM image of a single As-doped In_2O_3 nanowire with a diameter of ~16 nm. The electron diffraction pattern reveals a bcc crystal structure of As-doped In_2O_3 nanowire (inset). (d) In another HRTEM image, the (100) planes are clearly visible and oriented perpendicular to the vertical axis.

Electronic Transport Characteristics of As-Doped In_2O_3 Nanowire TTFTs. It is well-known that doping processes can substantially enhance the electrical properties of nanowire materials in a controlled fashion, and that zinc, antimony, and arsenic are all effective n-type dopants which increase the carrier concentration in In_2O_3 thin films.[31,32] Here we focus on As-doped In_2O_3 nanowires as the semiconductor in TTFT devices. After the nanowire synthesis, the as-grown nanowires were removed from the Si/SiO_2 substrates by ultrasonication to yield a suspension in isopropyl alcohol (IPA) and were then dispersed onto an ITO substrate with 50 nm Al_2O_3 dielectric. The process was performed repeatedly until the desired nanowire density was achieved, and then ITO was deposited as source and drain electrodes. The nanowire orientation is random, but with desired density, we can achieve a yield of 80% for the transistors. Figure 2a shows a schematic of an As-doped In_2O_3 nanowire TTFT on an ITO glass substrate, with an atomic layer deposition (ALD)-derived high-*k* Al_2O_3 (thickness of 50 nm, k_{eff} ~ 9.0) dielectric layer, and ion-assisted deposition-derived (IAD) ITO (thickness of 100 nm, sheet resistance ~60 Ω/□) source and drain electrodes, with the semiconductor-doped metal oxide nanowires as the active channel. Details can be found in the Supporting Information. Figure 2b displays the optical image of an As-doped In_2O_3 nanowire TTFT substrate, with the background photograph visible through the transistor regions. The transmittance spectrum in the Supporting Information (Figure S3) reveals ~81% optical transmission, essentially identical to that of bare glass or glass/ITO substrates.

Detailed electronic transport measurements were carried out to characterize the electronic properties of single As-doped In_2O_3 nanowire TTFTs. The measured drain current (I_{ds}) *versus* source−drain voltage (V_{DS}) characteristics of a representative single nanowire TTFT is shown in Figure 2c. The channel length of the as-fabricated TTFTs is ~1.8 μm, shown in the inset SEM image of Figure 2d (scale bar = 1 μm). The device exhibits typical enhancement-mode n-type semiconductor transistor behavior with an on-current (I_{on}) of ~60 μA, while V_g = 4.5 V and V_{DS} = 3 V. Note that doping helps to reduce the contact resistance in In_2O_3 nanowire FETs, shown by the absence of a Schottky barrier in Figure 2c.

Figure 2d shows the drain current (I_{ds}) *versus* gate voltage (V_g) characteristics for a single transparent As-doped In_2O_3 nanowire transistor. The doped In_2O_3 nanowire devices display $I_{on}/I_{off} = 5.7 \times 10^6$, a peak subthreshold slope (S) = 88 mV/dec, and threshold voltage (V_T) = 0.5 V, while V_{DS} = 200 mV. The mobility (μ) was calculated from the maximum transconductance by applying the eqs 1 and 2.[20]

$$\text{device mobility } (\mu) = \frac{L^2}{V_{DS}C_i} \times \frac{dI_{DS}}{dV_g} \qquad (1)$$

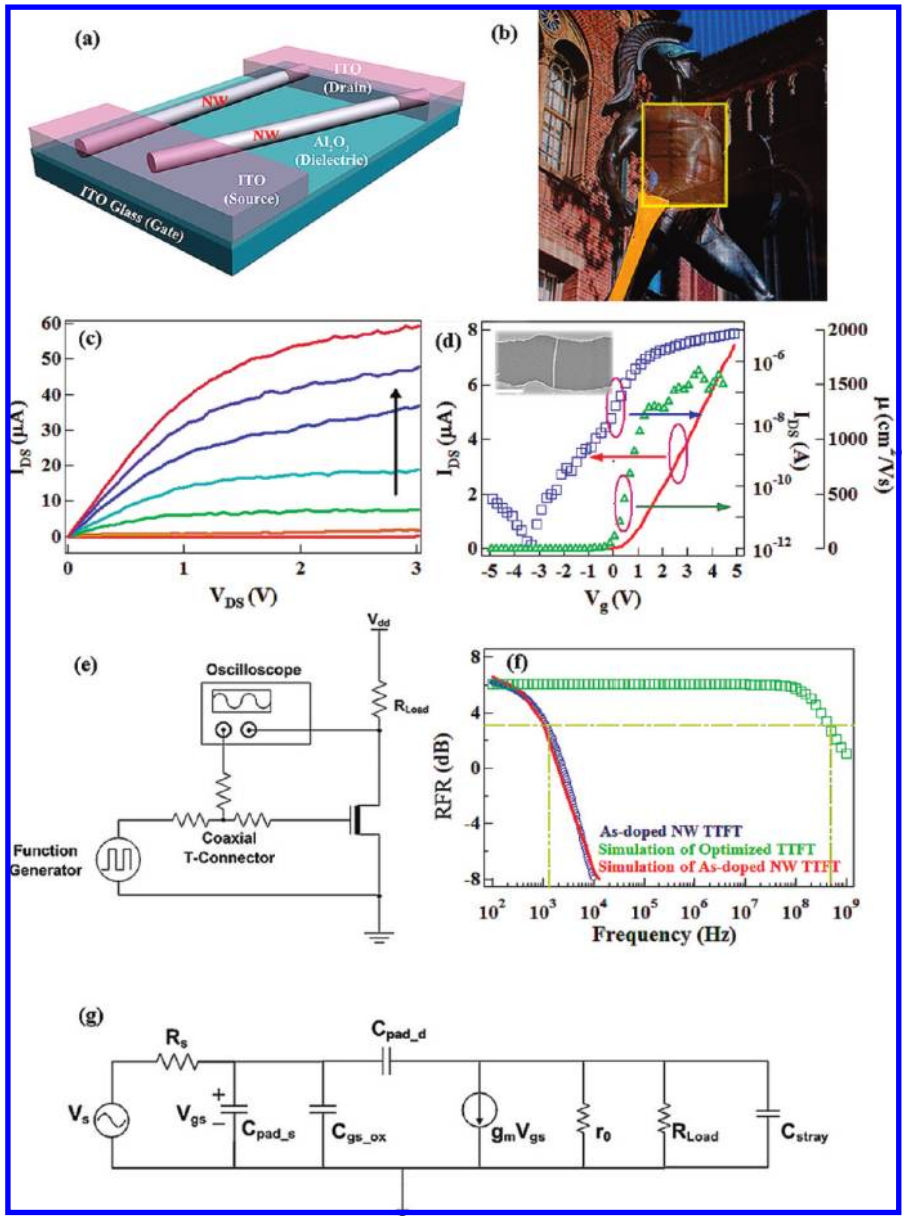

Figure 2. Fabrication of fully transparent As-doped In_2O_3 nanowire transistors. (a) Schematic diagram of As-doped In_2O_3 nanowire TTFT fabricated on an ITO glass substrate, with ALD-deposited Al_2O_3 or SAND as the dielectric layer and IAD-deposited ITO as source and drain electrodes. (b) Optical photograph of fully transparent As-doped In_2O_3 nanowire transistors. The substrate area is marked with a yellow frame for clarity. (c) Family of $I_{ds}-V_{DS}$ curves of a single As-doped In_2O_3 nanowire TTFT with the channel length of 1.8 μm. The gate voltage varied from −4.5 to 4.5 V in a step of 1.5 V from bottom to top. Inset: SEM image of an As-doped In_2O_3 nanowire bridging ITO electrodes. (d) Current *versus* gate voltage ($I_{ds}-V_g$) plot in the linear regime (V_{DS} = 200 mV). Red, green, and blue curve correspond to linear-scale $I_{ds}-V_g$, log scale $I_{ds}-V_g$, and μ, respectively. Inset shows an SEM image of the nanowire transistor. (e) Measurement setup showing As-doped In_2O_3 nanowire transistor configured as a common-source amplifier. (f) Frequency response of AC gain of As-doped In_2O_3 nanowire TTFT. Solid blue line shows the measured frequency response of As-doped In_2O_3 nanowire TTFT; dashed red line represents the simulated data of As-doped In_2O_3 nanowire TTFT. The green solid line shows simulation data for an optimized As-doped In_2O_3 nanowire TTFT. (g) Bilateral small-signal model used in this study.

where L is the channel length and C_i is the specific capacitance of single doped nanowire calculated as follows[26]

$$C_i = 2\pi\varepsilon_0\varepsilon_s L/\ln(2h/r) \quad (2)$$

where, r is the radius of doped In_2O_3 nanowires, h is the thickness of the dielectric layer, and ε_s is the dielectric constant of ALD-deposited Al_2O_3. It is found that the device mobility varies from ~1080 to 1490 $cm^2 V^{-1} s^{-1}$ as the gate bias is increased from 1.0 to 3.0 V. In comparisons to other nanowire TFTs, the present mobilities are substantially greater, with ZnO = 20 $cm^2 V^{-1} s^{-1}$, In_2O_3 = 35 $cm^2 V^{-1} s^{-1}$, and SnO_2 = 15 $cm^2 V^{-1} s^{-1}$.[11] This can be understood from the single-crystal nature of the As-doped In_2O_3 nanowires and the formation of relatively high-quality interfaces. Note that the present device performance rivals or exceeds that of previously reported doped and undoped metal oxide nanowire TTFTs.[20,21,33,34] Table 1 summarizes the relevant data which suggest that the As doping should significantly enhance overall nanowire device performance. Detailed statistical study of 10 single nanowire TTFTs (Figure S2, Supporting Information) reveals that the device mobility is 1200 $cm^2 V^{-1} s^{-1}$ on average with a standard deviation of 210 $cm^2 V^{-1} s^{-1}$, the subthreshold voltage is 170 mV/dec with a standard deviation of 90 mV/dec, and the I_{on}/I_{off} ratio is from 10^5 to 10^7.

To further modify device performance, the 50 nm Al_2O_3 gate dielectric was replaced with an organic self-assembled nanodielectric (SAND), layer (thickness ~16 nm, k_{eff} ~ 5; see the Supporting Information for details).[35] The mobility of a single As-doped In_2O_3 nanowire TFT is enhanced to ~2560 $cm^2 V^{-1} s^{-1}$ for V_g and V_{DS} = 4.4 and 200 mV, respectively. In addition, I_{on} is increased to 160 μA at V_g = 3.0 V and V_{DS} = 1.5 V, and S increased to 149 mV/dec (Figure S1a,b in the Supporting Information). These SAND effects can be attributed to the advantageous characteristics of the high-capacitance dipolar organic nanoscopic dielectrics.[36,37] A similar I_{on}/I_{off} ratio (~10^4) was previously reported for ZnO/SAND nanowire TFTs[38] and may result from the gate leakage current. The gate leakage current was measured between the source/drain pads and the back gate electrode (with overlapping area of ~2 × 10^5 μm^2) to be about 1 nA for the 16 nm SAND dielectric and 20 pA for

TABLE 1. Summary of the Electronic Properties of Different Doped and Undoped Metal Oxide Material-Based TTFTs

Material	on current (μA)	mobility ($cm^2/V \cdot s$)	on/off ratio	subthreshold slope (mV/dec)	ref
In_2O_3 NW	<1	98.1	2×10^4	N/A	25
In_2O_3 NW	10	514	10^6	160	19
In_2O_3 thin film	800	120	10^5	80	12
ZnO	2	96	10^6	300	19
Ta-SnO_2 NW	20	120	10^5	270	20
Sb-SnO_2 NW	22	550	10^5	170	33
Zn-In_2O_3 NW	8.5	80	10^6	700	34
As-In_2O_3 NW	60	1490	5.7×10^6	88	this work

the 50 nm Al_2O_3 dielectric at $V_g = 3$ V. This gate leakage current for SAND dielectric sets a lower limit for the off current that can be reliably measured and is likely a reason for the observed I_{on}/I_{off} ratio of 10^4 for the SAND-gated devices. We note that much of the measured leakage current may be conduction between the source/drain pads and the back gate electrode underneath, and thus the leakage current could be greatly reduced by using a patterned gate electrode with minimized overlap with the source and drain electrodes. Means to suppress this are under further investigation.

The present devices exhibit high mobilities and steep subthreshold slopes, which are desired properties for fast device operation, such as switching transistors in AMOLED displays. The unity-gain frequency of the nanowire TTFTs was estimated using eq 3, where $V_g - V_T$ is the gate overvoltage (the applied gate voltage in excess of the threshold voltage).[39]

$$f_T = \frac{\mu(V_g - V_T)}{2\pi L^2} \quad (3)$$

In this approximation, the unity-gain frequency of our TTFTs can reach 18.8 GHz. In addition, we also investigated the AC gain and radio frequency response (RFR) from the As-doped In_2O_3 nanowire TTFTs. Figure 2e shows the experimental setup for AC measurements. The nanowire TTFT is configured as common-source amplifier, and DC offsets are applied to the gate and drain electrodes to bias it in saturation, near the maximum g_m (~1.8 μS). Figure 2f shows the RFR of the device measured by applying digital signal processing (DSP) to the time domain signals (blue line), simulated data for the as-fabricated TTFT (red line), and simulated data for an optimized device structure (green line). A gain of ~6 dB can be observed at low frequency with a roll-off around 500 Hz and a cutoff frequency (f_{-3dB}) of ~1.5 kHz, which is comparable to earlier work. To understand the frequency response of our As-doped In_2O_3 nanowire TTFTs, a bilateral small-signal model[39] (shown in Figure 2g) is applied to model the AC characteristics of the present TTFTs. The simulated result (red line) agrees well with the measured data, suggesting that the operation frequency is strongly influenced by the parasitic capacitance associated with the source and drain contact electrodes (~157 pF) and the probes (~100 pF). By optimizing the device dimensions and structure (*i.e.*, use short channel widths and reduce overlaps between source and drain contact electrodes) and adopting an active probe (~1 MΩ) for the measurements, the cutoff frequency (f_{-3dB}) can be increased to 400 MHz, shown in the Figure 2f (green line). The simulated results, therefore, suggest that As-doped In_2O_3 nanowire TTFTs offer great potential in high-frequency device applications. Further optimization of the design toward functional, transparent integrated circuits is in progress.

Fully Transparent OLED Driving Circuitry. The ability to fabricate high-performance As-doped In_2O_3 nanowire TTFTs enabled further exploration of transparent circuit applications. Controlling a variable-intensity OLED was selected as the next target. Here a monochrome OLED is wire-bonded on a breadboard together with an As-doped In_2O_3 nanowire TTFT chip (Figure 3). The inset of Figure 3a shows the circuit diagram of the experimental setup, where one TTFT is connected to an external OLED, and V_{dd} is applied to drain of the transistor. By controlling V_{in} that provides a gate voltage for the transistor with fixed V_{dd}, the voltage drop across the OLED can be controlled. Figure 3a shows the current flowing through the OLED, which is successfully modulated *via* V_{in} by a factor of ~300, thus controlling the OLED light intensity, as shown in Figure 3b. OLED light intensity

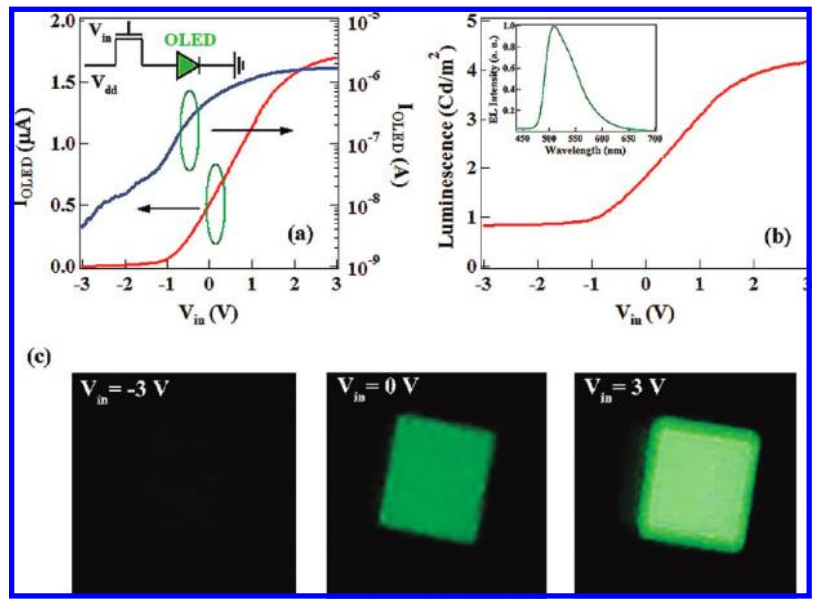

Figure 3. (a) Plot of the output current through the loaded phosphorus OLED (I_{OLED}) *versus* V_{in} with V_{dd} at 5.0 V in linear scale (red line) and log scale (blue line), respectively. Inset: Circuit diagram of an OLED driven by a transparent As-doped In_2O_3 nanowire transistor. (b) OLED light intensity *versus* V_{in} with $V_{dd} = 5.0$ V. Inset: OLED spectrum. (c) Optical images of the OLED under $V_{in} = -3.0$, 0.0, and 3.0 V.

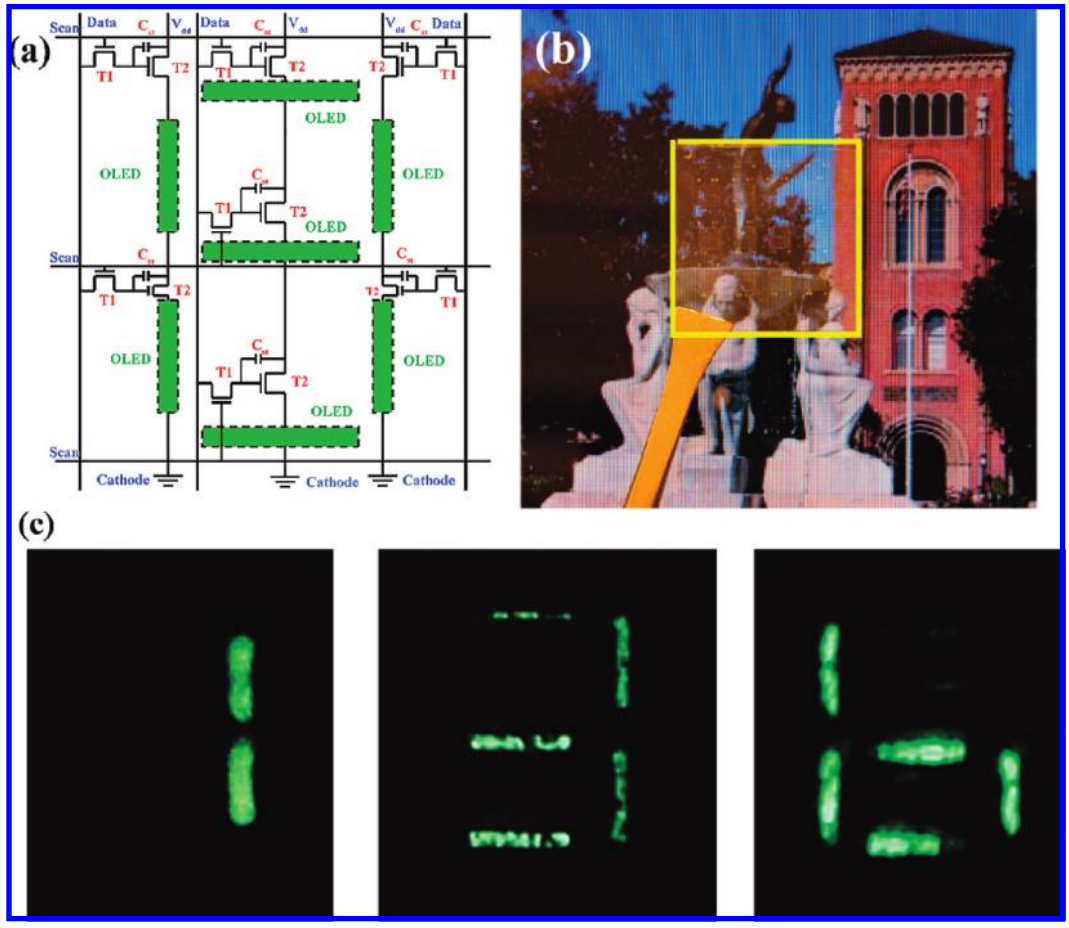

Figure 4. Application of As-doped In_2O_3 nanowire TTFT circuitry to drive a seven-segment AMOLED display. The phosphorus OLED structure is ITO/NPD/CBP:8% Irppy/BCP/LiF/Al. Details can be found in the Supporting Information. (a) Schematic of a seven-segment digit of AMOLED pixel, which consists of one switching transistor (T1), one driving transistor (T2), and one storage capacitor (C_{st}). The bias conditions to operate the circuit are −5 to 5 V of scan line to full turn-off and turn-on, varying −5 to 5 V on the data line, 3 V on the V_{dd} line, and 0 V on the cathode line. (b) Optical photograph of fully transparent AMOLED display before OLED layer deposition with the substrate area marked with a yellow frame for clarity. The feature on the background picture is clearly visible. (c) Optical photograph of AMOLED animation. The seven-segment digit displays numbers 1, 3, and 6, respectively.

below 1 Cd/m^2 is usually defined as the off-state and above 1 Cd/m^2 as the on-state.[40] Although the present off-state/on-state light intensity ratio is ~5, the effect is clearly visible in Figure 3c, where the OLED is operated with $V_{in} = -3$ (left), 0 (middle), and 3 (right) V.

AMOLED Display and Drive Circuitry. The discussion above demonstrates the high-performance characteristics of As-doped In_2O_3 nanowire/SAND TTFTs, including high device mobility and fast device operation, and can be employed as switching and driving transistors in an AMOLED display circuitry. Here, we go one step further to fabricate an AMOLED display using high-performance As-doped In_2O_3 TTFTs based on our earlier collaborative results on AMOLED display fabrication together with our cooperators and colleagues at Purdue University.[41] Figure 4a shows the equivalent circuit diagram of seven-segment AMOLED display circuitry. Note that the driving circuit of each OLED pixel consists of one switching transistor (T1), one driving transistor (T2), and one storage capacitor (C_{st}). T1 is employed to select a specified pixel and transfer data through the data line to the OLED. T2 is employed to control the current supplied to the OLED pixel, which is adjusted by controlling the V_g of T2, equal to the voltage difference between the ends of C_{st}. The storage capacitor is employed to store data during one period for time-varying operations. The EL opening area of each segment is ~0.18 mm^2.

AMOLED display fabrication begins by patterning the OLED ITO anode and individually addressed bottom gate electrodes by photolithography and wet etching. Next, 50 nm ALD Al_2O_3 is deposited on the patterned ITO gate and OLED anodes. Following Al_2O_3 deposition, contact holes above the OLED anodes, as bottom gate electrode contacts for each pixel, are fabricated through a wet etching process. After that, a suspension of As-doped In_2O_3 nanowires in 2-propanol alcohol is dispersed on the device substrate. A thin layer of source and drain electrodes

(20 nm Al) is then deposited by e-beam evaporation and patterned by lift-off. Following source and drain electrode patterning, a 200 nm thick SiO_2 layer is deposited by e-beam evaporation to passivate the device and planarize the nanowire transistors for OLED fabrication. The detail of OLED deposition can be found in the Supporting Information.

Figure 4b shows an optical image of a 1 in. × 1 in. AMOLED display substrate before OLED deposition, with a background image visible through the display region. The optical transmittance spectrum (Figure S3 in the Supporting Information) reveals that the optical transmittance values of the AMOLED display before and after OLED layer deposition are ~81 and ~35% in the visible region, respectively. The optical transmittance should be readily increased using a more transparent OLED design. The display consists of 12 seven-segment OLED pixels, 84 OLED unit pixels, and 156 nanowire TTFTs. For each seven-segment OLED pixel, the scan lines for all unit pixels are individually controlled, as are the data lines. Figure 4c shows optical images of the seven-segment pixels with different numerical digits at different data line voltages (V_{data} = −5 to 5 V) with different scan line voltages (V_{scan} = −5 to 5 V) and fixed V_{dd} (=3 V). To the best of our knowledge, this is the first demonstration of a seven-segment AMOLED display driven entirely by TTFT circuits.

In summary, we have demonstrated the great potential of As-doped In_2O_3 nanowires for high-performance transparent electronics. With the aid of arsenic dopants and a self-assembled gate nanodielectric, As-doped In_2O_3 nanowire TTFTs with transparent ITO contacts show good transparency and excellent transistor performance such as high mobility, high on/off ratio, low operation voltage, and steep subthreshold slope. A saturation device mobility of 1490 $cm^2 V^{-1} s^{-1}$ is achieved on glass substrates, which is the highest TTFT device mobility reported so far. We further examined the AC gain from a single As-doped In_2O_3 nanowire TTFT, and the results indicate good frequency response and a unity-gain frequency of 18.8 GHz. In addition, the TTFTs were further utilized to construct a transparent circuit and used to control a variable-intensity OLED. Moreover, an AMOLED display with good transparency was also fabricated which generates numerical displays. Our results suggest that As-doped In_2O_3 nanowires have great potential to serve as building blocks for future transparent electronics.

METHODS

As-Doped In_2O_3 Nanowire Synthesis. Ten nanometer gold nanoparticles were dispersed on a Si/SiO_2 substrate and utilized as catalysts in the nanowire synthesis. The substrate was then placed into a quartz tube at the down stream end of a furnace, while an InAs target was placed at the upper stream of the furnace. During the laser ablation process, the chamber was maintained at 760 Torr, 700 °C with a constant flow of 150 standard cubic centimeters (sccm) of Ar mixed with 10% H_2. The typical reaction time was about 50 min. After cooling, the samples were characterized using FESEM, TEM, XRD, and EDS.

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Supporting Information Available: Fabrication details for TTFTs and AMOLED. Electrical and optical data figures for TTFTs. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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