

Threshold Voltage and On–Off Ratio Tuning for Multiple-Tube Carbon Nanotube FETs

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Abstract—In this paper, we demonstrate postprocessing techniques to adjust the threshold voltage (V_t) and on–off ratio (I_{ON}/I_{OFF}) of multiple-tube carbon nanotube field effect transistors (CNFETs). These postprocessing techniques open up an additional degree of freedom to further tune individual CNFETs in addition to various device synthesis and processing techniques. We demonstrate proof-of-concept experiments and fully characterize their design spaces and tradeoffs. The techniques, *Threshold Voltage Setting* and *On–Off Ratio Tuning*, were able to adjust the threshold by as much as 2 V and tune the on–off ratio across 5×10^3 to 5×10^5 . In addition, V_t Setting could be used as an analysis tool to infer the V_t distribution of grown carbon nanotubes (CNTs). These tuning techniques, combined with processes such as doping, will enable high-performance multiple-nanotube devices.

Index Terms—Carbon nanotube field effect transistor (CNFET), ICs, nanotechnology.

I. INTRODUCTION

CARBON nanotube field effect transistors (CNFETs) are promising extensions to silicon complementary metal–oxide–semiconductor (Si-CMOS) technology because of their excellent intrinsic delay (CV/I) [1], [2]. Many groups have reported the fabrication of CNFETs consisting of only a single carbon nanotube (CNT¹) [3]. But single-tube CNFETs, while appropriate for scientific exploration, do not have sufficient current drive for practical circuit applications [4], so CNFETs with multiple nanotubes per device are required. Such multiple-tube CNFETs can show significant performance advantage over Si-CMOS in both inverter fanout-of-4 (FO4) delay (4.7 \times) and energy per cycle (2.6 \times) [5]. Multiple-tube CNFETs also enable new methods for tuning the device characteristics previously impossible with single-tube CNFETs. Here, we demonstrate two such techniques for tuning the threshold voltage and on–off ratio of multiple-tube CNFETs.

In FETs, the ability to tune the device threshold voltage (V_t) and on–off ratio (I_{ON}/I_{OFF}) is extremely important. For example,

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¹The nanotubes used in this paper are all horizontally aligned, single-walled carbon nanotubes.

in digital logic, an incorrect V_t can lead to digital gates with large short-circuit currents during switching, while a tuned V_t can result in optimal performance and reduced power dissipation. Similarly, a poor I_{ON}/I_{OFF} can cause slow output transitions or impractically low output swings, while an appropriate I_{ON}/I_{OFF} can improve speed and minimize leakage. We demonstrate V_t Setting and I_{ON}/I_{OFF} Tuning as effective techniques for tuning the device characteristics of multiple-tube CNFETs.

The V_t Setting and I_{ON}/I_{OFF} Tuning techniques presented here are applied postsynthesis/postprocessing, thus they complement and can be used in conjunction with many other techniques to achieve greater control. For example, there are existing and on-going efforts to develop techniques to control V_t and I_{ON}/I_{OFF} , including preferential growth of CNTs [6], [7], sorting/separating metallic CNTs from semiconducting CNTs [8], [9], plasma etching of metallic CNTs [10], and chemical doping of CNTs [11]. V_t Setting and I_{ON}/I_{OFF} Tuning can be applied to CNFETs in addition to the previous processes to attain greater device control; however, in this paper, we focus on proof-of-concept demonstrations of V_t Setting and I_{ON}/I_{OFF} Tuning as stand-alone techniques since many of the other developing techniques have not yet matured to sufficient robustness.

V_t Setting and I_{ON}/I_{OFF} Tuning adjust the threshold and on–off ratio of multiple-tube CNFETs by selectively pruning the composing CNTs within the device. This concept of device tuning is enabled by multiple-tube CNFETs, and would not otherwise be possible in single-tube CNFETs. A multiple-tube CNFET consists of many CNTs, each with its own threshold voltage and on–off ratio due to natural variations in CNT synthesis. Thus, there is a distribution of thresholds and a distribution of on–off ratios for the CNTs within the CNFET. The overall CNFET threshold voltage and on–off ratio is a function of this distribution, i.e., the aggregation of the individual CNT thresholds and on–off ratios determines the overall observed CNFET device threshold voltage and on–off ratio. Consequently, by selectively pruning the CNTs and shaping the distributions, V_t Setting and I_{ON}/I_{OFF} Tuning can adjust the device characteristics; however, this incurs tradeoffs with device drive current. In this study, CNT pruning is implemented using selective electrical burning of CNTs², a method similar to [12], but modified and extended appropriately to allow for the precise control and selectivity required for device tuning. The tradeoffs and design spaces for V_t Setting and I_{ON}/I_{OFF} Tuning via selective electrical burning are comprehensively characterized and analyzed.

²CNT pruning can potentially be implemented using other methods, such as selective plasma etching based on diameter, which is strongly correlated with CNT properties such as threshold and current drive.

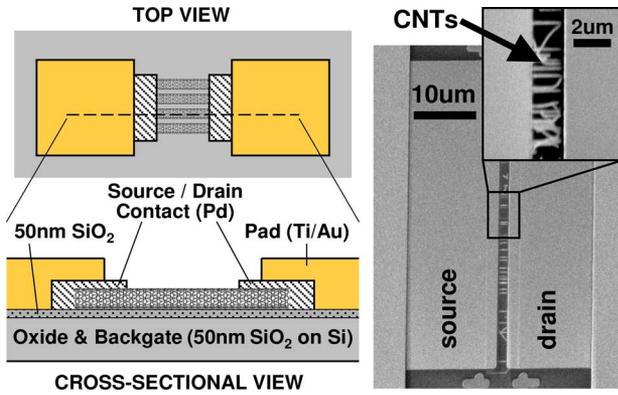


Fig. 1. Multiple-nanotube CNFET structure. The devices are back-gated, p-type CNFETs. The SEM image of the channel region shows CNTs in a $W/L = 50 \mu\text{m}/1 \mu\text{m}$ CNFET. CNT density is about 1–3 CNT/ μm , yielding an estimate of ~ 100 CNTs in this CNFET device.

II. FABRICATION OF CNFETS

Simple, substrate-gated CNFETs were fabricated as part of the proof-of-concept demonstration of these device tuning techniques. Horizontally aligned, single-walled carbon nanotubes were grown ($\sim 1\text{--}3$ CNTs/ μm density) on single-crystal quartz using ferritin catalyst in a chemical vapor deposition (CVD) furnace (similar to [13] and [14]). Using CNT transfer via a thermal-release adhesive tape [15], a process similar to [13], CNTs were transferred from the quartz substrate onto a 50-nm SiO₂/Si substrate for CNFET fabrication. Palladium (Pd) source/drain contacts [16] and titanium/gold (Ti/Au) pads were patterned on top of the CNTs (see Fig. 1). Next, the active device region (channel region) was masked using photoresist, and CNTs outside the channel region were etched away using oxygen plasma (100 W, 150 mtorr, 20 sccm O₂) for 2 min, thus leaving CNTs only in the device channel region (active region definition is important as it prevents “stray” CNTs from causing leakage paths between the gate and source/drain pads). Approximately 150 back-gated CNFETs of varying lengths (1–4 μm) and widths (10–50 μm), all p-type due to the palladium contacts and exposure to air [16], [17], were tested and tuned using V_t Setting and $I_{\text{ON}}/I_{\text{OFF}}$ Tuning.

III. THRESHOLD VOLTAGE (V_t) SETTING

The ability to adjust the threshold voltage (V_t) not only ensures proper logic functionality, but also allows optimization, such as reduced leakage, less variation, and multiple V_t circuit techniques. For CNFETs, there is currently no method for adjusting the V_t of each device independently; we present an option, V_t Setting, which selectively prunes the CNTs within a CNFET to adjust the CNFET V_t .

Before explaining CNT pruning and distribution shaping in detail, the definitions used in this paper are as follows.

- 1) V_t : The threshold voltage is defined and extracted from the device $I - V$ measurement using the *linear extrapolation* technique [18]. First, the $I_{\text{DS}} - V_{\text{GS}}$ curve is filtered appropriately to reduce the error due to measurement noise. The maximum transconductance (g_m) point is found and a line is extrapolated from this point with a slope equal

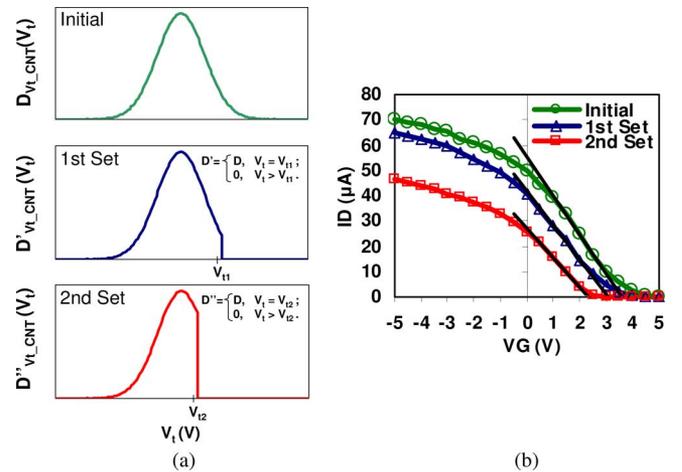


Fig. 2. Example of V_t Setting. V_t Setting was applied twice to shift the threshold voltage. (a) Conceptual illustration of how the upper branch of the V_{t_CNt} distribution is removed via selective CNT pruning. (b) Corresponding $I - V$ measurements. The black lines are used to extract the V_t . The results show V_t shifting from 3.6 V (“Initial”) to 3.1 V (“1st Set”) and then to 2.4 V (“2nd Set”). ($I_{\text{ON}} = I_{\text{D}}@V_{\text{GS}} = -5$ V; $V_{\text{DS}} = -1$ V; $W/L = 50 \mu\text{m}/1 \mu\text{m}$; CNT density = 1–3 CNTs/ μm).

to the maximum g_m . The voltage at which this line intersects the off-state current (I_{OFF}) is defined as the threshold voltage [18]. An illustration of the definition of V_t can be seen in Fig. 2(b).

- 2) I_{OFF} : The off-state current is defined as the value of the drain current (I_{D}) at $V_{\text{GS}} = 5$ V and $V_{\text{DS}} = -1$ V.
- 3) I_{ON} : The on-state current is defined as the value of the drain current (I_{D}) at $V_{\text{GS}} = -5$ V and $V_{\text{DS}} = -1$ V.

Fig. 2(a) illustrates the concept of selective CNT pruning to shape the distribution of CNT thresholds, and Fig. 2(b) shows the corresponding effects (actual measurements) on the device level. Each CNFET consists of multiple nanotubes, and each nanotube has its own threshold voltage (V_{t_CNt} ³). This forms a V_{t_CNt} distribution [see Fig. 2(a)], which then determines the overall CNFET threshold voltage (V_t) [see Fig. 2(b)]. V_t Setting adjusts the threshold by removing the upper tail of the V_{t_CNt} distribution. After selective electrical burning, the corresponding CNTs in the upper part of the distribution no longer contribute any current (they are purposely broken down), and thus, do not contribute to the CNFET device characteristics. Consequently, the overall CNFET V_t is shifted to a more negative value. As shown in Fig. 2, by removing more and more of the upper part of the V_{t_CNt} distribution, the corresponding CNFET $I - V$ curve exhibits shifts in the threshold voltage at the cost of reduced on-state current. The V_t was changed from 3.6 V (“initial”) to 3.1 V (“1st Set”) and then to 2.4 V (“2nd Set”), while incurring a total penalty of 33% reduction in I_{ON} from 70 to 47 μA .

A. Method

To set the desired CNFET V_t , CNTs with V_{t_CNt} more positive than the desired V_t were electrically burnt. V_G was set to

³ V_{t_CNt} refers to the threshold voltage of a CNT within a CNFET. V_t refers to the threshold voltage of the overall CNFET device.

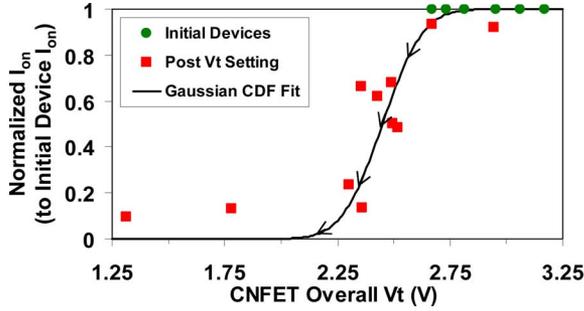


Fig. 3. V_t Setting design curve with I_{ON} versus V_t tradeoff. V_t Setting was repeatedly applied to six CNFETs to sweep the design space. The black arrowed line is the corresponding Gaussian CDF fit and represents the attainable design points for I_{ON} versus V_t tradeoff. The results also suggest the distribution of V_{t_CNT} 's is Gaussian with $\mu_{V_{t_CNT}} = 2.45$ V and $\sigma_{V_{t_CNT}} = 0.2$ V. ($I_{ON} = I_D @ V_{GS} = -5$ V; $V_{DS} = -1$ V; $W/L = 50$ $\mu\text{m}/1$ μm ; CNT density = $1-3$ CNTs/ μm).

the desired V_t , turning off and “protecting” all CNTs with a more negative V_{t_CNT} , while CNTs with V_t more positive than V_G remain “on” and susceptible to electrical breakdown (since these are p-type CNFETs). V_D was then swept up to -15 V repeatedly, and if necessary, as high as -35 V, to burn CNTs with V_{t_CNT} more positive than the desired V_t (V_S is set to 0 V). The result is a pruned distribution like that in Fig. 2(a) and a shifted V_t . This technique results in a tradeoff with current density; the tradeoff and design space were characterized by repeatedly applying the V_t Setting technique to a batch of CNFETs to sweep through the entire design space.

B. Results and Discussion

Fig. 3 illustrates the results and V_t Setting design space and tradeoff. The data points on the top right (circles) correspond to the initial CNFET devices with V_t 's ranging from 2.6 to 3.2 V. As V_t Setting is repeatedly applied, the V_t is set to more negative values and the current density is reduced as CNTs are selectively pruned (square data points in Fig. 3). The black curve is an approximate Gaussian cumulative distribution function (CDF) fit to describe the design space. Further tuning moves the design point down the curve along the direction of the arrows. Using this curve for interpolation, a V_t adjustment of 0.5 V from 2.9 V will incur a penalty of $\sim 64\%$ reduction in the current density.

In addition, V_t Setting can be used to analyze the threshold voltage distribution of the CNTs within the CNFET. Each data point in Fig. 3 represents the sum of the on-state currents of all CNTs with V_{t_CNT} less than the V_t at that data point, i.e.,

$$\text{Normalized } I_{ON}(V_t) = \frac{1}{k} \int_{-\infty}^{V_t} D_{V_{t_CNT}}(x) dx \quad (1)$$

where

$$k = \int_{-\infty}^{\infty} D_{V_{t_CNT}}(x) dx \quad (2)$$

is the normalizing constant and $D_{V_{t_CNT}}(x)$ is the distribution of V_{t_CNT} with respect to current (i.e., $D_{V_{t_CNT}}(x)$ is the amount of device current “gated” by the threshold $V_{t_CNT} = x$). Thus, the V_{t_CNT} distribution can be found by taking the derivative of

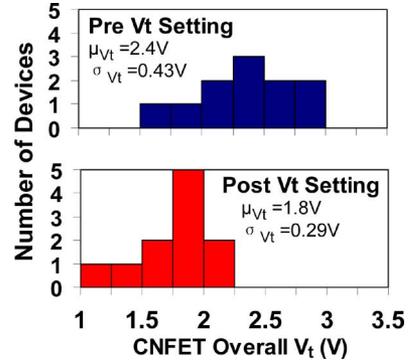


Fig. 4. Distribution of overall CNFET V_t for 11 devices. The distribution was measured after one V_t set step (target $V_t = 2$ V). The average V_t shifts down and the variation⁴ of the device V_t 's also decreased significantly, with nearly 65% of the CNFETs having V_t 's within 2 ± 0.25 V.

the design space curve. Using the Gaussian CDF fit in Fig. 3, the V_{t_CNT} distribution ($D_{V_{t_CNT}}$) can be inferred as a Gaussian distribution with $\mu_{V_{t_CNT}} = 2.45$ V and $\sigma_{V_{t_CNT}} = 0.2$ V⁴. In summary, V_t Setting can be used as an analysis tool for studying CNT synthesis, e.g., how growth conditions and factors impact the threshold distribution of the CNTs.

Another experiment was performed to study the variance of V_t after setting. V_t Setting was applied once to each of the 11 devices with a target V_t of 2 V. The histograms in Fig. 4 show that V_t Setting successfully shifts the CNFET V_t 's down to around 2 V, with an average V_t of 1.8 V (note that this error/offset can be systematically removed by compensating the original V_t set target; however, the exact characterization of this offset was not included in this study). Furthermore, V_t Setting also tightens the distribution of the V_t 's (σ_{V_t} ⁴ reduces from 0.43 to 0.29 V). Nearly 65% of the CNFETs have V_t 's within ± 0.25 V of the target (2 V), illustrating how V_t Setting can be used to obtain better matched multiple-tube CNFETs despite variability in the initial CNT composition.

It is important to note here that the fabricated multiple-tube CNFETs are depletion mode by nature [16], [17]; however, V_t Setting is certainly applicable to enhance-mode devices as well (or can convert depletion mode into enhancement mode if the depletion mode V_t is around 1 V). As methods to reliably synthesize enhancement-mode devices are still under development [19], we have chosen depletion-mode CNFETs for this V_t Setting proof-of-concept demonstration due to their ease and robustness of fabrication. Once the research of enhancement-mode multiple-tube CNFETs has matured to allow the fabrication of 100s of devices with high yield, V_t Setting can be applied to achieve tuned, high-performance logic and circuits.

IV. ON-OFF RATIO (I_{ON}/I_{OFF}) TUNING

Similar to V_t Setting, the CNFET I_{ON}/I_{OFF} can be adjusted by selectively pruning the CNTs within the CNFET. In this case, the conditions are applied to preferentially burn the

⁴ μ_{V_t} , σ_{V_t} describe the thresholds of the CNFETs, each consisting of multiple CNTs with V_{t_CNT} distribution described by the inferred $\mu_{V_{t_CNT}}$, $\sigma_{V_{t_CNT}}$ from Fig. 3.

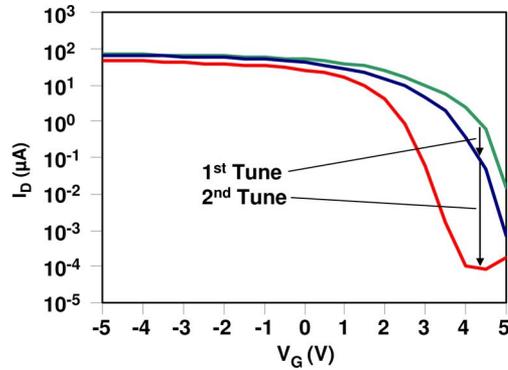


Fig. 5. Example of I_{ON}/I_{OFF} Tuning. A multiple-tube CNFET with metallic-CNTs already removed shows an on-off ratio of 5×10^3 . I_{ON}/I_{OFF} Tuning is applied twice to improve I_{ON}/I_{OFF} to 9×10^4 (“1st Tune”) and then to 3×10^5 (“2nd Tune”). ($V_{DS} = -1$ V; $L = 1$ μm ; CNT density = 1–3 CNTs/ μm).

high-leakage CNTs, resulting in an improved I_{ON}/I_{OFF} . Fig. 5 shows an example of I_{ON}/I_{OFF} Tuning, adjusting the CNFET I_{ON}/I_{OFF} from 5×10^3 to 9×10^4 and then to 3×10^5 .

A. Method

First, useful CNFETs with switching behavior (on-off ratio $> 10^3$) were obtained by removing metallic CNTs (m -CNTs) using an electrical burning method similar to [12].

Then, using these m -CNT-free CNFETs, I_{ON}/I_{OFF} Tuning was applied to finely adjust I_{ON}/I_{OFF} : the undesirable, high-leakage semiconducting CNTs (s -CNTs) that contribute proportionally more to the off-state leakage than to the on-state current were burnt to suppress the off-state leakage and improve I_{ON}/I_{OFF} . V_D was incrementally swept up to -25 V (in most cases, -15 V was sufficient) with $V_G = 15$ V and $V_S = 0$ V, which progressively burns away the high-leakage s -CNTs. By applying this technique repeatedly, a range of I_{ON}/I_{OFF} can be attained for the multiple-tube CNFET. I_{ON}/I_{OFF} Tuning also trades away current density (I_{ON}/W); this current density versus I_{ON}/I_{OFF} design space was characterized by progressively burning the CNTs in the CNFETs to sweep the design space.

B. Results and Discussion

Fig. 6 illustrates the results and I_{ON}/I_{OFF} Tuning design space/tradeoff. Region ① shows the initial CNFETs prior to m -CNT burning. These CNFETs contain both m -CNTs and s -CNTs, and exhibit high I_{ON} but impractically low I_{ON}/I_{OFF} .

Region ② is the m -CNT burning step. By burning away m -CNTs, the CNFET I_{ON}/I_{OFF} is greatly improved to more than 10^3 ; however, this step lacks fine control, and a jump in I_{ON}/I_{OFF} is observed from the initial range of 2–10 to about $10^3 - 10^4$.

Region ③ illustrates I_{ON}/I_{OFF} Tuning in devices with m -CNTs removed. The curved arrow in Region ③ approximates the I_{ON}/I_{OFF} versus I_{ON}/W design points attainable through I_{ON}/I_{OFF} Tuning. I_{ON}/I_{OFF} Tuning allows the on-off ratio to be precisely adjusted from 5×10^3 to 5×10^5 . At first, I_{ON}/I_{OFF} is improved by burning high-leakage CNTs. However, the bend in Region ③ marks the maximally attainable I_{ON}/I_{OFF} . At this point, most high-leakage s -CNTs have been burnt and high- I_{ON} s -CNTs (which contribute proportionally more to on-state

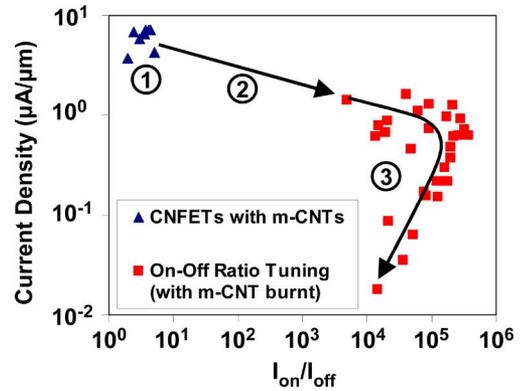


Fig. 6. On-Off Ratio Tuning design and tradeoff curve. Region ①: CNFETs containing both metallic CNTs (m -CNTs) and semiconducting CNTs (s -CNTs) have poor I_{ON}/I_{OFF} . Region ②: Electrical burning removes m -CNTs to obtain useful switching behavior. Region ③: I_{ON}/I_{OFF} Tuning on these m -CNT-void devices further removes high-leakage s -CNTs and I_{ON}/I_{OFF} can be finely adjusted (from $\sim 5 \times 10^3$ to $\sim 5 \times 10^5$) while trading off I_{ON}/W . But after all high-leakage CNTs are removed, high- I_{ON} CNTs begin to be burned with excessive application of the technique, so both I_{ON}/W and I_{ON}/I_{OFF} are reduced. The black curve/arrow in region ③ approximates the attainable I_{ON}/W versus I_{ON}/I_{OFF} design points. ($I_{ON} = I_D @ V_{GS} = -5$ V; $I_{OFF} = I_D @ V_{GS} = 5$ V; $V_{DS} = -1$ V; $L = 1$ μm ; CNT density = 1–3 CNTs/ μm).

current than to off-state leakage) begin to be burned, thus resulting in both diminished I_{ON}/I_{OFF} and I_{ON}/W with further burning. The first half of Region ③ suggests I_{ON}/I_{OFF} can be tuned from 5×10^3 to 5×10^5 while trading off $\sim 55\%$ current density (I_{ON}/W from 1.4 $\mu\text{A}/\mu\text{m}$ to 0.63 $\mu\text{A}/\mu\text{m}$).

V. CONCLUSION

We demonstrated V_t Setting and I_{ON}/I_{OFF} Tuning techniques for multiple-tube CNFETs and characterized their respective design spaces and tradeoffs. Using these tuning techniques, multiple-tube CNFETs with on-off ratios of 5×10^3 up to 5×10^5 can be achieved, and threshold voltages can also be adjusted by up to ~ 2 V. These techniques enable device tuning for performance optimization, and in some cases, can enable a completely new set of device operation (e.g., shifting V_t to transform depletion-mode devices into enhancement-mode devices). By enabling high-performance CNFETs, these techniques will allow practical, multiple-nanotube CNFET switches, complementary logic, and other circuits to be realized and investigated, advancing CNFET technology forward as a viable candidate for future ICs.

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He is interested in exploring how nanotechnology can emerge to become the future of large-scale ICs.

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