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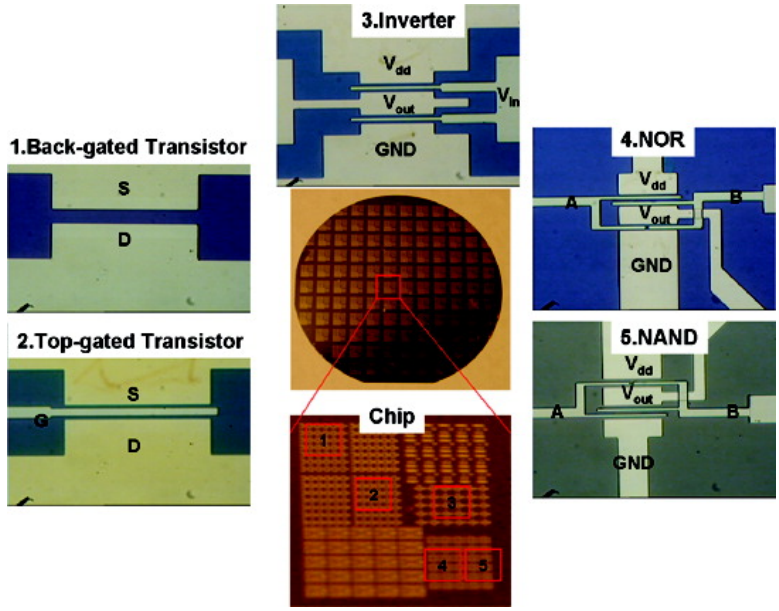


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# CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes

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## ABSTRACT

**Massive aligned carbon nanotubes hold great potential but also face significant integration/assembly challenges for future beyond-silicon nanoelectronics. We report a wafer-scale processing of aligned nanotube devices and integrated circuits, including progress on essential technological components such as wafer-scale synthesis of aligned nanotubes, wafer-scale transfer of nanotubes to silicon wafers, metallic nanotube removal and chemical doping, and defect-tolerant integrated nanotube circuits. We have achieved synthesis of massive aligned nanotubes on complete 4 in. quartz and sapphire substrates, which were then transferred to 4 in. $Si/SiO_2$ wafers. CMOS analogous fabrication was performed to yield transistors and circuits with features down to 0.5 $\mu$m, with high current density $\sim$20 $\mu$A/$\mu$m and good on/off ratios. In addition, chemical doping has been used to build fully integrated complementary inverter with a gain $\sim$5, and a defect-tolerant design has been employed for NAND and NOR gates. This full-wafer approach could serve as a critical foundation for future integrated nanotube circuits.**

Single-walled carbon nanotubes (SWNTs) are expected to offer much better performance for electronics than traditional silicon due to their high carrier mobility and current-carrying capacity. Nanotubes can work as ballistic and high mobility transistors,[1,2] and integrated logic circuits such as inverters and ring oscillators[3−7] have been constructed using individual nanotubes. Recently, significant advance has been made using randomly grown nanotube networks for flexible devices and circuits;[8] however, the stripe-patterning used to remove heterogeneous percolative transport through metallic nanotube networks cannot be easily scaled to submicrometer regime, and only PMOS transistors were demonstrated for the reported circuits. In parallel, aligned nanotubes, with potentially significant advantages over randomly grown nanotubes in terms of manipulation and integration of nanotubes for device applications, have been grown on either sapphire or quartz substrates from several research groups[9−12] or deposited on solid or flexible substrates by dielectrophoresis method for submicrometer rf devices.[13,14] On the basis of massively aligned SWNTs grown on sapphire, we have further reported a high-yield, registration-free nanotube-on-insulator approach to fabricate nanotube devices,[15] in a way analogous to the silicon-on-insulator process adopted by the semiconductor industry. The aligned nanotube devices such as transistors,[16] rf devices,[17] and high-frequency transistor oscillators[18] have also been made based on aligned nanotubes on quartz with good uniformity over chip scale and minimized parasitic capacitance. However, previous studies[15−18] on aligned nanotube devices usually share the following drawbacks: (1) small sample size which prevents wafer-scale fabrication and integration, (2) micrometer-scale channel length that limits the transistor performance, and (3) a lack of controlled doping that prevented truly integrated circuits with p-type and n-type transistors on one chip. To demonstrate truly integrated nanotube circuits and wafer-scale fabrication, technological components such as wafer-scale synthesis and transfer of aligned nanotubes and integrated submicrometer-scale device fabrication and tuning, are highly desired for the high-performance integrated nanotube circuits. In addition, defect-tolerant circuit design would also be an essential feature for such integrated nanotube circuits.

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Here, we report our recent advance on full wafer-scale processing of massively aligned carbon nanotube arrays for high-performance submicrometer channel transistors and integrated nanotube circuits, including the following essential components. (1) The massive highly aligned nanotubes were successfully grown on 4 in. quartz and sapphire wafers via meticulous temperature control and then transferred onto Si/$SiO_2$ wafers using a facile transfer printing method. (2) Wafer-scale device fabrication was performed on 4 in. Si/$SiO_2$ wafers to yield submicrometer channel transistors and circuits with high on-current density $\sim$20 $\mu$A/$\mu$m and good on/off ratios. (3) Chemical doping methods[19−23] were successfully demonstrated to get CMOS inverters with a gain $\sim$5. (4) Defect-tolerant circuit design for NAND and NOR was proposed and demonstrated to guarantee the correct operation of logic circuit, regardless of the presence of misaligned or mispositioned nanotubes. Our wafer-scale nanotube-on-insulator processing using multiple aligned nanotubes shows significant advantage over conventional processes based on individual nanotubes with respect to current output and device uniformity and suggests a practical and realistic approach for integrated nanotube circuit applications.

Figure 1 illustrates our full wafer processing including synthesis and transfer printing of aligned nanotubes and device fabrication. Aligned nanotube growth was previously limited to small pieces of quartz or sapphire substrates,[15,16] as growing nanotubes over complete 4 in. wafers has been very difficult due to the quartz wafer breakage during temperature ramping and the difficulty in uniform growth on complete wafers. Here, we successfully synthesized aligned SWNTs arrays (Supplementary Figure S1) on 4 in. quartz and sapphire wafers by overcoming the above-mentioned technical difficulties. First, both quartz and sapphire wafers were annealed to improve the alignment of nanotubes at 900 and 1100 °C for 1.5 h in air, respectively. In particular, the thermally robust a-plane sapphire wafer can be annealed at 1100 °C at high ramping rate (45 °C/min) as shown in Figure 1a, while the 4 in. quartz wafer required meticulous temperature control (extremely slow ramping rate <1 °C/min) to avoid wafer breakage due to the phase transformation[24] of quartz from alpha ($\alpha$) to beta ($\beta$) around 573 °C, as shown in Figure 1b. In addition, we used the same total gas flow rate for both the ramping up step (3000 sccm Ar and 600 sccm $H_2$) and the growth step (3000 sccm $CH_4$ and 600 sccm $H_2$) to minimize the temperature perturbation. A uniform temperature on the entire wafer is also an essential requirement for the uniform wafer-scale growth of aligned nanotubes on both quartz and sapphire wafers. Therefore, a 9 foot long growth furnace with three-zone temperature controller was used for this study.

After growth (Figure 1c), we used a facile transfer method to transfer the aligned nanotubes from 4 in. quartz or sapphire wafers to 4 in. Si/$SiO_2$ wafers as follows. A 100 nm thick gold film was first deposited onto the aligned SWNTs on the original substrate to ensure conformal contact between nanotubes and the gold film (Figure 1d). To transfer SWNTs onto the targeting substrate, our key innovation is the use of Revalpha thermal tape (from Nitto Denko), which has an interesting temperature-dependent adhesive property: it is highly adhesive at room temperature but loses its adhesion at a moderate temperature of 120 °C. This tape was pressed against the original substrate with nanotubes covered by the gold film, and then peeled off together with the gold film and nanotubes (Figure 1e). The nanotube/gold film/thermal tape trilayer structure was pressed against the target substrate, and the tape was then released by simply heating to 120 °C (Figure 1f). The gold film was subsequently removed using gold etchant, thus leaving a nice array of massively aligned SWNTs on the target substrate (Figure 1g). Scanning electron microscopy (SEM) images of transferred nanotubes on Si substrate with 50 nm thickness of $SiO_2$ are shown in inset of Figure 1g. The device fabrication based on transferred nanotubes on 4 in. Si/$SiO_2$ wafer (Figure 1h) was obtained by standard silicon CMOS technology such as projection photolithography using a stepper with 0.5 $\mu$m resolution for submicrometer device patterning, metal deposition for electrodes, and high $k$ dielectric ($HfO_2$ or $Al_2O_3$) deposition for gate dielectric. Figure 1i shows the photo images of nanotube devices built on a 4 in. Si/$SiO_2$ wafer, and a typical chip consisted of five different types of devices, including back-gated transistors, top-gated transistors, CMOS inverters, and CMOS, NOR, and NAND logic gates.

We first characterized the electrical properties of nanotube transistors as basic components for nanotube circuits. Compared with previous work[15,16] with micrometer or tens of micrometers channel length, we have pushed the channel length to submicrometer. Figure 2 shows a schematic diagram, SEM image, and electrical characteristics of back-gated nanotube devices. On the basis of the transferred nanotubes on Si with 50 nm $SiO_2$, 5 Å of Ti and 70 nm of Pd were deposited as source/drain electrodes (Figure 2a), followed by the removal of nanotubes outside the active channel with $O_2$ plasma. Such devices were made with channel lengths ($L$) of 0.5, 0.75, 1, 2, 5, 10, 20 $\mu$m and channel widths ($W$) of 2, 5, 10, 20, 50, 100 $\mu$m. The SEM image in Figure 2b shows a typical submicrometer channel device with two to three tubes/$\mu$m. Figure 2c exhibits the current-gate voltage ($I_{ds} - V_g$) characteristics of the transistors at $V_{ds} = 1$ V with $W = 100$ $\mu$m and various channel lengths, showing on-currents at $V_g = -10$ V varying from several tens of microamperes to 1.8 mA, reversely proportional to the channel length. The normalized on and off current densities ($I_{ds}/W$) are further deduced from the same devices in Figure 2c, and the transconductances ($g_m$) are also calculated from the linear proportion of the transfer curves, as shown in Figure 2d. The highest on-current density in a transistor with $W = 100$ $\mu$m and $L = 0.5$ $\mu$m is up to 20 $\mu$A/$\mu$m, and $g_m$ is close to 100 $\mu$S. This on-current density is the highest achieved so far for aligned nanotube transistors, as a result of the submicrometer channel length we used. The performance of these devices can be improved even further with higher-density nanotubes. To estimate the nanotube mobility, devices with long channel lengths are selected to minimize the effect of metal/nanotube contacts. An effective device mobility of 2685 $cm^2$ $V^{-1}$ $s^{-1}$ was

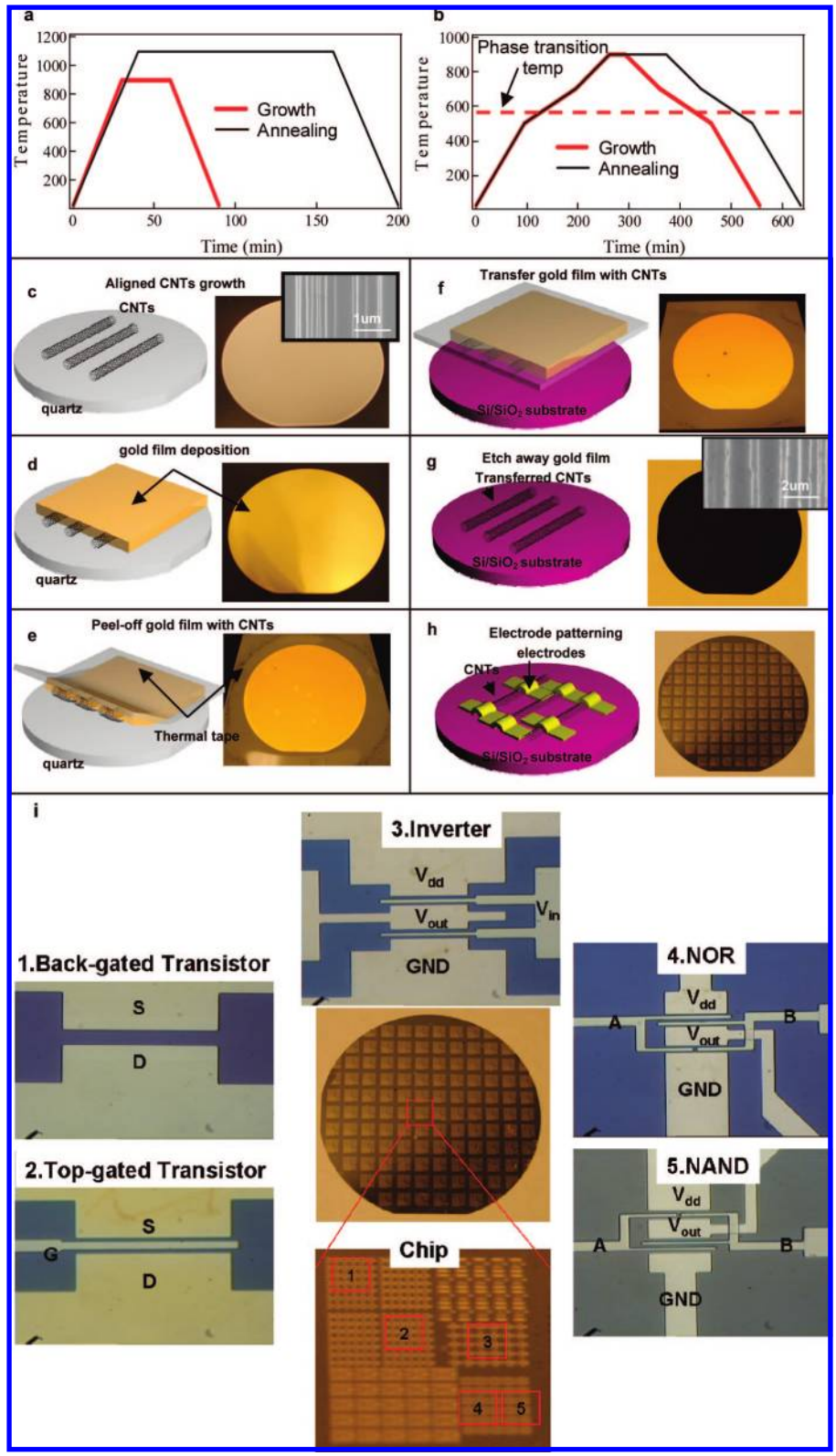


**Figure 1.** Wafer-scale aligned nanotube synthesis, transfer, and fabrication. (a, b) Temperature flowcharts for annealing and nanotube growth on sapphire and quartz wafers, respectively. (c) Schematic diagram and photograph of full wafer synthesis of aligned nanotubes on a 4 in. quartz wafer. Inset shows SEM image of aligned nanotubes. (d−h) Schematic diagrams and photographs showing the transfer procedure, i.e., gold film deposition (d), peeling off the gold film with nanotubes (e), transfer of the gold film with nanotubes onto a $Si/SiO_2$ substrate (f), etching away the gold film (g), and device fabrication on the transferred nanotube arrays (h). (i) Photo images of nanotube devices and circuits built on a 4 in. $Si/SiO_2$ wafer: 1, back-gated transistor; 2, top-gated transistor; 3, CMOS inverter; 4, NOR logic gate; 5, NAND logic gate.

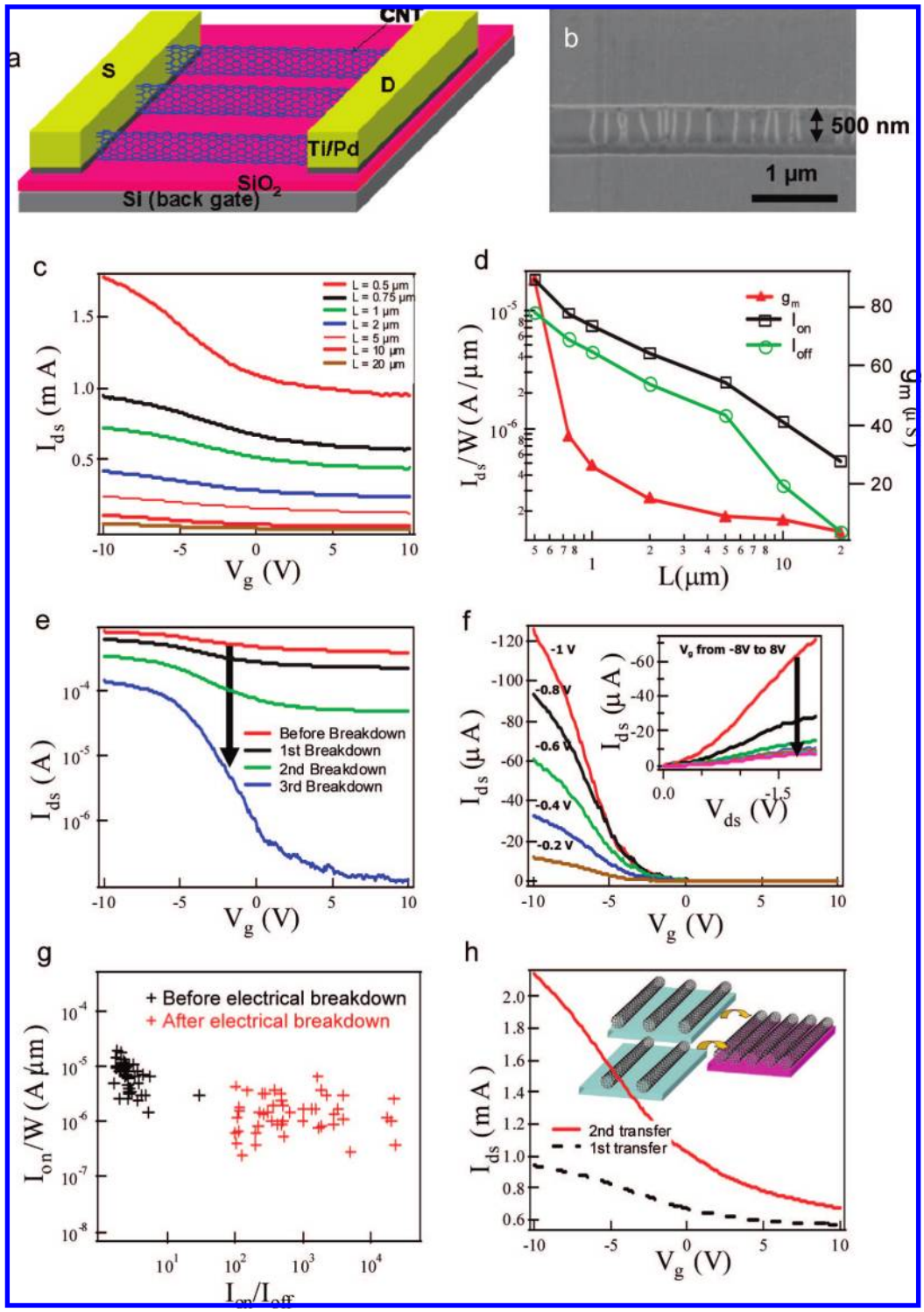


**Figure 2.** Characteristics of back-gated transistors down to submicrometer channel length. (a) Schematic diagram of a back-gated transistor built on transferred nanotubes. (b) SEM image of a transistor with submicrometer channel length. (c) Transfer ($I_{ds} - V_g$) characteristics of transistors with different $L$ = 0.5, 0.75, 1, 2, 5, 10, and 20 $\mu$m, and $W$ = 100 $\mu$m. (d) Normalized on and off current densities and transconductance ($g_m$) derived from (c). (e−g) Electrical breakdown study of the transistors; $I_{ds}-V_g$ curves for a typical transistor after consecutive electrical breakdown (e), $I_{ds}-V_g$ curves and $I_{ds}-V_{ds}$ curves of the transistor in (e) after three rounds of electrical breakdown (f), and statistics of devices before and after electrical breakdown (g). (h) $I_{ds}-V_g$ curves of two representative devices, with one (black) and two (red) steps of transfer, respectively. Inset illustrates the multiple transfer process.

obtained for typical devices with 50 $\mu$m channel length, asdescribed in Supporting Information (S5). By assuming that one-third of the nanotubes are metallic, one can further derive a nanotube mobility of 3571 cm$^2$ V$^{-1}$ s$^{-1}$.

To improve the on/off ratio ($I_{on}/I_{off}$), controlled electrical breakdown[25] was used to remove metallic and high-leakage semiconducting nanotubes. Specifically, we developed an automated electrical breakdown process by setting target on/

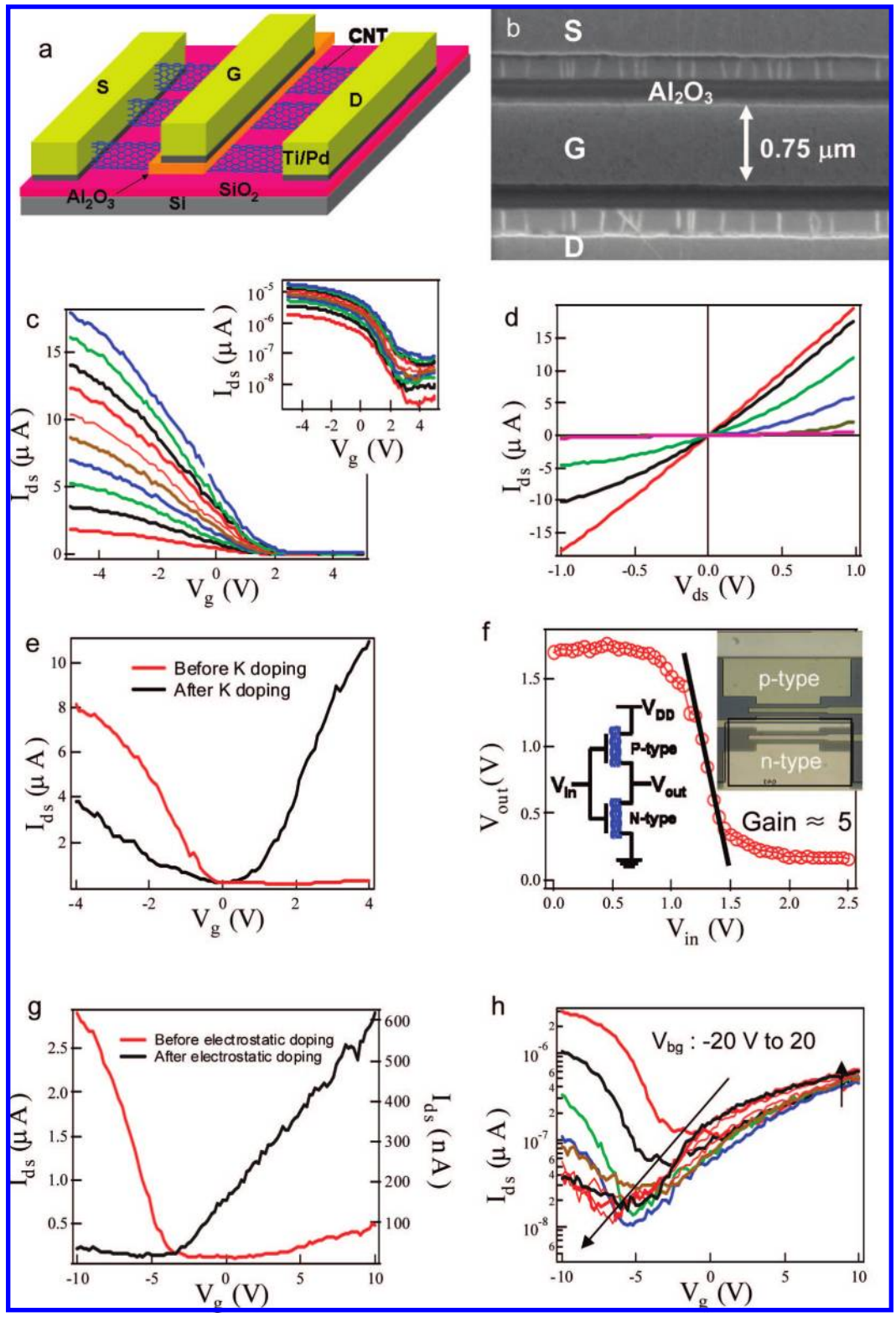


**Figure 3.** Top-gated transistors for doping and truly integrated CMOS inverters. (a, b) Schematic diagram and SEM image of a top-gated transistor, respectively. (c) $I_{ds}-V_g$ curves of the transistor with $L = 3$ $\mu$m and $W = 25$ $\mu$m at different $V_{ds} = 0.1$ to 1.1 V in steps of 0.1 V. Inset: $I_{ds}-V_g$ curve in logarithm scale. (d) $I_{ds}-V_{ds}$ curves at different $V_g = -20$, $-15$, $-10$, 10, 15, and 20 V for the same device in (c). (e) $I_{ds}-V_g$ curves of the top-gated transistor before (red) and after (black) K doping. (f) Voltage transfer characteristic (VTC) of a CMOS inverter with selective K doping. Inset: schematic diagram (left) and photograph (right) of the circuit. (g) $I_{ds}-V_g$ curves of a dual-gated transistor before (red, back gate at $-20$ V) and after (black, back gate at 20 V) electrostatic doping. (h) $I_{ds}-V_g$ curves at different $V_{bg} = -20$ to 20 V for the same device in (e), showing a significant shift of threshold voltage and enhancement of n-type conduction.

off ratio and on-current and then using computer control to perform multiple steps of breakdown until the target values were reached. This process, when combined with an automatic probe station, can make electrical breakdown fairly

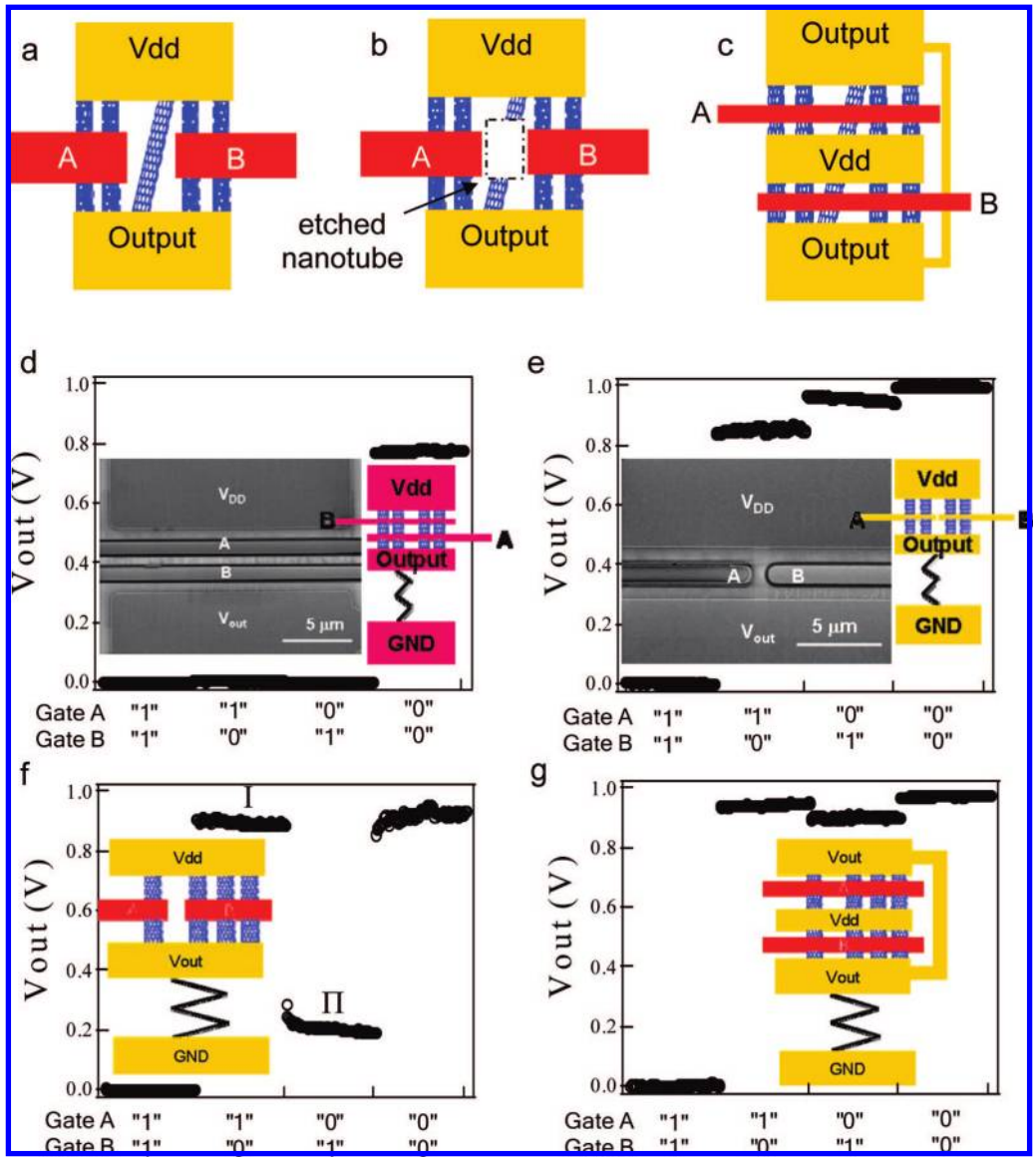


**Figure 4.** PMOS NOR and NAND gates with top-gated transistors. (a−c) Schematic diagrams of a defect-influence layout and two defect-tolerate layouts with two transistor in parallel, respectively. (d, e) Output characteristics of PMOS NOR and NAND, respectively. Inset: SEM image of integrated pull-up networks and schematic diagram of PMOS circuits. (f, g) Output characteristics of PMOS NAND with pull-up networks (b) and (c), respectively, where the nanotube density was not uniform in the circuit, as depicted in schematic diagram in inset.

practical for wafer-scale processing. The back-gate was set to 15 V to turn off the desired semiconducting nanotubes, while the source/drain voltage ($V_{ds}$) was swept from 0 to −35 V to electrically stress and break the undesired tubes. The $I_{on}/I_{off}$ of a transistor with $W = 100$ $\mu$m and $L = 0.75$ $\mu$m in Figure 2e significantly increased from ~2 to $10^3$ with multiple steps of electrical breakdown, accompanied by a moderate degradation of the on current. After electrical breakdown, Figure 2f and inset show the $I_{ds}-V_g$ curves at different $V_{ds}$ from −0.2 to −1 V and $I_{ds}-V_{ds}$ curves at different $V_g$ from − 8 to 8 V. Figure 2g is a statistical study of about 50 devices from altogether 10 chips with $L = 0.75$ $\mu$m and various $W$ before and after electrical breakdown, where the on-state current density is plotted versus the on/off ratio. $I_{on}$ is measured at $V_{ds} = 1$ V and $V_g = -10$ V, and $I_{off}$ is measured at $V_{ds} = 1$ V and $V_g = 10$ V. Before breakdown, the devices exhibited on/off ratios in the range of 1 to 10, due to the presence of metallic nanotubes. In contrast, after electrical breakdown, the on/off ratios underwent significant improvement to the range of $10^2-10^5$, which can be used as building blocks for the following nanotube circuits. More details about the on/off ratio and on-state current distribution can be found in Supporting Information (S6).

In addition to the tuning of the on/off ratio using electrical breakdown, we can adjust the transistor conductance by performing multiple steps of nanotube transfer to increase the tube density. Figure 2h shows the $I_{ds}-V_g$ curves of two representative devices, with one and two steps of transfer, respectively. Devices fabricated in the double transfer region showed ~2.2 times more current per unit width in Figure 2h. Multiple nanotube transfer is a novel technique to

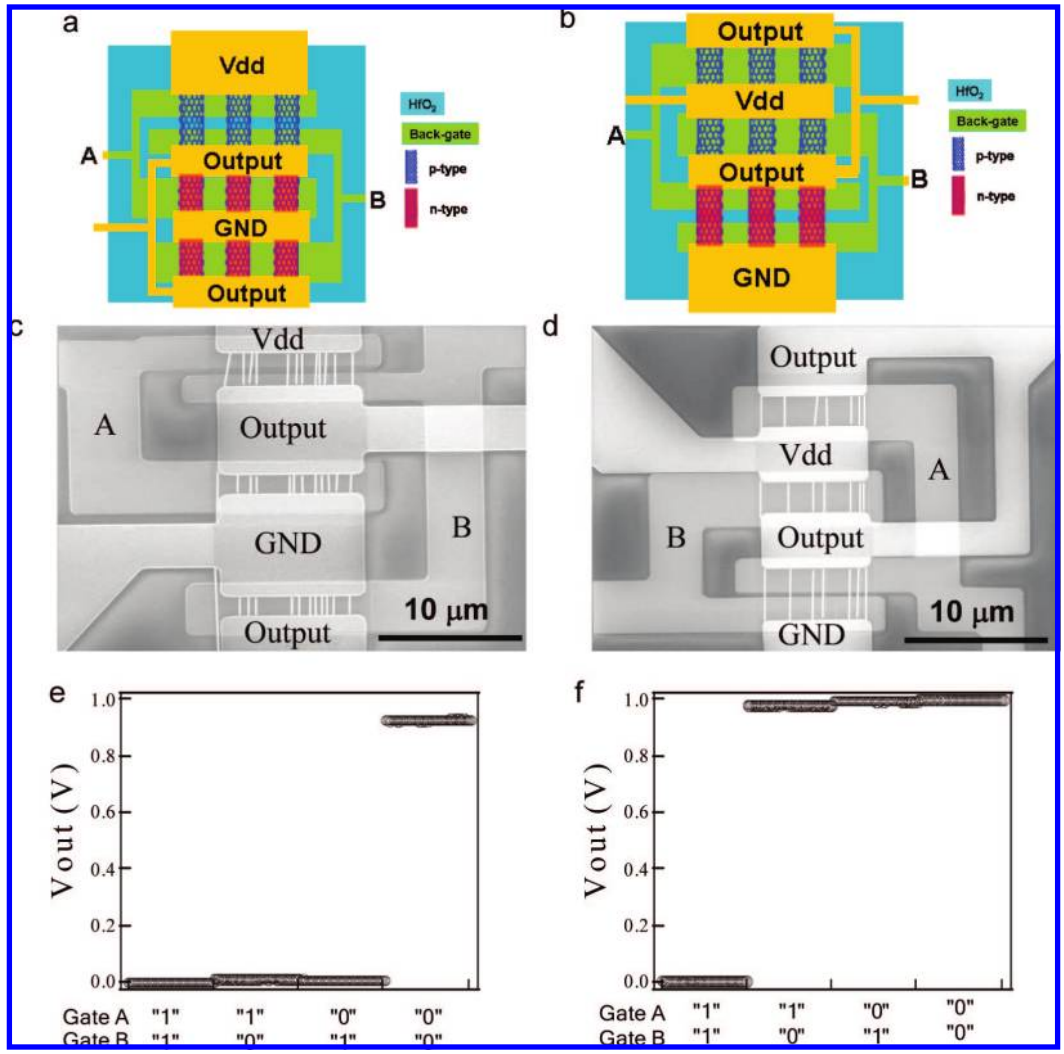


**Figure 5.** Defect-tolerant CMOS NOR and NAND with individual back-gated transistors. (a, b) Schematic diagrams of CMOS NOR and NAND, respectively. (c, d) SEM images of CMOS NOR and NAND, respectively. (e, f) Output characteristics of CMOS NOR and NAND, respectively.

compensate the decreased current after electrical breakdown, and additional transfers can be performed to achieve even higher current densities.

Besides the back-gated devices, top-gated devices were fabricated by defining top-gate electrodes on back-gated devices. Compared with the common back-gate devices, the top-gate structure has an intrinsic benefit such as individual control of each transistor in a nanotube circuit. In order to make the top-gate electrodes, we first formed the pattern using photolithography, deposited 50 nm of $Al_2O_3$ using atomic layer deposition (ALD) as top-gate dielectric, and then deposited 5 nm of Ti/45 nm of Pd as the top-gate electrodes, followed by the lift-off process. Figure 3a illustrates a schematic diagram of a top-gated device, where top gate partially covers the active channel so that nanotubes can be exposed to n-type dopants such as potassium. In Figure 3b, one can clearly see nanotubes which bridge between S/D electrodes and are partially covered by $Al_2O_3$ and top-gate. Panels c and d of Figure 3 are the typical transfer characteristics ($I_{ds}-V_g$ curves) and output characteristics ($I_{ds}-V_{ds}$ curves) for a transistor with $W = 25\ \mu$m, $L = 3\ \mu$m, and top-gate length $= 1\ \mu$m after proper electrical breakdown. The $I_{ds}-V_{ds}$ curves appear to be very linear, indicating that ohmic contacts are formed between the electrodes and the nanotubes. The on-current is measured to be 20 $\mu$A, corresponding to a current density of 0.8 $\mu$A/$\mu$m, and the on/off ratio exceeds $10^4$. We used such devices in the following doping study.

One of the most important characteristics of CMOS circuits is low static power consumption. Significant power is only drawn when the CMOS circuits are switching between on and off states. Unlike doping in silicon CMOS processes, nanotubes cannot be easily doped via ion implantation. The ability to obtain both p- and n-type nanotube FETs, therefore, is important to construct complementary electronics. A p-type nanotube device can be doped electrostatically, substitutionally, or via charge transfer to convert it into an n-type one. Four different methods, with potassium[21,22] and electrostatic[23] doping for top-gated devices, and polyethilenimine (PEI)[19] and hydrazine ($N_2H_4$)[20] for back-gated ones, have been studied here to produce n-type transistors and to evaluate the most practical way for integrated circuits. In order to dope nanotube devices with potassium, we first spin-coated poly(methyl methacrylate) (PMMA) as a capping layer for

p-type transistor and then opened up the window for other devices which can be altered into n-type after doping, as shown in inset of Figure 3f. This device was loaded into high vacuum ($\sim 10^{-5}$ Torr), followed by the evaporation of potassium. Figure 3e shows the $I_{ds}-V_g$ characteristics of the top-gated transistor before and after potassium doping. This doping produced an n-type transistor by shifting the Fermi level of nanotubes to the conduction band, and the conductance of the transistor increased at positive gate voltage. The potassium doping has clear advantage over other doping methods such as PEI showing low on−off ratio (Figure S2) and $N_2H_4$ with toxicity and difficulty in integration (Figure S2). Armed with potassium doping, we have constructed a truly integrated CMOS aligned nanotube inverter, i.e., with the p-type and n-type transistors residing on one chip and located side by side. Figure 3f includes the voltage transfer characteristics (VTC), the schematic diagram, and the photo image of the CMOS inverter. Our inverter was operated with a VDD = 2 V and an input voltage range from 0 to 2.5 V, and the gain deduced from VTC data was 5, which can be high enough to drive a more complicated logic circuit such as a ring oscillator.

In addition to potassium doping, electrostatic doping has been studied on top-gated transistors with Si common back-gate. We utilized electrostatic doping effects[23] in the dual-gate nanotube FET to obtain the polarity control (p or n) and to tune the threshold voltage of FET. Figure 3g exhibits the current−gate voltage ($I_{ds}-V_g$) characteristics of the dual-gated transistor and clearly shows p- and n-type properties at back-gate voltage ($V_{bg}$) = −20 and 20 V, respectively, which can be understood as follows. For sufficiently negative (or positive) back-gate voltage, the Schottky barriers are thinned enough to allow for hole (or electron) tunneling from the metal contact into the nanotube, and thus the nanotube channel can be electrostatically doped into p-type or n-type. Therefore, varying the top gate voltage can switch on and off the transistor with assist of back-gate voltage, which determines the type of majority carrier and the device on-current. In our device, the n-type conduction is slightly lower than the p-type conduction, which is attributed to asymmetrical Schottky barrier heights for holes and electrons and environmental doping effect from $O_2$ and moisture. We also measured the current versus the top-gate voltage ($I_{ds}-V_g$) at different back-gate $V_{bg}$ from −20 to 20 V, and a significant shift of threshold voltage and enhancement of n-type conduction were observed from 0 to −6 V, as shown in Figure 3h. Compared with other doping methods such as potassium and hydrazine, which are not stable in air, the electrostatic doping is stable and tunable but requires sophisticated device structure and circuit design.

On the basis of top-gated aligned nanotube transistors, more sophisticated PMOS circuits have also been demonstrated. It is, however, inevitable that there are misaligned or misoriented nanotubes in these devices, which can result in incorrect logic behavior. Therefore, an innovative circuit design such as defect-tolerate structure is required to guarantee the correct logic behavior. We hereby report defect-immune circuit layouts for PMOS NOR and NAND circuits. Panels a−c of Figure 4 show a defect-influence layout and two defect-tolerate layouts with transistors connected in parallel, respectively. For Figure 4a, misaligned nanotubes outside the gates are not under the control of either gate and therefore may impair the logic operation. In Figure 4b, the nanotubes lying between gate A and B are removed using oxygen plasma etching, and thus this design is immune to such misaligned nanotubes. Furthermore, Figure 4c represents an even better design, where two transistors controlled by gates A and B are connected in parallel and utilize the same bunch of aligned nanotubes. This design enables virtually identical device performance between two parallel transistors, as shown in Figure S3.

We fabricated PMOS circuits using the defect-immune layout. Panels d and e of Figure 4 include SEM images of the integrated pull-up networks, the schematic diagrams, and the output characteristics for PMOS NOR and NAND, respectively. A 20 MΩ resistive load was chosen so that it was between the on-state resistance and the off-state resistance of the transistors. The NAND and NOR circuits were both operated with a VDD of 1 V. Voltages of 10 V and −10 V applied on gates A and B were treated as logic "1" and "0", respectively. For the NAND, the output was "1" when either one of the two inputs was "0", while for the NOR, the output was "0" when either one of the two inputs was "1". These output characteristics confirm that our circuits realized the logic function correctly. However, the design in Figure 4b may suffer from the problem of having nonuniform nanotube density and consequently different characteristics for gate A and B. Figure 4f shows the data and schematic diagram of a PMOS NAND gate, where the nanotube density happened to be nonuniform. One can clearly see that the outputs were asymmetric between points I and II, and also the transfer characteristics for gate A and B showed a significant difference in terms of on-current (Figure S3). The low output at the point II was attributed to the relatively large dc current leakage through the pull-down resistor, which was comparable to the on-current of transistor controlled by gate A. In contrast, for the NAND with design shown in Figure 4, panels c and g inset, the transistor transfer characteristics (Figure S3) and the outputs of circuits were more symmetric than the ones in Figure 4f. This confirms that the NAND design in Figure 4c performed the logic function correctly even with nonuniform nanotube density and misaligned nanotubes.

While PMOS logic is easy to design and manufacture, it has several shortcomings as well. The worst problem is that current flows through the pull-down resistor when the pull-up network is active, as discussed above. This leads to static power dissipation even when the circuit sits idle. In order to overcome such a problem, CMOS nanotube circuits have been studied here using the defect-tolerant design with individual back-gates for efficient chemical doping. Specifically, the individual back-gated devices have relative advantages over the top-gated ones, such as easy chemical doping and electrical breakdown owing to the fully exposed device structure. For the individual back-gated devices, we first defined individual back-gate electrodes on a $Si/SiO_2$

wafer via photolithography, 5 nm Ti/ 45 nm Au deposition, and a lift-off process. A 50 nm ALD $HfO_2$ was deposited as the gate-dielectric, and then the aligned nanotubes were transferred. Finally, the source/drain electrodes were formed. The CMOS NOR and NAND are depicted in panels a and b of Figure 5, respectively. After the device fabrication, we performed the potassium doping to get n-type devices as mentioned in the CMOS inverter study. Panels c and d of Figure 5 show SEM images of the CMOS NOR and NAND, respectively. The pull-up and pull-down networks were built on the same nanotube arrays, and the pull-down network was converted from p-type into n-type after potassium doping, as shown in Figure S4. Compared with the PMOS circuits, the CMOS logic circuits showed almost ideal performance, where the outputs were close to 0 or 1.0 V, as shown in Figure 5, panels e and f.

In summary, we have reported significant progress on CMOS-analogous wafer-scale processing of integrated aligned nanotube circuits, including progress on wafer-scale synthesis and transfer of aligned nanotubes, metallic nanotube removal and chemical doping, and defect-tolerant integrated nanotube circuits. Synthesis of massive aligned nanotubes has been achieved on complete 4 in. quartz and sapphire substrates, followed by successful transfer of the nanotubes to 4 in. Si/$SiO_2$ wafers. CMOS analogous fabrication was performed to yield transistors and circuits with features down to 0.5 $\mu$m, with high current density $\sim$20 $\mu$A/$\mu$m, and good on/off ratios. In addition, extensive chemical doping has been studied and used to build fully integrated complementary inverters with a gain $\sim$5, and defect-tolerant designs have been proposed and employed for NAND and NOR gates. Our work represents significant advance toward the challenging task of nanotube assembly and integration for future beyond-silicon integrated circuits.

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**Supporting Information Available:** Photograph and SEM images of aligned nanotubes on 4 in. quartz wafer (S1), in-depth doping studies using PEI and $N_2H_4$ (S2), comparison of two defect-tolerant designs on the PMOS NAND logic circuits with nonuniform nanotube density (S3), transfer characteristics of the CMOS NAND before and after doping (S4), effective device mobility (S5), and device statistics including on-current and on/off ratio before and after electrical breakdown (S6). This material is available free of charge via the Internet at http://pubs.acs.org.

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